

TRANSISTOR CIRCUIT DESIGN

Heathkit



**Educational
Systems**

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INTRODUCTION

This is the second course in the Heathkit/Zenith Engineering Circuit Design Series. Prerequisites for this course include:

1. A knowledge of the techniques used to analyze DC and AC circuits.
2. A knowledge of elementary algebra.
3. The ability to analyze and design basic passive circuits.

The required prerequisite material is thoroughly covered in the Heathkit/Zenith **Passive Circuit Design** course.

As the title implies, the principle objective of this course is to teach you how to design useful transistor circuits. To accomplish this objective, the course will:

1. Describe device characteristics and define relevant parameters.
2. Using simplified models, develop the appropriate AC and DC equivalent circuits.
3. Analyze the equivalent circuits to determine how various component values affect the operation of a given circuit.
4. Follow the analysis examples with specific design examples that take you step-by-step through the actual design process.

Perhaps the most unique feature of this course is the abundance of **summary** and **design guides** that are provided in Units 1 through 8. By referring to these guides, you should be able to design a multitude of useful transistor circuits.

The information in Units 1 through 8 is complemented by thirteen hands-on experiments in Unit 9. The easiest way to perform these experiments is with the Heathkit/Zenith ET-1000 Engineering Design Trainer — which contains all of the necessary functions to complete all of the experiments.

I do hope you enjoy this course. As always learning is, and should be, fun.

Sincerely

Vincent F. Leonard Jr.

COURSE OBJECTIVES

When you complete this course, you should be able to:

1. Analyze and design RC-coupled common-emitter, common-base, and common-collector class A voltage amplifiers.
2. Analyze and design class A RC-coupled and class A transformer-coupled power amplifiers.
3. Analyze and design class AB complementary symmetry power amplifiers.
4. Analyze and design elementary differential amplifiers using constant-current source biasing techniques.
5. Analyze and design a two-stage, RC-coupled voltage amplifier.
6. Describe the characteristics of voltage-series negative feedback.
7. Analyze and design common-source and common-drain voltage amplifiers.
8. Predict the approximate lower and upper (F_1 and F_2), cutoff frequencies for common-emitter voltage amplifiers.

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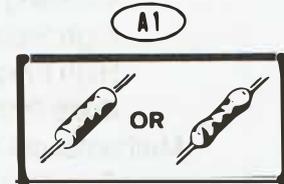
PARTS LIST

This list contains all of the parts for the experiments that you will perform with this course. The key numbers correspond to the numbers on the parts illustrated in the column. Some parts are packaged in envelopes. Except for this initial parts check, keep these parts in their envelopes until they are called for in an experiment.

KEY No.	PART No.	QTY	DESCRIPTION
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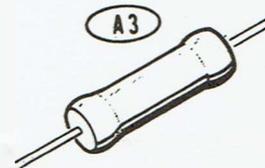
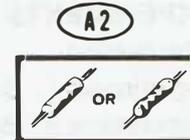
1/2 — WATT RESISTORS

A1	6-101	1	100Ω
A1	6-181	1	180Ω
A2	6-750	5	75Ω



1/4 — WATT RESISTORS

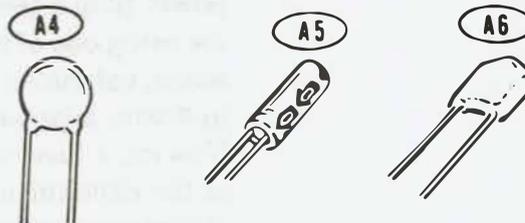
A2	6-101-12	1	100Ω
A2	6-102-12	2	1kΩ
A2	6-103-12	3	10kΩ
A2	6-104-12	2	100kΩ
A2	6-105-12	2	1MΩ
A2	6-121-12	2	120Ω
A2	6-123-12	2	12kΩ
A2	6-151-12	1	150Ω
A2	6-152-12	2	1.5kΩ
A2	6-155-12	1	1.5MΩ
A2	6-182-12	1	1.8kΩ
A2	6-221-12	1	220Ω
A2	6-222-12	3	2.2kΩ
A2	6-223-12	1	22kΩ
A2	6-224-12	1	220kΩ
A2	6-225-12	1	2.2MΩ
A2	6-273-12	2	27kΩ
A2	6-274-12	1	270kΩ
A2	6-332-12	2	3.3kΩ
A2	6-333-12	2	33kΩ
A2	6-335-12	1	3.3MΩ
A2	6-392-12	1	3.9kΩ
A2	6-471-12	1	470Ω
A2	6-472-12	2	4.7kΩ
A2	6-473-12	1	47kΩ
A2	6-561-12	2	560Ω
A2	6-562-12	2	5.6kΩ
A2	6-681-12	2	680Ω
A2	6-682-12	1	6.8kΩ
A2	6-684-12	1	680kΩ
A2	6-822-12	1	8.2kΩ
A2	6-823-12	1	82kΩ
A3	6-685-1	1	6.8MΩ, 1 watt
A3	6-100-2	1	10Ω, 2 watt
A3	3-7-2	1	1Ω, 2 watt



KEY No.	PART No.	QTY	DESCRIPTION
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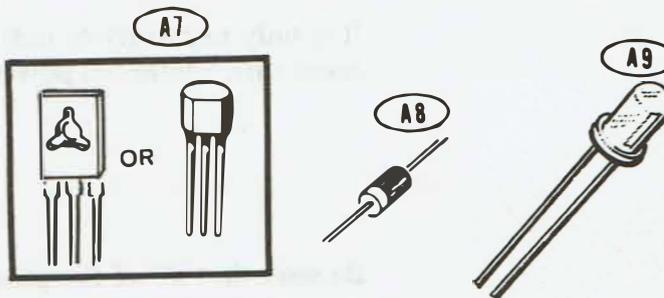
CAPACITORS

A4	21-192	1	.1μF, 50V ceramic
A4	21-717	1	.01μF, 50V ceramic
A5	25-892	1	470μF electrolytic
A5	25-900	1	1μF, 50V electrolytic
A5	25-868	3	47μF, 50V electrolytic
A5	25-870	2	100μF, 50V electrolytic
A5	25-881	3	10μF, 63V electrolytic
A6	27-77	1	.1μF, 50V Mylar*



TRANSISTORS — DIODE — LED

A7	417-291	2	2N5458
A7	417-801	3	MPSA20
A7	417-818	1	MJE181
A7	417-874	1	2N3906
A7	417-875	2	2N3904
A8	57-65	2	1N4002
A9	412-640	2	Light Emitting Diode (LED)



INTEGRATED CIRCUIT

A10	442-22	1	741 op amp
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MISCELLANEOUS

344-59	13'	#22 white solid wire
266-962	1	5-compartment container
51-97	1	Transformer
401-163	1	Speaker

* DuPont Registered Trademark

IMPORTANT NOTICE

Newer Heathkit Electronic Design Experimenters use a 3-terminal power plug rather than the conventional 2-terminal power plug. If you are using one of these newer Trainers, and your test equipment (oscilloscope, voltmeter, etc.) also uses a 3-terminal power plug, install a 3-wire to 2-wire adapter on the Trainer power plug. This will keep you from blowing a fuse in your Trainer or obtaining invalid results from some of the experiments. These adapters are inexpensive and readily available at most stores.

It is only necessary to use this adapter when you are using test equipment with 3-terminal power connectors.

CAUTION

Be sure that all of the pieces of equipment used in your experiments are connected to the same power source.

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UNIT 1

BIPOLAR TRANSISTORS

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INTRODUCTION

Circuit components are classified as being either **passive** or **active**. Passive components cannot provide a power gain — active components can.

Some examples of passive components include resistors, capacitors, inductors, transformers, and diodes. Typical applications for passive components, discussed in Heathkit/Zenith Educational Systems **Passive Circuit Design** course EE-1001, include:

Coupling circuits	Clippers
Bypass circuits	Clampers
Rectifiers	Peak detectors
Smoothing filters	Voltage multipliers
High-pass filter	Low-pass filter
Differentiators	Integrators
Lead circuit	Lag circuit

The transistor is an active device. Consequently, transistors can be used to provide a power gain. In addition, the transistor can provide a voltage and/or current gain, and function as an electronic switch. For these reasons, the transistor is a very versatile device.

In this unit, you will begin your study of transistor circuit design by first reviewing the characteristics of PN junction diodes. This approach is desirable since bipolar transistors can be modeled as two back-to-back diodes. We will also discuss the major characteristics and parameters of bipolar transistors.

In this unit, the terms “bipolar transistor”, BJT, and “transistor” refer to the same device.

UNIT OBJECTIVES

When you have completed this unit, you should be able to:

1. Estimate the large-signal forward resistance of a semiconductor diode.
2. Estimate the bulk, junction, and small-signal AC resistance of a semiconductor diode.
3. Sketch the DC and AC equivalent circuits for a diode simultaneously driven from a large DC source, and a small AC source.
4. Sketch the DC and AC load lines for a simple diode circuit.
5. Describe the basic structure of BJTs.
6. Identify the three BJT circuit configurations.
7. Define the following BJT parameters: α , B , I_{CBO} , I_{CEO} , BV_{BCO} , BV_{CEO} , and V_{BE} .
8. Determine when the effects of I_{CBO} can be ignored.
9. Sketch two equivalent BJT DC models.

UNIT ACTIVITY GUIDE

- Read section on "Diode Approximation".
- Answer Self-Test Review Questions 1-10.
- Read section on "Bipolar Transistor".
- Answer Self-Test Review Questions 11-20.
- Perform Experiment 1 in Unit 9.
- Study Summary.
- Complete Experiment 1, Unit 9.
- Complete Unit Examination.
- Check Examination Answers.

DIODE APPROXIMATIONS

The transistor is a 3-terminal, solid-state amplifying device. There are two fundamental transistor types: bipolar junction transistors (BJTs) and field-effect transistors (FETs).

In this unit on BJTs, the transistor will be examined from the point of view of a circuit element. Therefore, the physics of the transistor will not be discussed in any detail. If you are interested in a discussion of appropriate solid-state physics, refer to the Heathkit/Zenith Educational Systems **Semiconductor Devices** course, EE-3103A.

A transistor can be modeled as two back-to-back diodes. For this reason, we will begin our discussion of transistors by considering large-signal and small-signal diode approximations.

Large-Signal Diode Approximation

The junction diode is formed by joining P-type and N-type semiconductors as shown in Figure 1-1A. The schematic symbol and IV curve for a typical junction diode are illustrated in Figure 1-1B and Figure 1-1C respectively.

In Figure 1-1C, note the models used to represent the diode in the various regions of the curve. From your knowledge of passive circuit design, you should recall the following important points:

1. V_T = diode's turn-on voltage. Typically, $V_T = 0.3V$ for germanium diodes, and $0.7V$ for silicon diodes.
2. r_F = diode's forward resistance. Since manufacturers list the forward diode current, I_F , at a specified forward voltage, V_F , you can estimate r_F from:

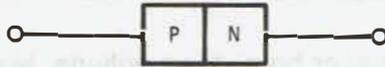
$$r_F = \frac{V_F - V_T}{I_F} \quad (\text{Eq. 1-1})$$

3. R_R = diode's reverse resistance. For values of reverse voltage, V_R , less than the diodes zener voltage, V_Z , you can estimate R_R from:

$$R_R = \frac{V_R}{I_R} \quad (\text{Eq. 1-2})$$

where: I_R = reverse diode current.

(A)



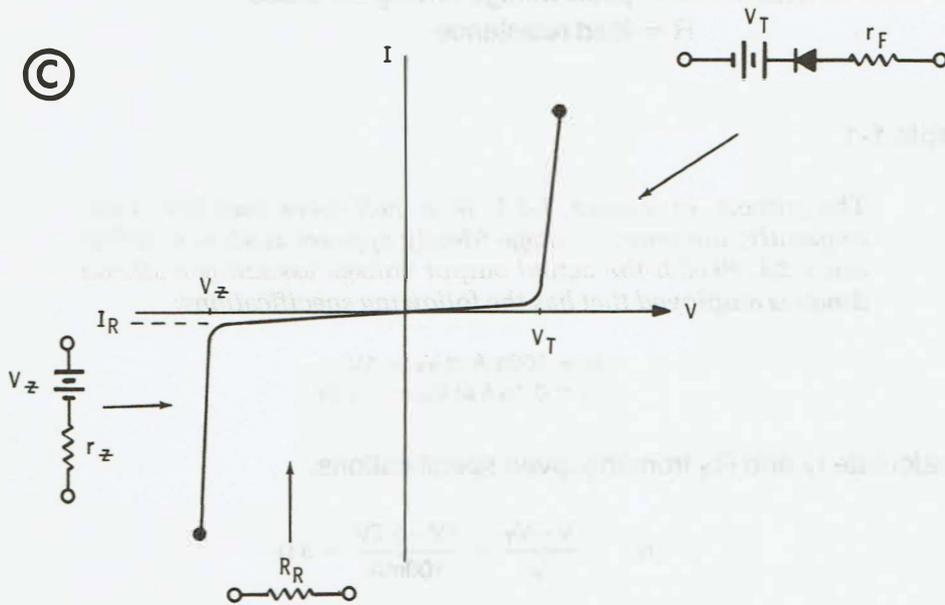
JUNCTION DIODE

(B)



SYMBOL

(C)



IV CURVE

Figure 1-1

The PN junction diode

- A. Junction diode
- B. Symbol
- C. IV curve

Incidentally, both V_T and I_R are temperature sensitive. As a rough guide:

V_T decreases by approximately 2.4mV for each °C increase in temperature. I_R doubles for each 10°C increase in temperature.

4. V_Z = diode's zener or breakdown voltage. Normally, general-purpose and rectifier diodes are not operated in the zener region. Diodes specifically designed to operate in the zener region are called zener diodes. Manufacturers list the values of zener voltage and zener resistance, r_Z , on the specification sheet for the zener diode.

When diode circuits are designed, component values should be chosen to mask out the nonideal effects due to V_T , r_F , and R_R . As a guide, component values are selected so that:

$$\begin{aligned} V &\geq 20V_T \\ R &\geq 20r_F \\ R &\leq \frac{R_R}{20} \end{aligned}$$

Where: V = peak voltage driving the diode

R = load resistance

Example 1-1

The circuit in Figure 1-2A is a half-wave rectifier. Consequently, the output voltage ideally appears as shown in Figure 1-2B. Sketch the actual output voltage assuming a silicon diode is employed that has the following specifications:

$$\begin{aligned} I_F &= 100\text{mA at } V_F = 1\text{V} \\ I_R &= 0.1\mu\text{A at } V_R = -20\text{V} \end{aligned}$$

First calculate r_F and R_R from the given specifications.

$$r_F = \frac{V - V_T}{I_F} = \frac{1\text{V} - 0.7\text{V}}{100\text{mA}} = 3\Omega$$

$$R_R = \frac{V_R}{I_R} = \frac{20\text{V}}{0.1\mu\text{A}} = 200\text{M}\Omega$$

When the diode is forward biased, the peak current equals:

$$I_m = \frac{V_m - V_T}{r_F + R} = \frac{20\text{V} - 0.7\text{V}}{3\Omega + 1\text{M}\Omega} \approx 19.3\mu\text{A}$$

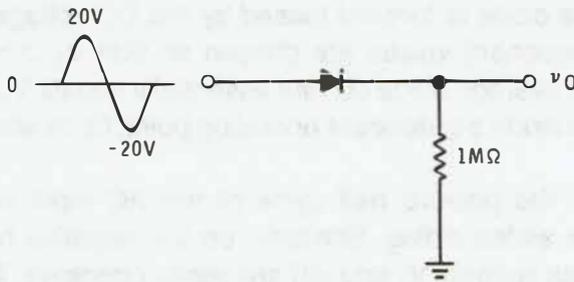
Thus, the peak output voltage is $19.3\mu\text{A} (1\text{M}\Omega)$ or 19.3V .

When the diode is reverse biased, the input voltage divides between R_R and R . Thus, the peak output voltage is:

$$v_{om} = \frac{-20\text{V} (1\text{M}\Omega)}{200\text{M}\Omega + 1\text{M}\Omega} \approx -0.1\text{V}$$

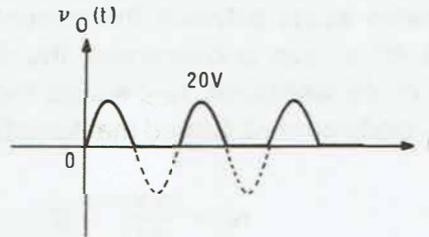
Figure 1-1C illustrates the actual output voltage. Since the component values satisfy the inequalities given previously the real diode is an excellent approximation of an ideal diode.

(A)



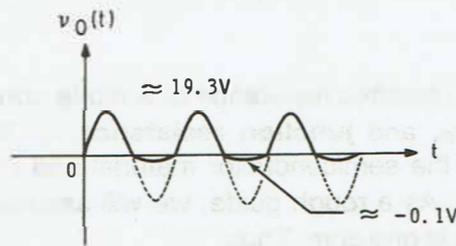
HALF-WAVE RECTIFIER

(B)



IDEAL OUTPUT VOLTAGE

(C)



ACTUAL OUTPUT VOLTAGE

Figure 1-2

Circuit and waveforms for Example 1-2

- A. Half-wave rectifier.
- B. Ideal output voltage
- C. Actual output voltage

Small-Signal Diode Approximations

The diode approximations introduced previously are referred to as DC, or large-signal, approximations. The term “large-signal” means that the DC or peak AC input voltage, as the case may be, is large compared to the diode’s turn-on voltage.

When the amplitude of the input voltage is on the same order of magnitude as, or less than, the diode’s turn-on voltage, you have small-signal operation. Especially important is the case where the diode is simultaneously driven from a large DC and small AC source as shown in Figure 1-3A. The following is a summary of the operation of the circuit in Figure 1-3A.

1. The diode is forward biased by the DC voltage source. Assuming component values are chosen so that $V_1 \gg V_T$ and $R \gg r_F$, the average diode current essentially equals V_1/R . This establishes the diode’s **quiescent** operating point, Q , as shown in Figure 1-3B.
2. On the positive half cycle of the AC input voltage, V_1 and $v(t)$ are series aiding. Similarly, on the negative half cycle of the AC input voltage, V_1 and $v(t)$ are series opposing. Thus, the AC source results in a diode current that varies between points 1 and 2, above and below the quiescent value, Q , as shown in Figure 1-3B.

In Figure 1-3B, note that for small changes in diode current, around the Q point, a linear relationship exists between the current and voltage. Consequently, as far as the small AC source is concerned, the diode acts like a resistance. This **AC** or **dynamic** diode resistance, r_{AC} , equals the change in diode voltage divided by the change in diode current. Stated mathematically:

$$r_{AC} = \frac{\Delta V}{\Delta I} \quad (\text{Eq. 1-3})$$

Since the graphic method suggested by Figure 1-3B and equation 1-3 is tedious, we will introduce several approximate formulas that can be used to estimate r_{AC} .

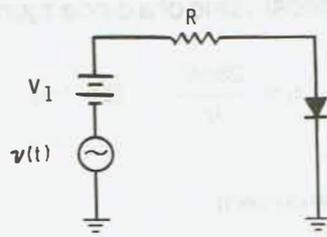
To begin, the dynamic resistance of a diode consists of two components — **bulk resistance**, r_B , and **junction resistance**, r_j . The bulk resistance includes the resistance of the semiconductor material and the contact resistance of the connecting leads. As a rough guide, we will assume the bulk resistance of a typical junction diode is one ohm. Thus:

$$r_B \approx 1\Omega \quad (\text{Eq. 1-4})$$

(A)

(LARGE DC)

(SMALL AC)



CIRCUIT

(B)

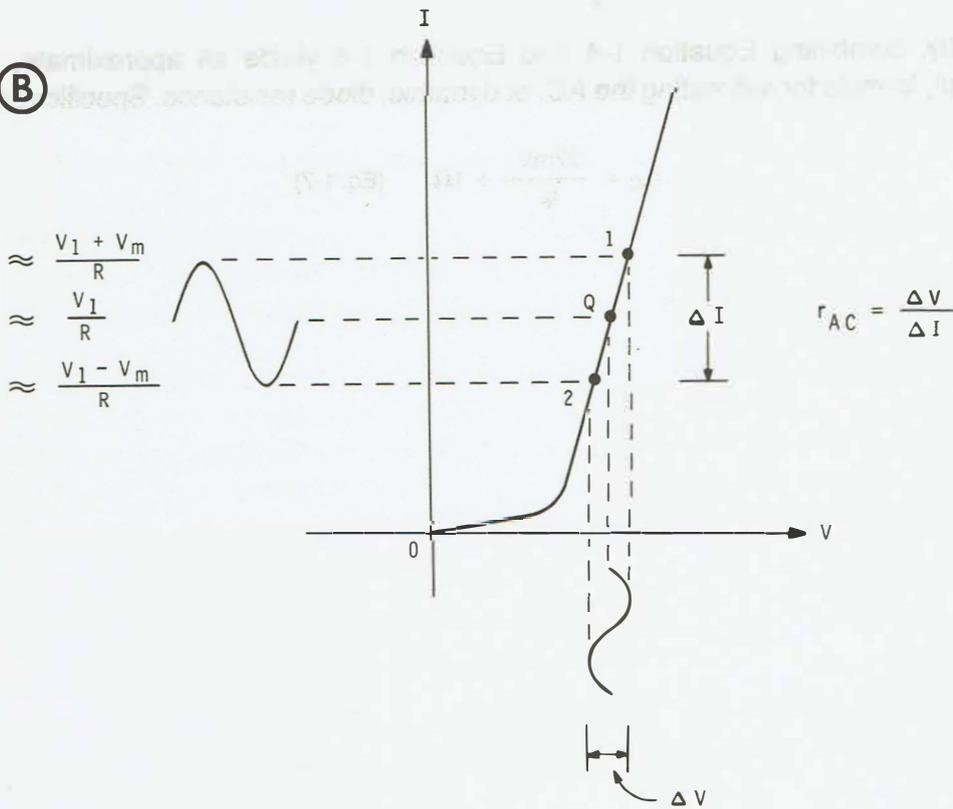


Figure 1-3

The concept of AC, dynamic, diode resistance

- A. Circuit
- B. IV curve

As the name implies, the junction resistance is the effective resistance of the PN junction. The value of the junction resistance depends upon the amount of forward DC diode current. The theoretical value of a diode's junction resistance is given by:

$$r_j = \frac{26\text{mV}}{I_F} \quad (\text{Eq. 1-5})$$

Where I_F = forward DC diode current.

In practice, the actual value of r_j typically varies over a 2:1 range from $26\text{mV}/I_F$ to $52\text{mV}/I_F$. Thus, for purpose of analysis and design, we will use the following "compromise formula" to calculate r_j :

$$r_j = \frac{37\text{mV}}{I_F} \quad (\text{Eq. 1-6})$$

Finally, combining Equation 1-4 and Equation 1-6 yields an approximate, but useful, formula for estimating the AC, or dynamic, diode resistance. Specifically:

$$r_{AC} = \frac{37\text{mV}}{I_F} + 1\Omega \quad (\text{Eq. 1-7})$$

Example 1-2

Estimate the AC resistance of a semiconductor diode for the following values of forward DC current. 1mA, 14mA, and 200mA.

When $I_F = 1\text{mA}$, the diode's junction resistance is:

$$r_j = \frac{37\text{mV}}{I_F} = \frac{37\text{mV}}{1\text{mA}} = 37\Omega$$

Assuming the diode's bulk resistance is 1Ω , the AC diode resistance is:

$$r_{AC} = r_B + r_j = 1\Omega + 37\Omega = 38\Omega$$

The result of similar calculations for $I_F = 14\text{mA}$ and 200mA are summarized in Table 1-1.

I_F	r_j	r_B	r_{AC}
1mA	37Ω	1Ω	38Ω
14mA	2.64Ω	1Ω	3.64Ω
200mA	0.185Ω	1Ω	1.185Ω

TABLE 1-1

Summary Of Calculations For Example 1-2

Note in Table 1-1 that, for small forward currents, the AC diode resistance approximately equals the junction resistance similarly, for large forward currents, the AC diode resistance approximately equals the bulk resistance.

DC and AC Equivalent Circuits

You can analyze multi-source circuits with the superposition theorem. Recall from your study of basic circuit analysis, that, when you apply the superposition theorem, you must consider the effect of each source “acting alone”. Also recall that the actual response equals the algebraic sum of the responses produced by each source acting alone.

When you apply the superposition theorem to diode and transistor circuits, you must also consider the effects of coupling and bypass capacitors. Therefore, we will use the following procedures to obtain the DC and AC equivalent circuits.

DC EQUIVALENT CIRCUITS

1. Replace coupling and bypass capacitors by open circuits.
2. Reduce AC sources to zero.
3. Replace the diode by its large-signal model.

AC EQUIVALENT CIRCUIT

1. Replace coupling and bypass capacitors by short circuits.
2. Reduce DC sources to zero.
3. Replace the diode by its AC, dynamic, resistance.

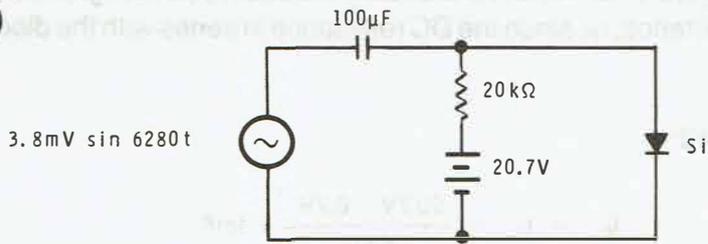
Once you have the DC and AC equivalent circuits, you can determine the appropriate DC and AC responses. Naturally, the actual response equals the algebraic sum of the DC and AC responses.

Example 1-3

For the circuit shown in Figure 1-4A.

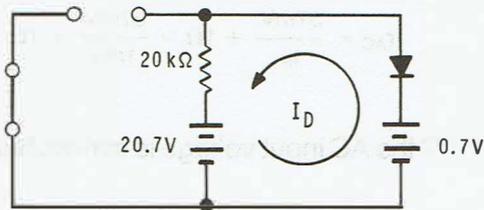
- (a) *Sketch the DC equivalent circuit.*
- (b) *Calculate the DC diode current and voltage.*
- (c) *Sketch the AC equivalent circuit.*
- (d) *Calculate the AC diode current and voltage.*
- (e) *Sketch the actual diode current and voltage.*

A



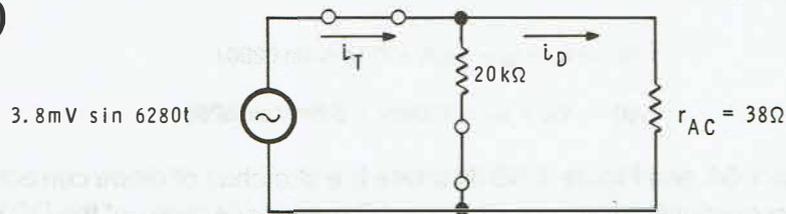
ORIGINAL CIRCUIT

B



DC EQUIVALENT CIRCUIT

C



AC EQUIVALENT CIRCUIT

Figure 1-4

- Circuits for Example 1-3
 A. Original circuit
 B. DC equivalent circuit
 C. AC equivalent circuit.

- (a) To obtain the DC equivalent circuit you open the coupling capacitor, reduce the AC source to zero and replace the diode by its large-signal model as shown in Figure 1-4B. Here, as is usually the case, you can ignore the diode's forward resistance, r_F , since the DC resistance in series with the diode is quite large.
- (b) In Figure 1-4B:

$$I_D = I_F = \frac{20.7V - 0.7V}{20k\Omega} = 1mA$$

$$V_D = V_T = 0.7V = 700mV$$

- (c) To obtain the AC equivalent circuit you short the coupling capacitor, reduce the DC source to zero and replace the diode by its dynamic resistance, r_{AC} , as shown in Figure 1-4C. The value of r_{AC} is estimated as follows:

$$r_{AC} = \frac{37mV}{I_F} + 1\Omega = \frac{37mV}{1mA} + 1\Omega = 38\Omega$$

- (d) In Figure 1-4C the AC input voltage is connected directly across r_{AC} . Thus:

$$v_D = 3.8mV \text{ peak}$$

$$i_D = \frac{3.8mV}{38\Omega} = 0.1mA \text{ peak}$$

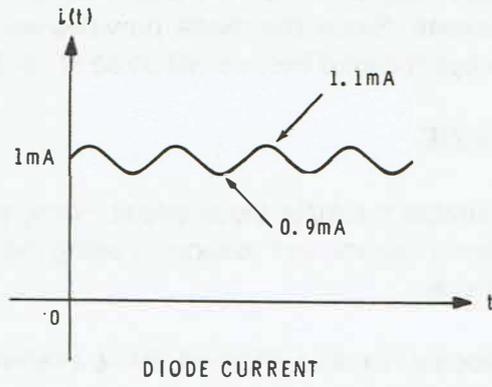
- (e) The actual responses equal the algebraic sum of the DC and AC responses. Therefore:

$$i(t) = I_D + i_D = 1mA + 0.1mA \sin 6280 t$$

$$v(t) = V_D + v_D = 700mV + 3.8mV \sin 6280 t$$

Figure 1-5A and Figure 1-5B illustrate the sketches of diode current and voltage respectively. Here, note that the AC responses "ride on" the DC levels.

(A)



(B)

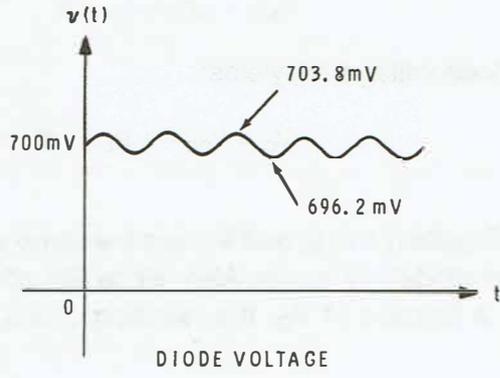


Figure 1-5

Sketches of diode current and voltage for Example 1-3.

- A. Diode current.
- B. Diode voltage.

Load Lines

Graphic methods, using load lines, are especially useful for analyzing and designing transistor circuits. Since the diode provides an excellent opportunity to introduce the concept of a load line, we will do so at this time.

THE DC LOAD LINE

Figure 1-6A illustrates a simple diode circuit. Here, you can obtain **approximate** values for the diode current and voltage by using the large-signal approximations discussed previously.

Assuming the diode's IV curve, Figure 1-6B, is available, it is possible theoretically to obtain **exact** values of the diode current and voltage. For an illustration of the method, consider the loop equation for the circuit in Figure 1-6A. Here:

$$V_{CC} - I_D R_L - V_D = 0$$

Solving for the diode voltage, V_D yields:

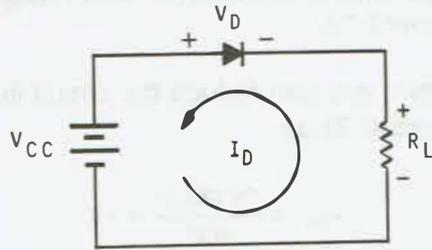
$$V_D = V_{CC} - I_D R_L \quad (\text{Eq. 1-8})$$

The variables in Equation 1-8, I_D and V_D , are the same variables that are displayed graphically by the diode's IV curve. Also, since Equation 1-8 is a linear equation if I is plotted as a function of V_D , the resulting graph, called the **DC load line**, is a straight line.

Recall that you can solve two simultaneous relationships in two unknowns by determining the point of intersection of their graphs. Consequently, for a particular value of V_{CC} and R_L , the diode current and voltage correspond to the point of intersection between the DC load line and the diodes IV curve as shown in Figure 1-6C. Here, you should note the following:

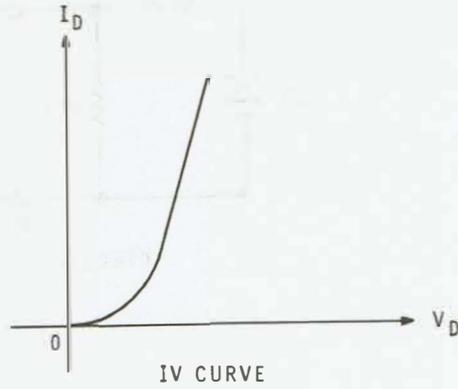
1. The vertical intercept of the DC load line equals V_{CC}/R_L .
2. The horizontal intercept of the DC load line equals V_{CC} .
3. The point of intersection of the DC load line and the diode's IV curve is called the Q, quiescent, point. The values of current and voltage at the Q point, I_{DQ} and V_{DQ} , are the theoretically exact values of the diode current and voltage.
4. The slope of the DC load line equals $-1/R_L$.

(A)



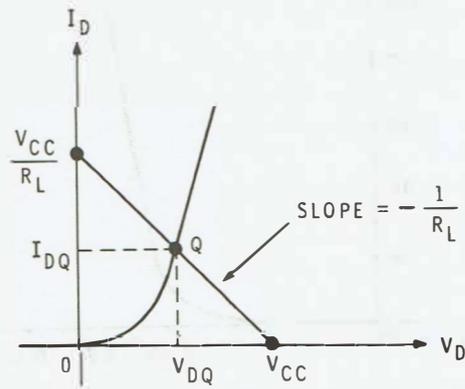
DIODE CIRCUIT

(B)



IV CURVE

(C)



PLOTTING THE DC LOAD LINE

Figure 1-6

The DC load line

- A. Diode circuit
- B. IV curve
- C. Plotting the DC load line.

Example 1-4

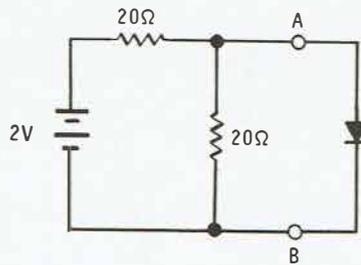
Work out the values of diode current and voltage for the circuit shown in Figure 1-7A.

With Thevenin's Theorem, you can reduce the circuit in Figure 1-7A to a simpler single-loop equivalent circuit. Thus:

$$V_{TH} = \frac{2V(20\Omega)}{40\Omega} = 1V$$

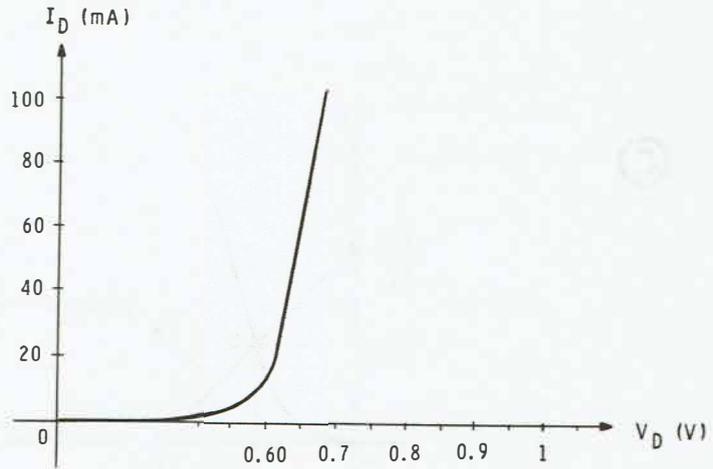
$$R_{TH} = 20\Omega || 20\Omega = 10\Omega$$

(A)



CIRCUIT

(B)



DIODE IV CURVE

Figure 1-7

Circuit and IV curve for Example 1-4.

- A. Circuit
- B. Diodes IV curve

The resulting Thevenin equivalent circuit is shown in Figure 1-8A. From this equivalent circuit, the intercept values of the DC load line are calculated as follows:

$$I = \frac{1V}{10\Omega} = 100\text{mA} \quad (\text{vertical intercept})$$

$$V = V_{TH} = 1V \quad (\text{horizontal intercept})$$

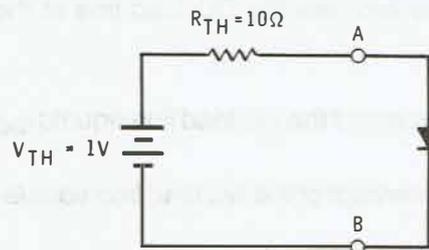
Next, you plot the DC load line on the diode's IV curve to determine the Q point values as shown in Figure 1-8B. Here:

$$I_{DQ} = 50\text{mA}$$

$$V_{DQ} = 0.64V$$

I_{DQ} and V_{DQ} are the actual values of diode current and voltage respectively for the circuit in Figure 1-7A.

(A)



THEVENIN EQUIVALENT CIRCUIT

(B)

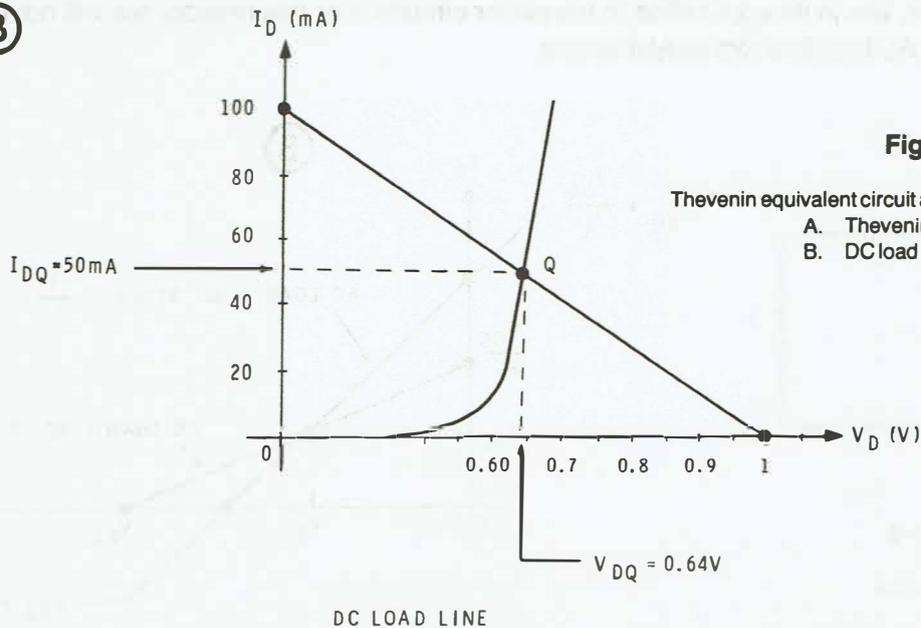


Figure 1-8

Thevenin equivalent circuit and DC load line for Example 1-4.

- A. Thevenin equivalent circuit
- B. DC load line.

THE AC LOAD LINE

Figure 1-9A illustrates a diode circuit driven from a large DC, V_{CC} , and small AC, $v(t)$ source. Here, the value of capacitor C is chosen so that the capacitor provides good coupling at the frequency of the AC source. For this reason, the capacitor is effectively an AC short. Consequently, the AC load resistance as seen from the diode is:

$$r_L = R_L \parallel R$$

Since the capacitor acts like an open circuit for DC signals, the DC load resistance as seen from the diode is simply R_L . For this reason, the DC load line and Q point values are calculated as illustrated previously.

By extending the DC load line concept, you can construct an AC load line as shown in Figure 1-9B. Here, you should note the following:

1. The AC load line crosses the DC load line at the Q point, and has a slope of $-1/r_L$.
2. The vertical intercept of the AC load line equals $I_{DQ} + V_{DQ}/r_L$.
3. The horizontal intercept of the AC load line equals $V_{DQ} + I_{DQ} r_L$.

The DC load line enables you to obtain a graphic solution for the DC diode current, I_{DQ} , and DC diode voltage, V_{DQ} . Similarly, the AC load line can be used to graphically determine the AC diode current. Our principle interest in the AC load line, however, lies in its application to transistor circuits. For this reason, we will not discuss the AC load line further at this time.

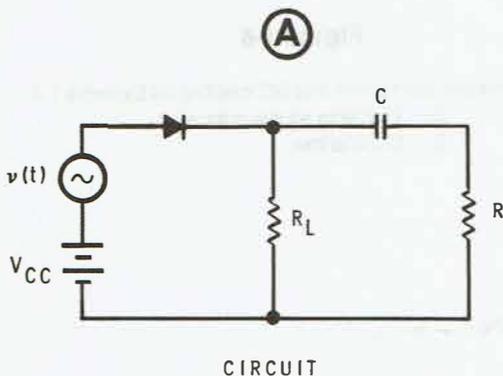
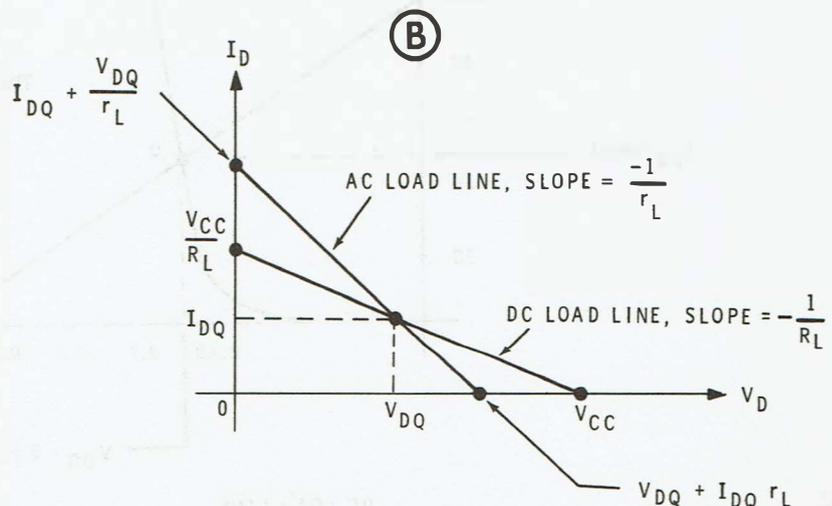


Figure 1-9

The AC load line

- A. Circuit.
- B. Plotting the DC and AC load lines.



Self-Test Review

1. In AC equivalent circuits, coupling and bypass capacitors are replaced by _____ circuits.
2. In DC equivalent circuits, coupling and bypass capacitors are replaced by _____ circuits.
3. A diode driven from a large DC and small AC source acts like a _____ to the AC source.
4. As a rough guide, the bulk resistance of a semiconductor diode is approximately _____ ohm.
5. The junction resistance of a semiconductor diode depends on the diode's forward _____ current.
6. The junction resistance of a semiconductor diode typically varies over a _____ range from the theoretical value.
7. For any value of I_F , $r_{AC} = \text{_____} + \text{_____}$.
8. The point of intersection of the DC load line and a diode's IV curve establishes the _____ point.
9. The AC load line has a slope of - _____.
10. The DC load line has a slope of - _____.

Answers

- | | |
|---------------|--|
| 1. Short | 6. 2:1 |
| 2. Open | 7. $r_B + r_j$ |
| 3. Resistance | 8. Q or quiescent |
| 4. One | 9. $1/r_L$, where r_L is the AC load resistance. |
| 5. DC | 10. $1/R_L$, where R_L is the DC load resistance. |

BIPOLAR TRANSISTORS

In this section, you will examine the structure, input and output characteristics, and selected parameters for bipolar transistors. In addition, appropriate models will be introduced that are used to analyze and design transistor circuits.

Structure

Bipolar junction transistors, BJTs, consist of NPN or PNP “semiconductor sandwiches” as shown in Figure 1-10A. Note that leads are affixed to each of the three semiconductor regions. These regions are called the emitter, E, base, B, and collector, C, respectively. The boundary between P-type and N-type semiconductor materials is referred to as a junction. Consequently, BJTs are 2-junction, 3-terminal devices.

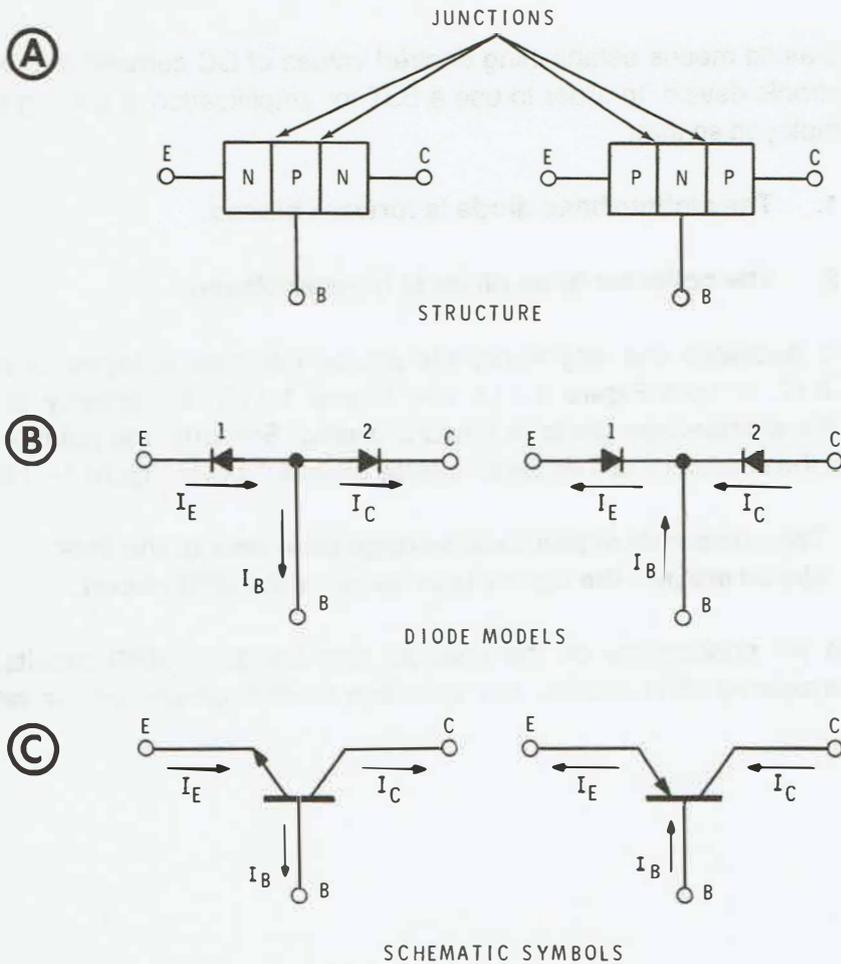


Figure 1-10

The two types of bipolar transistors - NPN and PNP.

- A. Structure
- B. Diode models
- C. Schematic Symbols

Recall that a junction diode is formed by joining P-type and N-type semiconductor materials as illustrated previously in Figure 1-1A. Consequently, BJTs can be modeled by two back-to-back diodes as shown in Figure 1-10B.

Here, diode number 1 is called the emitter-base diode, while diode number 2 is referred to as the collector-base diode.

The schematic symbols for both NPN and PNP BJTs are shown in Figure 1-10C. Notice that the only difference between the NPN and PNP symbols is the direction of the arrow, which indicates the emitter of the device. Specifically, the arrow points away from the base in the NPN symbol and toward the base in the PNP symbol. In Figure 1-10B and Figure 1-10C, note that the current directions in the PNP transistor are just the opposite of those in the NPN transistor.

Biasing BJTs

The term biasing means establishing desired values of DC currents and voltages for an electronic device. In order to use a BJT for amplification, a biasing scheme must be employed so that:

1. **The emitter-base diode is forward biased.**
2. **The collector-base diode is reverse biased.**

Figure 1-11 illustrates one way to provide appropriate bias voltages for an NPN and PNP BJT. In both Figure 1-11A and Figure 1-11B, the polarity of V_{EE} is such that the emitter-base diode is forward biased. Similarly, the polarity of V_{CC} is such that the collector-base diode is reverse biased. Note in Figure 1-11 that:

The current directions and voltage polarities of the PNP circuit are just the opposite of those in the NPN circuit.

Initially, we will concentrate on the analysis and design of NPN circuits. Once you have mastered NPN circuits, the transition to PNP circuits will be relatively easy.

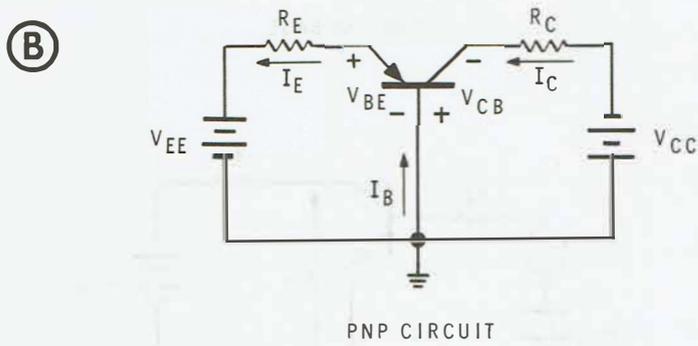
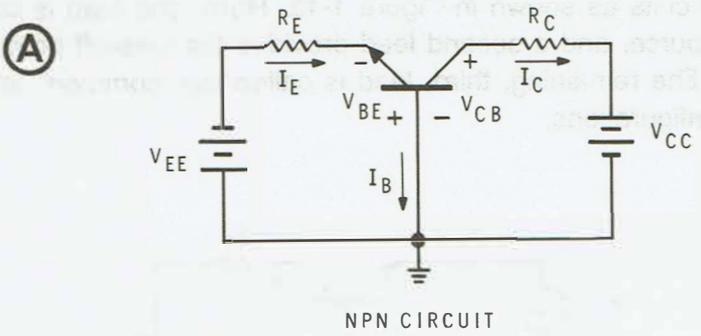


Figure 1-11

Property biased BJTs showing current directions and voltage polarities.
A. NPN circuit
B. PNP circuit.

BJT Circuit Configurations

Many BJT circuits can be classified as common-base, common-emitter, or common-collector circuits as shown in Figure 1-12. Here, one lead is connected to the AC signal source, and a second lead provides the take-off point for the AC output voltage. The remaining, third, lead is called the “common” and identifies the particular configurations.

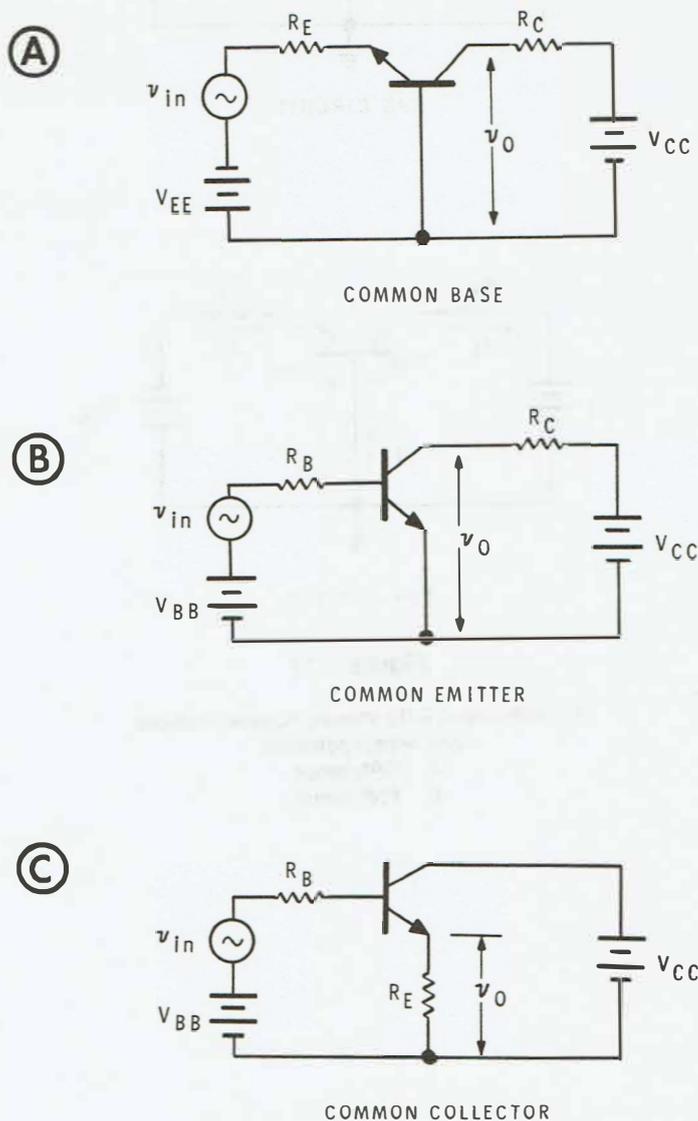


Figure 1-12

Standard BJT circuit configurations.

- A. Common base.
- B. Common emitter.
- C. Common collector.

Naturally, each configuration has its unique characteristics. These characteristics, and appropriate analysis and design methods will be discussed in detail in later units.

Reverse Currents

For each configuration in Figure 1-12, V_{CC} reverse biases the collector-base diode of the BJT. Opening the emitter circuit of Figure 1-12A produces the circuit shown in Figure 1-13A. Here, the collector current is simply the reverse current of the collector-base diode. Manufacturers list this reverse current as I_{CBO} on the transistor's data sheet. Note that current flows between the BJT terminals identified by subscripts C and B. Similarly, the O subscript indicates that the emitter terminal is open.

If you open the base circuit in Figure 1-12B you obtain the circuit shown in Figure 1-13B. Here, the collector current once again equals the reverse current of the collector-base diode. In this case, however, the reverse current is designated as I_{CEO} since the base terminal is open.

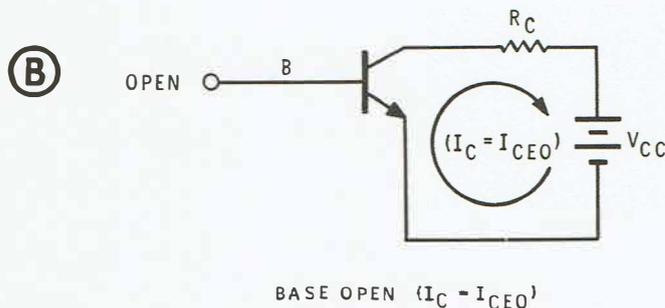
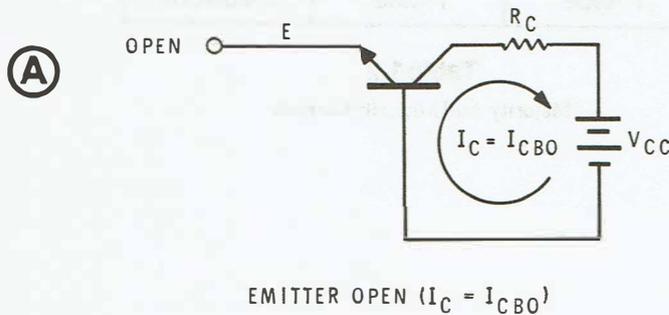


Figure 1-13

Reverse BJT currents

- A. Emitter open ($I_C = I_{CBO}$)
- B. Base open ($I_C = I_{CEO}$)

Basic Transistor Action

N-type material is rich in negative charge carriers (electrons) and P-type material is rich in positive charge carriers (holes). Consequently, electrons and holes are referred to as **majority carriers** in N-type and P-type materials respectively.

Since it is not possible to manufacture perfect semiconductor materials, N-type materials contain a small number of holes, and P-type materials contain a small number of free electrons. The electrons in the P-type material and the holes in the N-type materials are called **minority carriers**. Table 1-2 summarizes the concept of majority and minority carriers for N-type and P-type materials.

Material	Majority Carriers	Minority Carriers
N-type	Electrons	Holes
P-type	Holes	Electrons

Table 1-2

Majority And Minority Carriers

When a PN junction is said to be forward or reverse biased, it is important to realize that the forward or reverse biased condition applies only to the majority carriers. From the point of view of the minority carriers, the situation is the opposite. Specifically:

1. A forward biased PN junction is reverse biased with respect to minority carriers.
2. A reverse biased PN junction is forward biased with respect to minority carriers.

To illustrate statement 2 above, consider the circuit shown in Figure 1-14. Here, the PN junction is reverse biased by the external voltage source, V_{CC} . Consequently, majority carriers are prevented from crossing the junction. Note however, that the polarity of V_{CC} is such that the minority carriers are forced across the junction. For this reason, a small reverse current, I_R , flows in the circuit.

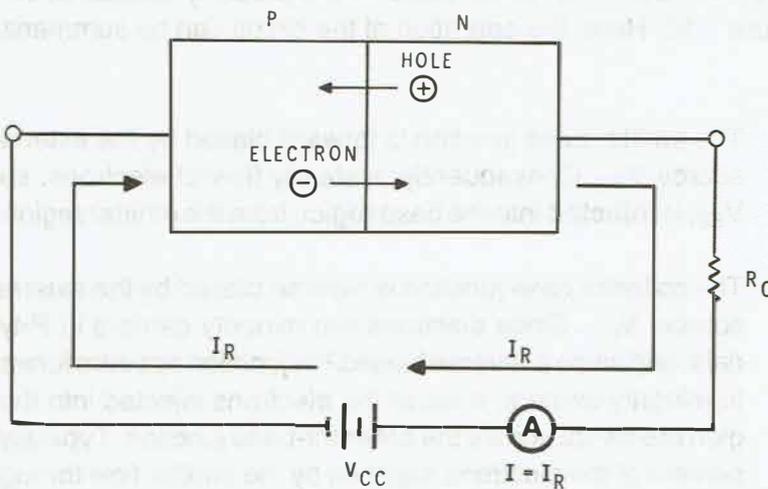


Figure 1-14

The movement of minority carriers across a reverse biased PN junction results in a small reverse current, I_R .

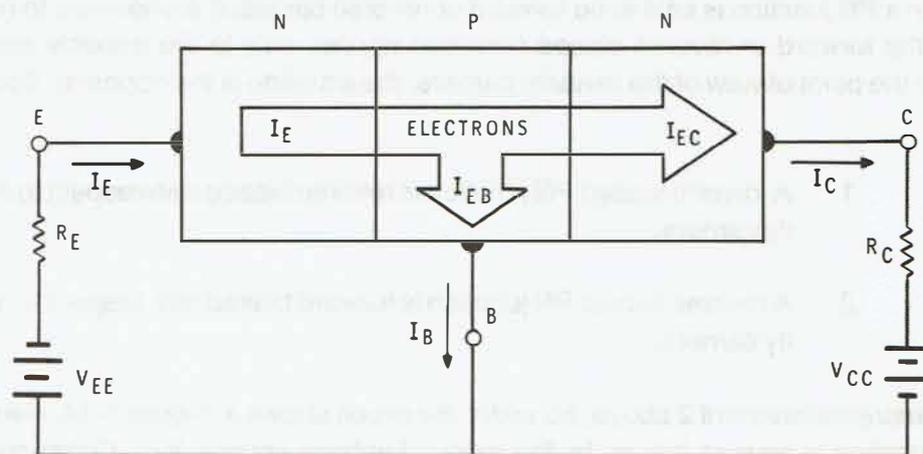


Figure 1-15

Basic transistor action for a NPN transistor in the common base configuration.

Let's examine the action that takes place in the properly biased NPN transistor shown in Figure 1-15. Here, the operation of the circuit can be summarized as follows:

1. The emitter base junction is forward biased by the external voltage source V_{EE} . Consequently, a steady flow of electrons, supplied by V_{EE} , is **injected** into the base region from the emitter region.
2. The collector base junction is reverse biased by the external voltage source, V_{CC} . Since electrons are minority carriers in P-type materials, and since a reverse biased PN junction appears forward biased to minority carriers, most of the electrons injected into the base region are swept across the collector-base junction. Typically, 95 to 99 percent of the electrons supplied by the emitter flow through the collector region and into the external voltage source, V_{CC} . The remaining 1 to 5 percent of the injected electrons combine with holes in the base region. This establishes a small base current which flows out of the base region and into the external circuit.

In order for the action just described to occur, the various regions of the BJT must be specially constructed. Specifically:

1. The emitter region contains large numbers of majority carriers. This ensures that a large number of electrons will be supplied to the base region.

2. The base region is very thin and contains relatively few majority carriers. This is necessary to minimize the combining of holes and injected electrons in the base region.
3. The collector region contains moderate numbers of majority carriers, and is physically larger than either the base or emitter regions. This ensures adequate "collection" of the electrons swept across the collector-base junction.

Although it is quite useful to model a BJT as two back-to-back diodes, the transistor action described previously does not occur if two discrete semiconductor diodes are placed back to back. This is because the P-type and N-type regions of semiconductor diodes do not satisfy the special requirements necessary for proper BJT operation.

BJT Formulas

At this point, we will introduce a number of formulas that are useful for the analysis and design of BJT circuits. In addition, we will use approximations in order to simplify the formulas as much as possible. With reference to Figure 1-15 then:

The algebraic sum of the currents entering and leaving the BJT must equal zero. Therefore:

$$I_E = I_B + I_C \quad (\text{Eq. 1-9})$$

Where: I_E , I_B , and I_C are the DC currents in amperes, A, in the emitter, base, and collector leads respectively.

In Figure 1-15, it is clear that internally, I_E supplies current to both the base and collector regions. The ratio of I_{EC} to I_E is called alpha, α , and indicates the portion of the emitter current, I_E , that enters the collector region. Stated mathematically:

$$\alpha = \frac{I_{EC}}{I_E}$$

Also, since $I_{EC} = I_C - I_{CBO}$, α , may be defined as:

$$\alpha = \frac{I_C - I_{CBO}}{I_E} \quad (\text{Eq. 1-10})$$

Where: I_C and I_E are as defined previously,
 I_{CBO} = reverse current in amperes, A, of the collector-base diode.

Since $I_C = I_{EC} + I_{CBO}$, and $I_{EC} = \alpha I_E$:

$$I_C = \alpha I_E + I_{CBO} \quad (\text{Eq. 1-11})$$

In Figure 1-15, note that $I_B = I_E - I_{EC} - I_{CBO}$. Substituting αI_E for I_{EC} yields:

$$I_B = I_E - \alpha I_E - I_{CBO}$$

$$I_B = I_E(1 - \alpha) - I_{CBO} \quad (\text{Eq. 1-12})$$

The ratio of I_{EC} to I_{EB} is defined as beta, B. Substituting $I_C - I_{CBO}$ for I_{EC} , and $I_B + I_{CBO}$ for I_{EB} yields:

$$B = \frac{I_C - I_{CBO}}{I_B + I_{CBO}} \quad (\text{Eq. 1-13})$$

Solving Equation 1-13 for the collector current, I_C , yields:

$$I_C - I_{CBO} = B I_B + B I_{CBO}$$

$$I_C = B I_B + B I_{CBO} + I_{CBO}$$

$$I_C = B I_B + I_{CBO}(B + 1) \quad (\text{Eq. 1-14})$$

Occasionally the following identities will also prove useful:

$$\alpha = \frac{B}{B + 1} \quad (\text{Eq. 1-15})$$

$$1 - \alpha = \frac{1}{B + 1} \quad (\text{Eq. 1-17})$$

$$B = \frac{\alpha}{1 - \alpha} \quad (\text{Eq. 1-16})$$

$$I_{CEO} = (B + 1) I_{CBO} \quad (\text{Eq. 1-18})$$

By using one or more of the previous identities, you can derive numerous equivalent relationships. For example, substituting Equation 1-17 into Equation 1-12 yields:

$$I_B = \frac{I_E}{B + 1} - I_{CBO} \quad (\text{Eq. 1-19})$$

If you examine typical BJT data sheets, you will find the following important facts:

1. Values of α typically range from 0.95 to 0.99.
2. B rarely has a value less than 20.
3. I_{CBO} is small compared to I_C for **silicon** transistors.
4. $(B + 1) I_{CBO}$ is small compared to $B I_B$ in most circuits that use **silicon** transistors.

Based upon the previous observations, the following approximations are frequently employed.

$$\alpha \approx 1$$

$$B + 1 \approx B$$

$$I_{CBO} \approx 0$$

By using one or more of these approximations, we can simplify most of the formulas given previously. Table 1-3 summarizes the original and resulting approximate formulas.

Original Formula	Approximate Formula
$\alpha = \frac{I_C - I_{CBO}}{I_E}$	$\alpha = \frac{I_C}{I_E}$
$B = \frac{I_C - I_{CBO}}{I_B + I_{CBO}}$	$B = \frac{I_C}{I_B}$
$I_C = \alpha I_E + I_{CBO}$	$I_C = \alpha I_E$
$I_C = B I_B + I_{CBO} (B + 1)$ $I_C = B I_B + I_{CEO}$	$I_C = B I_B$
$I_B = \frac{I_E}{B + 1} - I_{CBO}$	$I_B = \frac{I_E}{B}$

TABLE 1-3
Approximate BJT formulas

In many cases, the approximate formulas in Table 1-3 are sufficiently accurate for the analysis and design of BJT circuits.

Example 1-5

A silicon BJT has a B of 100, and an I_{CBO} of $0.01\mu\text{A}$. Calculate the value of α , I_C and I_B assuming $I_E = 1\text{mA}$.

We will calculate the various quantities using both the original and approximate formulas.

$$\alpha = \frac{B}{B + 1} = \frac{100}{101} \approx 0.99$$

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = 0.99(1\text{mA}) + 0.01\mu\text{A}$$

$$I_C = 0.99001\text{mA}$$

$$I_B = \frac{I_E}{B + 1} - I_{CBO}$$

$$I_B = \frac{1\text{mA}}{101} - 0.01\mu\text{A}$$

$$I_B = 9.89\mu\text{A}$$

Now for the approximate formulas:

$$\alpha \approx 1 \quad \text{For this reason} \quad I_C \approx I_E = 1\text{mA}$$

$$I_B \approx \frac{I_E}{B} = \frac{1\text{mA}}{100} = 10\mu\text{A}$$

Clearly, the values predicted by the approximate formulas are very close to the values predicted by the original formulas. As a guide, you can use the approximate formulas if:

$$\frac{I_E}{BI_{CBO}} \geq 20 \quad (\text{Eq. 1-20})$$

Example 1-6

A germanium BJT has a B of 100 and an I_{CBO} of 1mA. Should you use the original or approximate formulas, if I_E is 1mA?

In this case:

$$\frac{I_E}{B I_{CBO}} = \frac{1\text{mA}}{100(1\mu\text{A})} = 10$$

Since 10 is not > 20 , you should use the original formulas. Generally speaking, germanium transistors have large values of I_{CBO} compared to silicon transistors.

BJT DC Parameters

The data sheet of a particular BJT provides minimum, typical and/or maximum values for a number of BJT parameters. In this course, appropriate parameters will be introduced as required. In this section, we will briefly discuss the most important DC parameters.

MAXIMUM RATINGS

Like any electrical device, BJTs will be damaged or destroyed if the current, voltage or power is excessive. Consequently, you should never exceed the maximum ratings, usually specified at 25°C. Above 25°C, you should use appropriate derating factors to determine the maximum rating at the elevated temperature as illustrated by the following example.

Example 1-7

For a certain transistor, the following information is provided under the Maximum Ratings portion of the data sheet.

<i>Maximum Ratings</i>	<i>Symbol</i>	<i>Value</i>	<i>Unit</i>
<i>Total Power Dissipation @ 25°C</i>	P_D	2	Watt
<i>Derate Above 25°C</i>	D	20	mW/°C

What is the maximum power the transistor can dissipate at 50°C?

The difference between 50°C and 25°C is obviously 25°C. Since the power must be derated by 20mW for each °C rise in temperature, we have:

$$P = P_{25^{\circ}\text{C}} - D\Delta T$$

$$P = 2\text{W} - \frac{20\text{mW}}{^{\circ}\text{C}} \cdot 25^{\circ}\text{C}$$

$$P = 2\text{W} - 0.5\text{W} = 1.5\text{W}$$

DC CURRENT GAIN

This is the parameter B introduced previously. Data sheets use the symbol h_{FE} to indicate the value of B . Typically, h_{FE} can vary by as much as 4:1 among transistors of the same type. In addition, for a given transistor, h_{FE} varies with temperature, emitter current, and time.

LEAKAGE CURRENTS

I_{CBO} , I_{CEO} , and I_{EBO} are the symbols used to represent the various leakage currents. Even though these currents are measured respectively with the emitter, base, and collector leads open, they can adversely affect the operation of a BJT circuit when the leads are not open.

Data sheets almost always list the maximum value of I_{CBO} . For transistors of the same type, I_{CBO} can vary by as much as 100:1. In addition, for a given transistor, I_{CBO} is sensitive to temperature changes. As a guide, I_{CBO} doubles for, approximately, every 8°C rise in temperature.

BASE-TO-EMITTER VOLTAGE

For a given value of emitter current, the base-to-emitter voltage varies linearly by approximately -2mV to -2.5mV per °C rise in temperature. Variations in V_{BE} in turn produce changes in the emitter and collector current.

Techniques for stabilizing BJT circuits against variations in h_{FE} , I_{CBO} , and V_{BE} will be discussed in Unit 2.

BJT Input and Output Curves

The circuit shown in Figure 1-16A can be used to obtain both input and output curves for an NPN transistor in the common-base configuration. To obtain input curves, you can use the following procedure:

1. Adjust R_2 to obtain a particular value of V_{CB} — for example 1V.

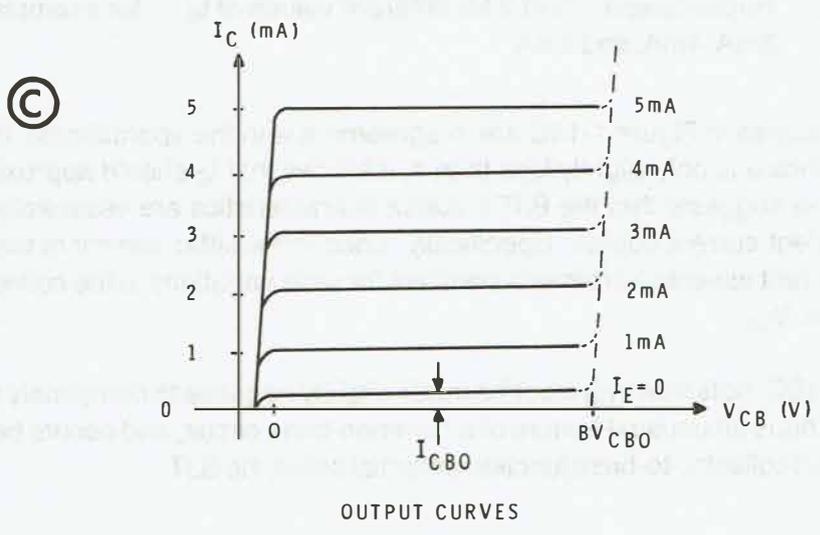
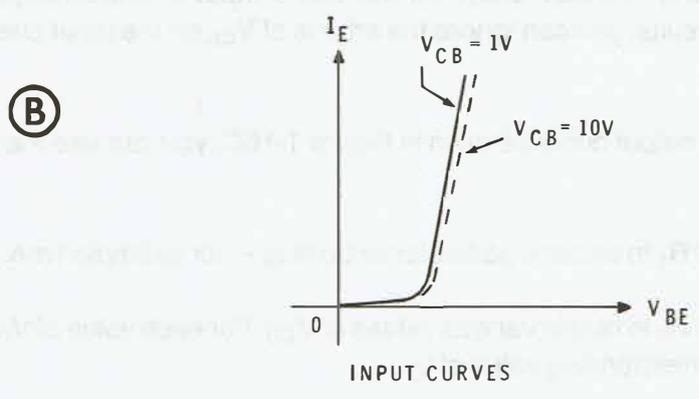
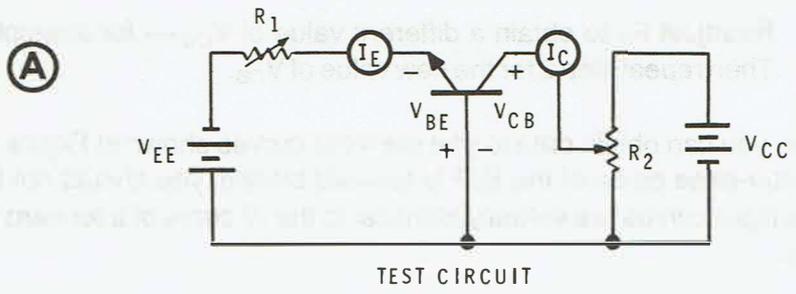


Figure 1-16

- Input and output curves for the common base configuration
- A. Test circuit.
 - B. Input curves.
 - C. Output curves.

2. Adjust R_1 to obtain various values of I_E . For each value of I_E , note the corresponding value of V_{BE} .
3. Readjust R_2 to obtain a different value of V_{CB} — for example 10V. Then repeat step 2 for the new value of V_{CB} .

In this manner, you can obtain data to plot the input curves shown in Figure 1-16B. Since the emitter-base diode of the BJT is forward biased, you should not be surprised that the input curves are virtually identical to the IV curve of a forward biased junction diode.

In Figure 1-16B, note that the curve obtained when $V_{CB} = 10V$ differs only slightly from the curve obtained when $V_{CB} = 1V$. Based on this observation, it should be clear that V_{CB} has only a minor affect on the BJT's input characteristics. Consequently, in most circuits, you can ignore the effects of V_{CB} on the input characteristics of the BJT.

In order to obtain the output curves shown in Figure 1-16C, you can use the following procedure.

1. Adjust R_1 to obtain a particular value of I_E — for example 1mA.
2. Adjust R_2 to obtain various values of V_{CB} . For each value of V_{CB} , note the corresponding value of I_C .
3. Repeat steps 1 and 2 for different values of I_E — for example 2mA, 3mA, 4mA, and 5mA.

The output curves in Figure 1-16C are in agreement with the approximate, formula $I_C = \alpha I_E$. Since α is only slightly less than 1, it follows that I_C should approximately equal I_E . This suggests that the BJT's output characteristics are essentially those of a dependent current source. Specifically, once the emitter current is fixed, the collector current essentially remains constant for wide variations in the collector-to-base voltage, V_{CB} .

In Figure 1-16C, note that V_{CB} must be made slightly negative to completely reduce I_C to zero. This is an unusual feature of a common-base circuit, and occurs because of an inherent collector-to-base junction potential within the BJT.

In Figure 1-16A, the polarity of V_{CB} is such that the collector-base diode is reverse biased. Consequently, as V_{CB} is increased, eventually a point is reached where the collector base diode breaks down. Once this point is reached, the collector current increases sharply, and can destroy the transistor. The value of this collector break down voltage is designated as BV_{CBO} or V_{CBO} . Obviously, in a given circuit, V_{CB} should never be permitted to equal or exceed the value of BV_{CBO} .

When $I_E = 0$, you have a situation that is essentially equivalent to an open emitter lead. For this reason, when $I_E = 0$, $I_C = I_{CBO}$ as shown by the bottom curve in Figure 1-16C. For clarity, the value of I_{CBO} has been exaggerated on the bottom curve in Figure 1-16C.

A circuit that can be used to obtain both input and output curves for an NPN transistor in the common-emitter configuration is shown in Figure 1-17A. By following a procedure similar to the one used for the common-base circuit, you can obtain the input and output curves shown respectively in Figure 1-17B, and Figure 1-17C.

Once again, the input curves are essentially those of a forward biased junction diode. The output curves in Figure 1-17C are in good agreement with the approximate formula $I_C = \beta I_B$. For example, since β is 100, you would expect I_C to be 10mA when I_B is 100 μ A. Similarly, when $I_B = 80\mu$ A, I_C should be about 8mA. These calculations agree with the curves in Figure 1-17C.

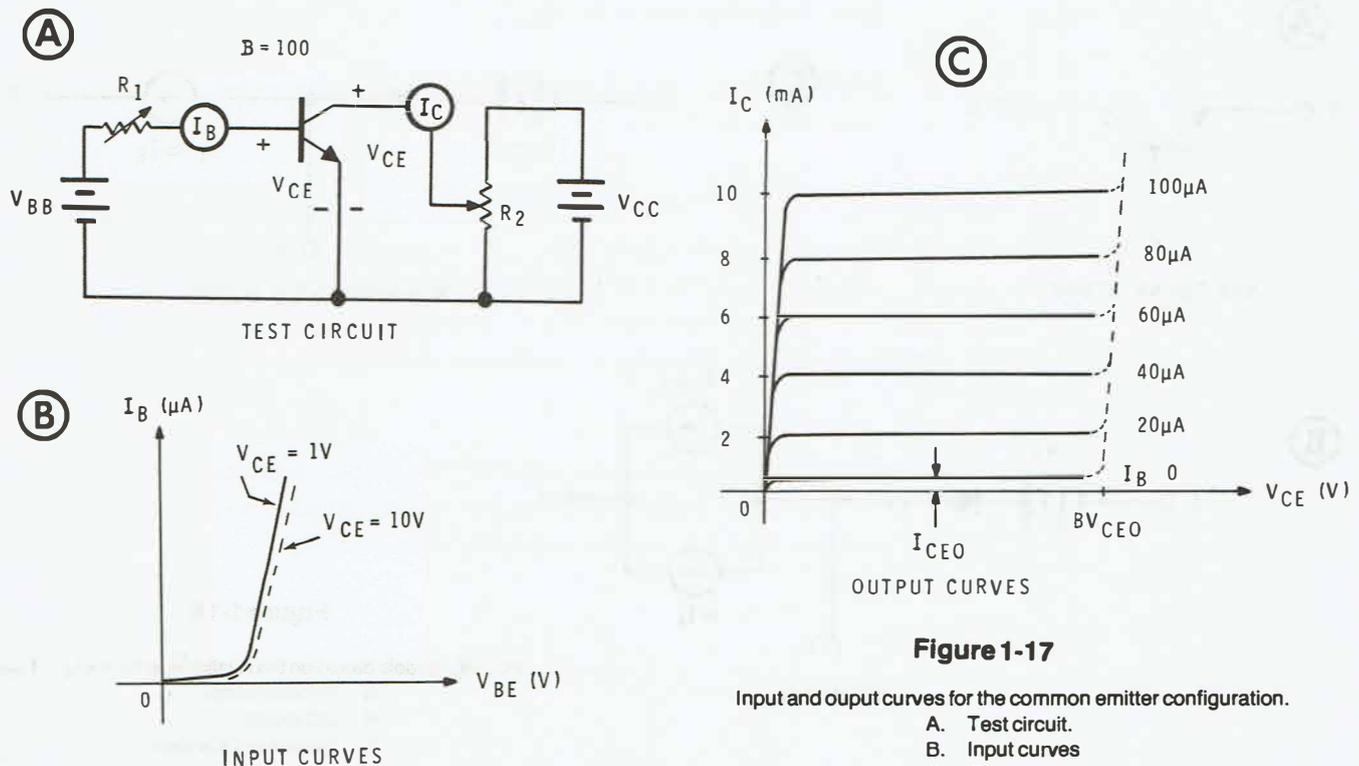


Figure 1-17

Input and output curves for the common emitter configuration.

- A. Test circuit.
- B. Input curves
- C. Output curves

BJT DC Models

The input curves of a BJT indicate that the BJT acts like a forward biased junction diode, when viewed from the emitter-base terminals. Similarly, the BJT's output curves indicate that the BJT acts like a current source, equal to I_C , when viewed from the collector-base terminals. For these reasons, a BJT can be represented by the DC equivalent circuit shown in Figure 1-18B. Here, note that:

1. The emitter-base portion of the BJT has been replaced by the large-signal model of a junction diode.
2. The collector-base portion of the BJT has been replaced by two shunt current sources. Recall that the collector current, I_C , equals $\alpha I_E + I_{CBO}$. Thus, each current source supplies one of the two components of the collector current.

As discussed previously, I_{CBO} is usually negligible compared to αI_E . Also, in most circuits r_F is negligible compared to the external circuit resistance. Consequently, the equivalent circuit in Figure 1-18B can often be simplified as shown in Figure 1-18C. Here, it is assumed that $\alpha = 1$, and that the transistor is a silicon transistor since $V_T = 0.7V$.

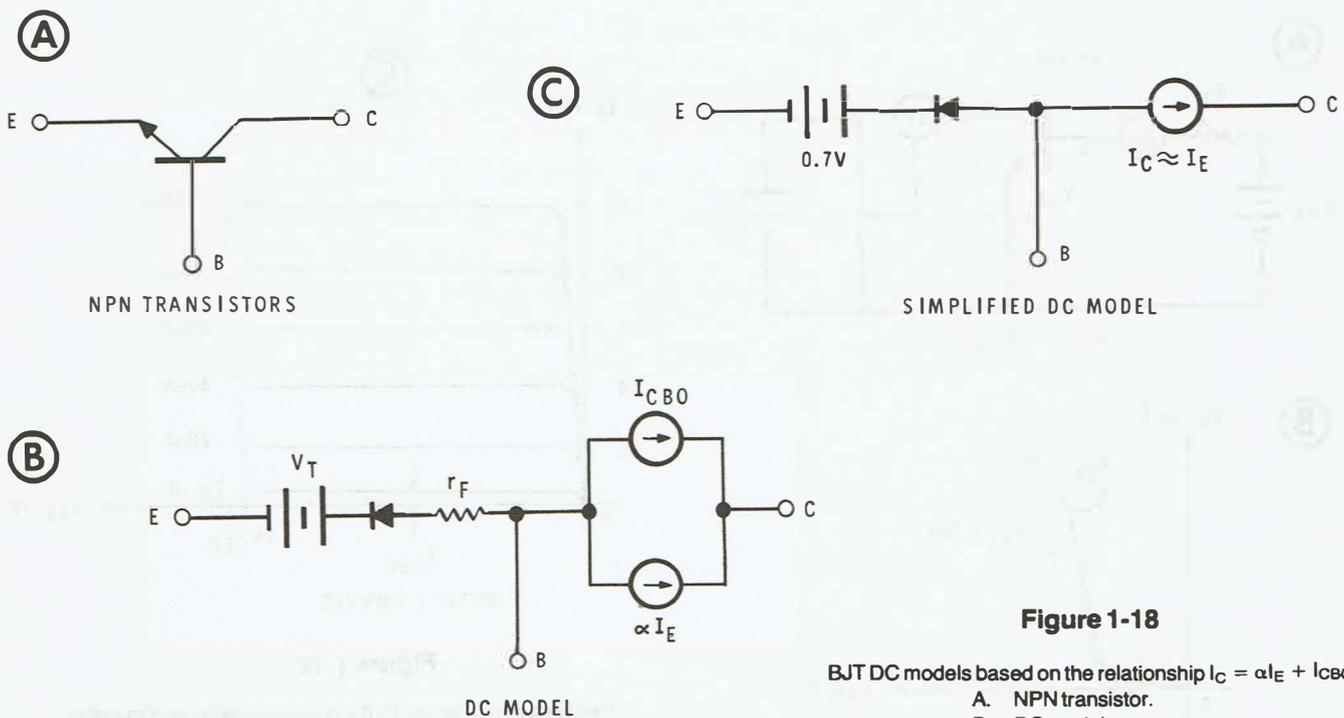


Figure 1-18

BJT DC models based on the relationship $I_C = \alpha I_E + I_{CBO}$

- A. NPN transistor.
- B. DC model.
- C. Simplified DC model.

The current sources in Figure 1-18B generate currents equal to αI_E and I_{CBO} so that $I_C = \alpha I_E + I_{CBO}$. Recall that an equally valid expression for the collector current, I_C , is $I_C = \beta I_B + I_{CEO}$. Consequently, a BJT can also be modeled as shown in Figure 1-19B. Furthermore, if the effects of r_F and I_{CEO} are negligible, the simplified model of Figure 1-19C can be used to represent the DC equivalent circuit of the BJT.

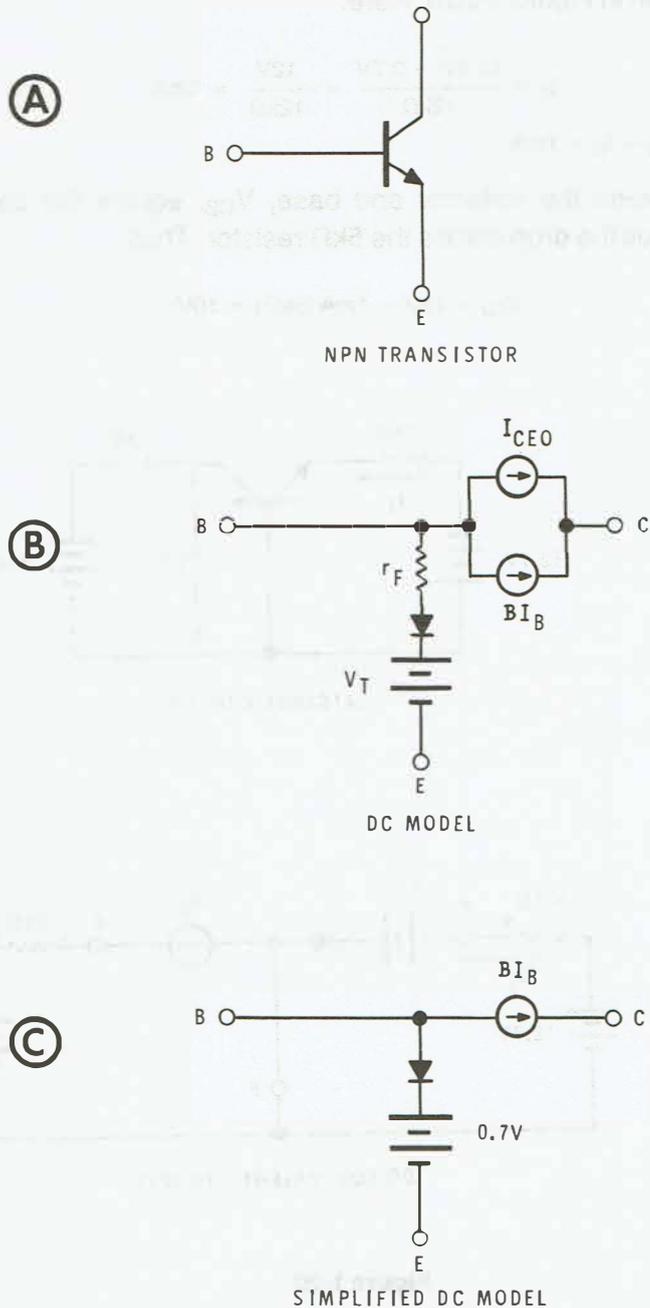


Figure 1-19

BJT DC models based on the relationship $I_C = \beta I_B + I_{CEO}$.

- A. NPN transistor.
- B. DC model.
- C. Simplified DC model.

Example 1-8

For the circuit shown in Figure 1-20A, estimate the values of I_E , I_C and V_{CB} . Assume the effects of r_F and I_{CBO} are negligible.

Using the simplified BJT model of Figure 1-18C, the DC equivalent circuit is sketched as shown in Figure 1-20B. Here:

$$I_E = \frac{12.7V - 0.7V}{12k\Omega} = \frac{12V}{12k\Omega} = 1mA$$

Since $\alpha \approx 1$ $I_C = I_E = 1mA$

The voltage between the collector and base, V_{CB} , equals the collector supply voltage, 15V, minus the drop across the $5k\Omega$ resistor. Thus:

$$V_{CB} = 15V - 1mA(5k\Omega) = 10V$$

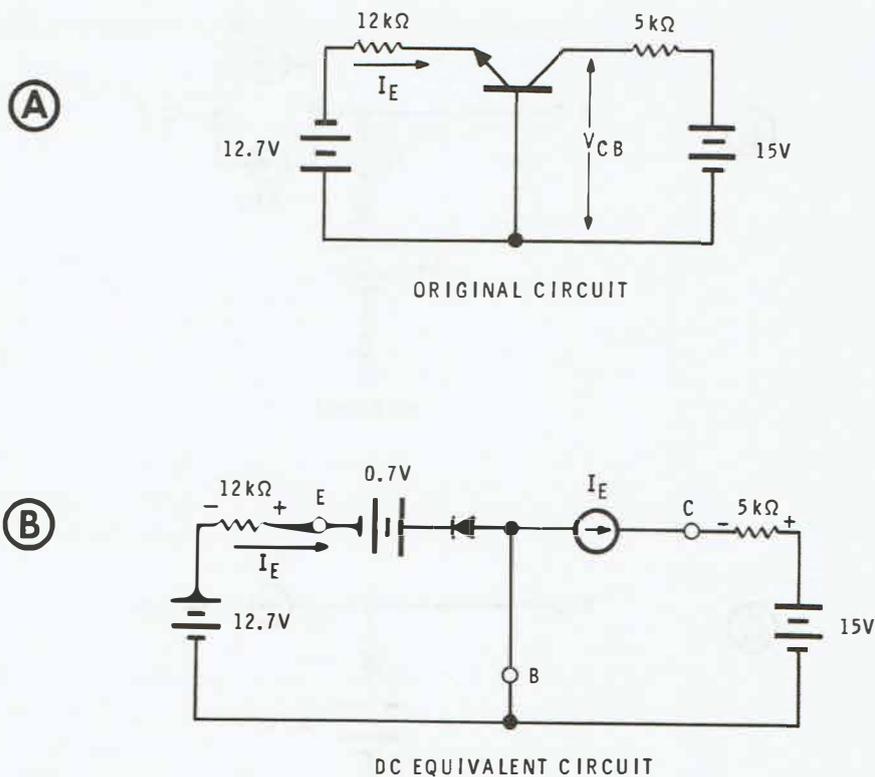


Figure 1-20

Circuits for Example 1-8.

- A. Original circuit.
- B. DC equivalent circuit.

Example 1-9

Estimate the values of I_B , I_C and V_{CE} for the circuit shown in Figure 1-21A.

The circuit in Figure 1-21A is drawn with “ground referenced notation”, in other words, the way it is conventionally drawn on a schematic diagram. For clarity, we have redrawn the circuit as shown in Figure 1-21B. Since the value of B is given, it is convenient to use the simplified BJT DC model of Figure 1-19C. Naturally we are assuming the effects of r_F and I_{CEO} are negligible. If this were not the case, you could use the BJT DC model of Figure 1-19B to analyze the circuit.

The DC equivalent circuit is provided in Figure 1-21C. Here:

$$I_B = \frac{10.7V - 0.7V}{1M\Omega} = \frac{10V}{1M\Omega} = 10\mu A$$

$$I_C = BI_B = 150(10\mu A) = 1.5mA$$

The voltage between the collector and emitter, V_{CE} , equals the collector supply voltage, 20V, minus the drop across the 10kΩ resistor. Thus:

$$V_{CE} = 20V - 1.5mA(10k\Omega) = 5V.$$

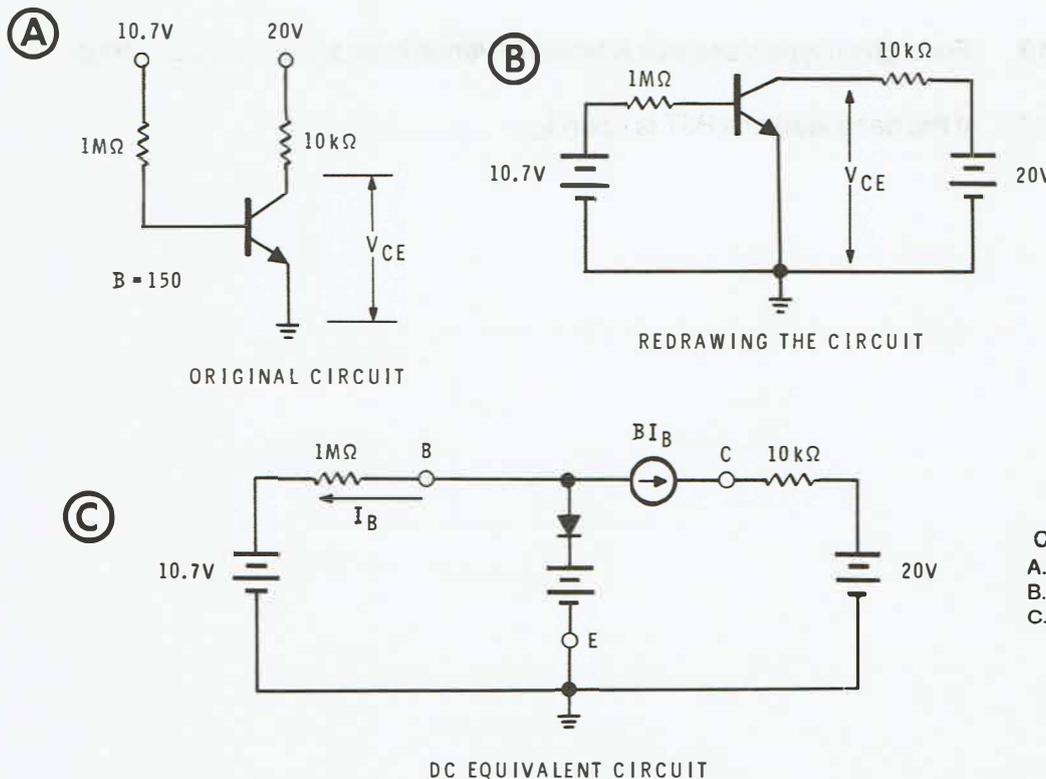


Figure 1-21

- Circuits for Example 1-9.
 A. Original circuit.
 B. Redrawing the circuit.
 C. DC equivalent circuit.

Self-Test Review

11. The emitter base junction of a BJT is normally _____ biased, and the collector-base junction is _____ biased.
12. I_{CEO} is _____ than I_{CBO} .
larger/smaller
13. Electrons are _____ carriers in P-type materials.
14. On a data sheet the symbol _____ represents B.
15. α is approximately equal to _____.
16. When viewed from the emitter-base terminals, a BJT acts like a _____.
17. When viewed from the collector-base terminals, a BJT acts like a _____ source.
18. If the α of a BJT changes from 0.98 to 0.99, B will change from _____ to _____.
19. For a given type transistor B typically varies over a _____ range.
20. If the base lead of a BJT is open $I_C =$ _____.



Answers

- | | |
|----------------------|--------------------------|
| 11. forward, reverse | 16. forward biased diode |
| 12. larger | 17. current |
| 13. minority | 18. 49 to 99 |
| 14. h_{FE} | 19. 4:1 |
| 15. 1 | 20. I_{CEO} |

The solution to question 18 follows:

$$B = \frac{\alpha}{1 - \alpha}$$

Thus, when $\alpha = 0.98$

$$B = \frac{0.98}{1 - 0.98} = 49$$

Similarly, when $\alpha = 0.999$:

$$B = \frac{0.999}{1 - 0.999} = 999$$

Notice that small changes in α produce large changes in B .

SUMMARY

Junction diodes are formed by joining P-type and N-type semiconductor materials. The DC, or large-signal model of a diode is represented by the series combination of an ideal diode, the diode's forward resistance, r_F , and the diode's turn-on voltage V_T .

When a diode is simultaneously driven from a large DC and a small AC source, the diode acts like a resistance to the AC source. This AC, dynamic, resistance consists of two components — bulk resistance, r_B , and junction resistance, r_j . You can estimate a diode's AC resistance by using the following formula:

$$r_{AC} = \frac{37\text{mV}}{I_F} + 1\Omega$$

When you analyze diode and transistor circuits, it is often necessary to obtain DC and AC equivalent circuits. In the DC equivalent circuit, capacitors are replaced by open circuits, and the device is replaced by its large-signal model. Similarly, in the AC equivalent circuit, capacitors are replaced by short circuits, and the device is replaced by its AC, or small-signal, model.

You can use graphic methods, using load lines, to analyze diode, and transistor circuits. The intersection between the DC load line, and the device's characteristic curve establishes the DC or quiescent operating point. The AC load line is useful for determining how a device responds to AC signals. You will encounter applications for load lines in later units.

BJTs consist of NPN or PNP "semiconductor sandwiches". For normal operation of a BJT, the emitter-base junction is forward biased, and the collector-base junction is reverse biased. Consequently, the current directions and voltage polarities in PNP circuits are just the opposite of those encountered in NPN circuits.

Frequently, BJT circuits are classified as common-base, common-emitter, or common-collector circuits. In each case, one lead is connected to the AC signal source, and one lead is used as the take-off point for the AC output voltage. The remaining lead is termed the "common", and identifies the particular configuration.

BJTs operate by the processes of injection, diffusion, and collection. The forward biased emitter-base junction majority carriers are injected from the emitter region into the base region. Since the base region is thin and has few of its own majority carriers, the injected carriers rapidly diffuse, or spread out, in the base region.

Finally, most of the injected carriers are swept across the reverse biased collector-base junction where they are effectively collected by the relatively large collector region.

Various parameters and formulas used to describe the operation of BJTs were introduced in the unit. Important parameters include α , β or h_{FE} , V_{BE} , I_{CBO} , I_{CEO} , BV_{CBO} , and BV_{CEO} . Definitions for these parameters are provided in appropriate sections in the unit. Many of these parameters vary widely from one BJT to another. In addition, V_{BE} , I_{CBO} , I_{CEO} , and h_{FE} are very temperature sensitive.

Table 1-3 summarizes the most frequently used BJT DC formulas. By using the formulas for I_C given in Table 1-3, two equivalent DC models for the BJT were developed. Examples illustrating the use of each model are provided in the unit.

Complete Experiment 1 in Unit 9 at this time.

Finally, most of the included names are single names that were found in the
same region where they are listed, only selected by the surveyor in the
region.

Various government and business names are included in the list of
names. In the past, important government officials such as the Mayor, the
Mayor and Mayor. Various business names are included in the list of
names. Many of these names are listed in the list of names in the list of
names. In addition, the list of names is a list of names.

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Complete the list of names in the list of names.

UNIT EXAMINATION

The following multiple choice examination is designed to test your understanding of the material presented in this unit. Place a check beside the multiple choice answer (A, B, C, or D) that you feel is most correct. When you have completed the examination, compare your answers with the correct ones that appear after the exam.

1. A BJT has an I_{CBO} of 150nA and an h_{FE} of 100. The value of I_{CEO} is therefore:
 - A. 150nA.
 - B. 1.5nA.
 - C. 15.15 μ A.
 - D. 1.5mA.
2. A diode has a DC current of 2mA. The dynamic resistance of the diode is therefore approximately:
 - A. 19.5 Ω .
 - B. 0 Ω , since the diode is forward biased.
 - C. $\infty\Omega$.
 - D. Depends on whether the diode is Ge or Si.
3. In Figure 1-22, the DC load line would have a vertical intercept of:
 - A. 4mA.
 - B. 6mA.
 - C. 8mA.
 - D. 10mA.

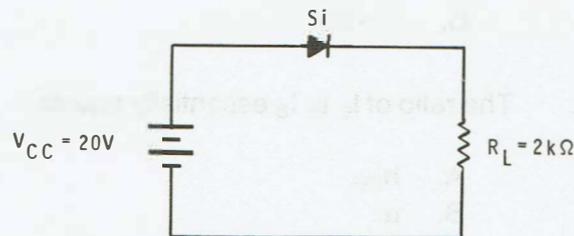


Figure 1-22

Circuit for questions 3 and 4.

4. In Figure 1-22, the DC load line would have a horizontal intercept of:
 - A. 0V.
 - B. 20V.
 - C. ∞V .
 - D. Depends on the diode's turn-on voltage.

5. In Figure 1-22 the DC load line has a slope of:

- A. $1/20\text{k}\Omega$.
- B. $-1/20\text{k}\Omega$.
- C. $1/5\text{k}\Omega$.
- D. $-1/5\text{k}\Omega$.

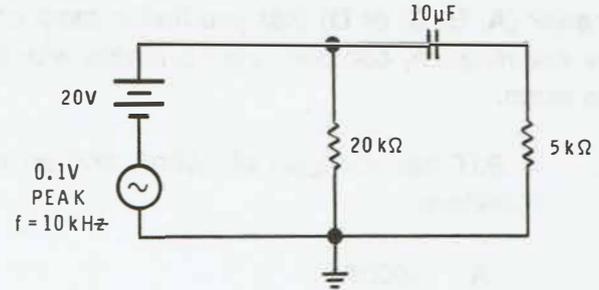


Figure 1-23

Circuit for questions 5 and 6.

6. In Figure 1-23, the AC load line has a slope of:

- A. $-1/20\text{k}\Omega$.
- B. $-1/5\text{k}\Omega$.
- C. $-1/4\text{k}\Omega$.
- D. $-1/25\text{k}\Omega$.

7. Leakage currents can be considered negligible if:

- A. $\alpha > 1$.
- B. $I_{CBO} = I_{CEO}$.
- C. $I_E / I_{CBO} \geq 20$.
- D. $B \geq 20$.

8. The ratio of I_C to I_B essentially equals:

- A. h_{FE} .
- B. α .
- C. $\alpha + 1$.
- D. B^2 .

9. Small changes in α produce:

- A. Small changes in B .
- B. Moderate changes in B .
- C. Large changes in B .
- D. No changes in B .

10. The thinnest region of a BJT is the:
- A. Emitter
 - B. Base.
 - C. Collector.
 - D. Anode.
11. Which of the following varies linearly with temperature?
- A. h_{FE} .
 - B. I_{CBO} .
 - C. I_{CEO} .
 - D. V_{BE} .
12. BJT maximum ratings are usually:
- A. Stamped on the BJT case.
 - B. Not available.
 - C. Specified at 25°C.
 - D. Specified at 75°C.
13. The thickest region of a BJT is the:
- A. Emitter
 - B. Base.
 - C. Collector.
 - D. Anode.
14. The output curves for the common-emitter configurations show the relationship between the BJT's:
- A. I_C , I_B and V_{CE} values.
 - B. I_C , I_B and V_{CB} values.
 - C. I_E , I_C and V_{CB} values.
 - D. I_E , I_B and V_{CE} values.

10. The primary reason for a BJT being

- A. emitter
- B. base
- C. collector
- D. anode

11. Which of the following statements will be true?

- A. The
- B. also
- C. less
- D. var

12. BJT maximum gain is usually

- A. 100
- B. 1000
- C. 10000
- D. 100000

13. The primary reason a BJT is used

- A. emitter
- B. base
- C. collector
- D. anode

14. The most common reason for the common-emitter configuration is that it provides the highest

- A. input impedance
- B. output impedance
- C. voltage gain
- D. current gain

EXAMINATION ANSWERS

1. C — $I_{CEO} = (B + 1) I_{CBO}$.

$$I_{CEO} = (101)(150\text{nA}) = 15.15\mu\text{A}$$

2. A — $r_{AC} \approx \frac{37\text{mV}}{I_F} + 1\Omega$

$$r_{AC} = \frac{37\text{mV}}{2\text{mA}} + 1\Omega = 19.5\Omega$$

3. D — The vertical intercept of the DC load line is V_{CC}/R_L . Thus:

$$\frac{V_{CC}}{R_L} = \frac{20\text{V}}{2\text{k}\Omega} = 10\text{mA}$$

4. B — The horizontal intercept of the DC load line is V_{CC} . Thus:

$$V_{CC} = 20\text{V}$$

5. B — The DC load line has a slope of $-1/R_L$, where R_L is the DC diode load resistance. Thus:

$$m = -\frac{1}{20\text{k}\Omega}$$

6. C — The AC load line has a slope of $-1/r_L$ where r_L is the AC diode load resistance. Thus, in this case:

$$r_L = 20\text{k}\Omega \parallel 5\text{k}\Omega = 4\text{k}\Omega$$

$$m = -\frac{1}{4\text{k}\Omega}$$

7. C — As a guide, leakage currents can be neglected if:

$$\frac{I_E}{\beta I_{CBO}} \geq 20$$

8. A — $B = h_{FE} = \frac{I_C}{I_B}$

9. C — Small changes in α results in large changes in B.
10. B — The base region of a BJT is very thin, and lightly doped.
11. D — For both silicon and germanium BJTs, V_{BE} decreases by approximately 2 to 2.5mV for each °C rise in temperature.
12. C — Maximum ratings are usually specified at 25°C.
13. C — The collector region of a BJT is the thickest region.
14. A — The corresponding values of I_C and V_{CE} are plotted for various values of I_B .

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UNIT 2

BIASING SCHEMES

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INTRODUCTION

The first step in designing a transistor circuit is to select a suitable operating point for the transistor. The purpose of the biasing circuit is to establish the desired operating point.

In this unit, you will study the most frequently encountered BJT biasing circuits. Since the common-emitter circuit is used more extensively than the common-base and common-collector circuits, our discussion emphasizes common-emitter biasing techniques.

Numerous summary guides are included at appropriate points in order to simplify the analysis and design process. Once NPN biasing circuits are covered, a discussion of complementary PNP circuits is presented.

UNIT OBJECTIVES

When you have completed this unit, you should be able to:

1. Analyze and design the following biasing circuits using NPN transistors:

Base bias.

Emitter feedback bias.

Collector feedback bias.

Collector and emitter feedback bias.

Voltage divider bias.

Emitter bias.

2. Sketch complementary PNP biasing circuits.
3. Sketch PNP circuits as they usually appear on schematic diagrams.
4. Analyze and design complementary PNP biasing circuits.

UNIT ACTIVITY GUIDE

- Read section on “Base Bias Circuits”.
- Answer Self-Test Review Questions 1-10.
- Read section on “Quasi-Stable Biasing Circuits”.
- Answer Self-Test Review Questions 11-20.
- Perform Experiment 2 in Unit 9.
- Read section on “Stable Biasing Circuits”.
- Answer Self-Test Review Questions 21-27.
- Perform Experiment 3 in Unit 9.
- Study Summary.
- Complete Unit Examination.
- Check Examination Answers.

BASE BIAS CIRCUITS

In the previous unit, the transistor was discussed as an isolated circuit component. This unit examines the transistor as an important part of a more complex DC circuit.

The purpose of a biasing circuit is to establish an appropriate DC operating point for the transistor. Consequently, we will begin our discussion of biasing schemes by considering the range of possible DC operating points within which a particular BJT can operate.

Modes of Operation

A BJT can be biased to operate in any one of three possible regions or modes: cutoff, saturation and active, or linear. Recall that this concept was briefly introduced in Experiment 1 of Unit 9. The important characteristics for each region are summarized in the following sections.

CUTOFF

In this mode, both the emitter-base and collector-base junctions are reverse biased. Consequently, except for a relatively small reverse current, the transistor is nonconducting and $I_C \approx 0$. In a common-emitter circuit, the collector-to-emitter voltage, V_{CE} , is maximum. The value of V_{CE} is determined by component values in the external circuit. Since $I_C \approx 0$ and V_{CE} is maximum, the transistor acts like an open switch when viewed from the collector-emitter terminals.

SATURATION

In this mode, both the emitter-base and collector-base junctions are forward biased. For this reason, the transistor conducts heavily, and I_C is maximum. The value of I_C is determined by component values in the external circuit. Ideally, $V_{CE} = 0V$. In real circuits, V_{CE} is typically a few tenths of a volt for general purpose BJT's. Since I_C is maximum and $V_{CE} \approx 0$, the transistor acts like a closed switch when viewed from the collector-emitter terminals.

ACTIVE

In this mode, the emitter-base junction is forward biased and the collector-base junction is reverse biased. The active region is the normal mode of operation for linear transistor circuits. This type of circuit is emphasized in this course.

In the active region, values of I_C and V_{CE} fall within the extremes of I_C and V_{CE} characteristic of the cutoff and saturation regions. For this reason, the transistor acts like a resistance, equal to V_{CE}/I_C , when viewed from the collector-emitter terminals. In addition, the emitter and collector currents are directly proportional to the base current since, in the active region, $I_E \approx I_C \approx \beta I_B$.

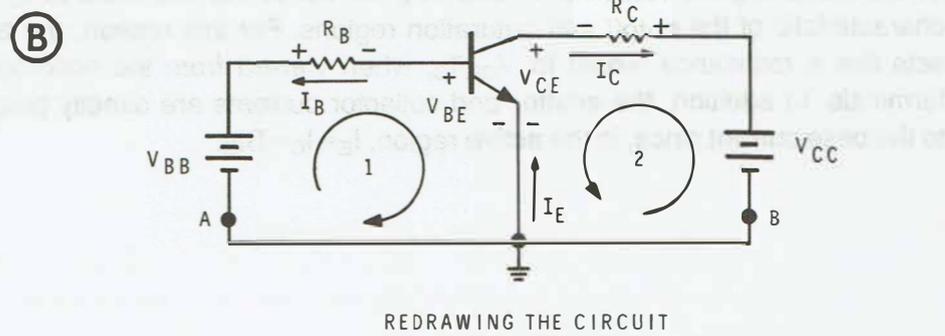
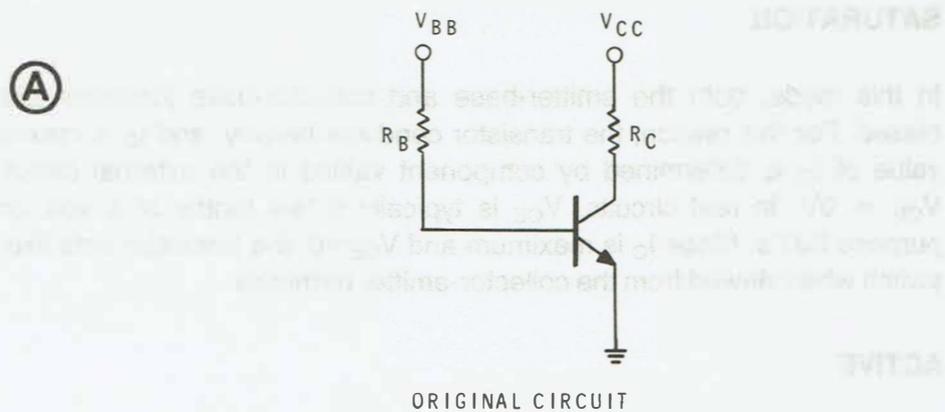


Figure 2-1

- Base bias.
 A. Original circuit.
 B. Redrawing the circuit.

Base Bias Analysis

The common emitter circuit in Figure 2-1A illustrates base bias. This is one of the simplest ways to bias a BJT. The circuit is easy to redraw to emphasize the base and collector loops as shown in Figure 2-1B. Here, by applying Kirchhoff's voltage law to the base loop, and starting at point A and going around the loop in a clockwise direction, yields:

$$-V_{BB} + I_B R_B + V_{BE} = 0 \quad (\text{loop 1})$$

Solving the base loop equation for the base current, I_B , you obtain:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} \quad (\text{Eq. 2-1})$$

Typically, V_{BE} is small compared to the base supply voltage V_{BB} . Consequently, the value of I_B is essentially “fixed” by the value chosen for R_B . For this reason, base bias is also referred to as fixed bias.

Assuming the effects of I_{CEO} are negligible, the collector current, I_C , equals:

$$I_C = \beta I_B \approx I_E$$

Applying Kirchhoff’s voltage law to the collector loop, by starting at point B and going around the loop in a counterclockwise direction, yields:

$$-V_{CC} + I_C R_C + V_{CE} = 0 \quad (\text{loop 2})$$

Solving the collector loop equation for the collector-to-emitter voltage, V_{CE} , you obtain:

$$V_{CE} = V_{CC} - I_C R_C \quad (\text{Eq. 2-2})$$

The variables in Equation 2-2, I_C and V_{CE} , are the variables displayed graphically by the BJT’s output, or collector, curves. Consequently, Equation 2-2 is the equation of the circuit’s DC load line. As you recall, the DC load line represents all possible DC operating points for a given circuit. One end of the line corresponds to the saturation mode and the other end to the cutoff mode.

In the saturation mode, V_{CE} equals $V_{CE(\text{sat})}$ and I_C equals $I_{C(\text{sat})}$. A typical value of $V_{CE(\text{sat})}$ can be obtained from the BJT’s data sheet. Substituting $V_{CE(\text{sat})}$ for V_{CE} , and $I_{C(\text{sat})}$ for I_C into Equation 2-2 yields:

$$V_{CE(\text{sat})} = V_{CC} - I_{C(\text{sat})} R_C$$

Solving for $I_{C(\text{sat})}$ you obtain:

$$I_{C(\text{sat})} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} \quad (\text{Eq. 2-3})$$

For a given circuit, Equation 2-3 predicts the maximum possible DC collector current.

In the cutoff mode, I_C equals I_{CEO} , and V_{CE} equals $V_{CE(\text{cut})}$. Substituting $V_{CE(\text{cut})}$ for V_{CE} , and I_{CEO} for I_C into Equation 2-2 yields:

$$V_{CE(\text{cut})} = V_{CC} - I_{CEO} R_C \quad (\text{Eq. 2-4})$$

For a given circuit, Equation 2-4 predicts the maximum possible DC collector-to-emitter voltage.

The points on the DC load line corresponding to saturation and cutoff intersect the collector curves at $I_B = I_{B(\text{sat})}$ and $I_B = 0$ as shown in Figure 2-2A. Here, the minimum value of base current, $I_{B(\text{sat})}$, required to produce saturation is:

$$I_{B(\text{sat})} = \frac{I_{C(\text{sat})}}{\beta} \quad (\text{Eq. 2-5})$$

Since $I_{C(\text{sat})}$ is the maximum possible DC collector current, values of I_B larger than $I_{B(\text{sat})}$ do not produce values of I_C larger than $I_{C(\text{sat})}$. Consequently, the relationship $I_C \approx \beta I_B$ is **not** valid for values of I_B larger than $I_{B(\text{sat})}$.

All points on the DC load line between saturation and cutoff are in the BJT's active region. Typically, when used as an amplifier, the transistor is biased to establish a DC operating point at, or near, the middle of the load line as shown in Figure 2-2B. Here, the following points should be noted.

1. The subscript Q is employed to indicate the values of collector current, I_{CQ} , and collector-to-emitter voltage, V_{CEQ} , at the operating point.
2. The DC load line has a slope equal to $-1/R_C$.
3. The DC load line crosses the vertical axis when $V_{CE} = 0$. Consequently, the value of the vertical intercept can be calculated by substituting $V_{CE} = 0$ into Equation 2-2. Specifically:

$$0 = V_{CC} - I_C R_C$$

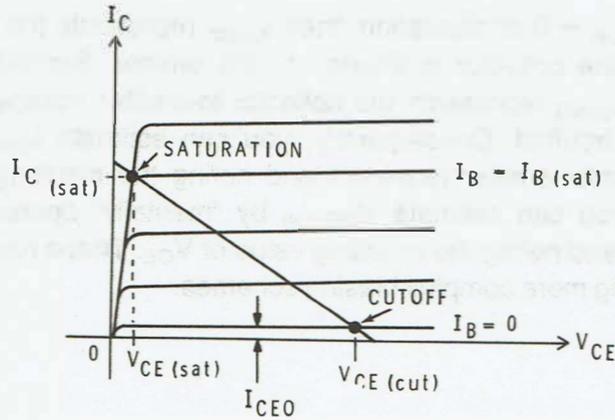
Solving for I_C yields:

$$I_C = \frac{V_{CC}}{R_C} \quad (\text{vertical intercept})$$

4. The DC load line crosses the horizontal axis when $I_C = 0$. Therefore, the value of the horizontal intercept can be calculated by substituting $I_C = 0$ into Equation 2-2. Thus:

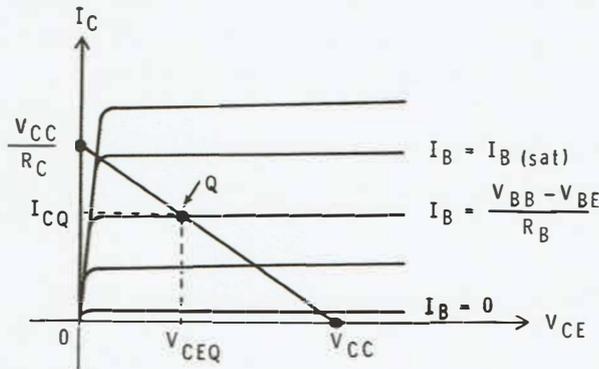
$$V_{CE} = V_{CC} \quad (\text{horizontal intercept})$$

(A)



SATURATION AND CUT OFF POINTS ON THE DC LOAD LINE.

(B)



A QUIESCENT, Q, OPERATING POINT IN THE ACTIVE REGION.

Figure 2-2

The DC load line.

- A. Saturation and cutoff points on the DC load line.
- B. A quiescent, Q, operating point in the active region.

Comparing Figure 2-2A with Figure 2-2B, you can see that the value of I_C at the vertical intercept in Figure 2-2B is only slightly larger than $I_{C(sat)}$ in Figure 2-2A. Similarly, the value of V_{CE} at the horizontal intercept in Figure 2-2B is only slightly larger than $V_{CE(cut)}$ in Figure 2-2A. For these reasons, $I_{C(sat)}$ and $V_{CE(cut)}$ are closely approximated by the vertical and horizontal intercept values respectively. Stated mathematically:

$$I_{C(sat)} \approx \frac{V_{CC}}{R_C} \quad (\text{Eq. 2-6})$$

$$V_{CE(cut)} \approx V_{CC} \quad (\text{Eq. 2-7})$$

In effect, since $V_{CE} \approx 0$ at saturation, then $I_{C(sat)}$ represents the collector current that flows when the collector is shorted to the emitter. Similarly, since $I_C \approx 0$ at cutoff, then $V_{CE(cut)}$ represents the collector-to-emitter voltage if the collector-emitter is open circuited. Consequently, you can estimate $I_{C(sat)}$ by “mentally” shorting the collector-emitter terminals and noting the resulting value of I_C . In the same way, you can estimate $V_{CE(cut)}$ by “mentally” opening the collector-emitter terminals and noting the resulting value of V_{CE} . These rules are especially useful for analyzing more complex biasing schemes.

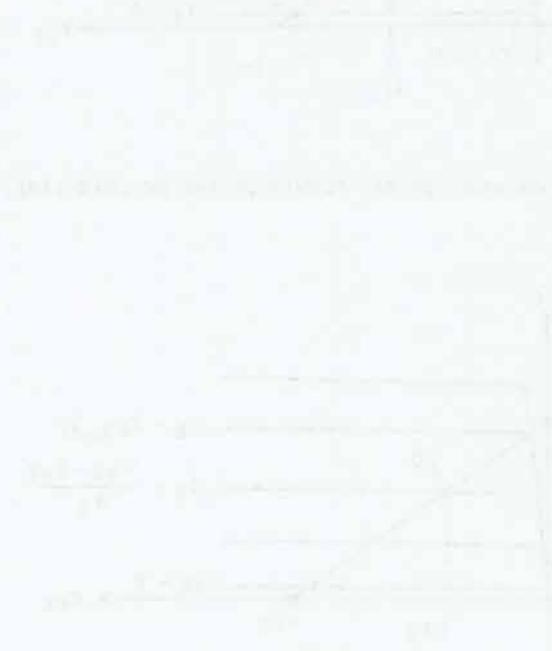


FIGURE 2-11

Comparing Figure 2-10 with Figure 2-11, you can see that the value of V_{CE} is the vertical intercept in Figure 2-10 and the horizontal intercept in Figure 2-11. Similarly, the value of I_C is the horizontal intercept in Figure 2-10 and the vertical intercept in Figure 2-11. These intercept values are directly related to the values of $V_{CE(cut)}$ and $I_{C(sat)}$ respectively. The values of $V_{CE(cut)}$ and $I_{C(sat)}$ are the values of V_{CE} and I_C respectively when the collector-emitter terminals are open and shorted, respectively.

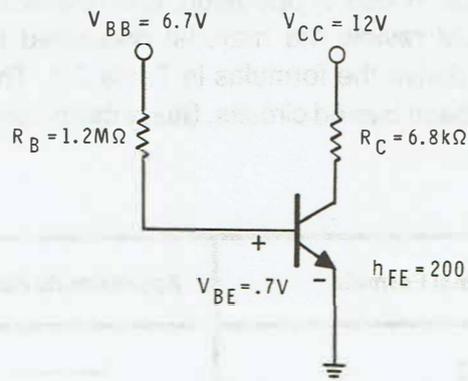
A summary of the various modes of operation, and relevant formulas, is provided in Table 2-1. You should review the material presented this far to make sure you understand how to derive the formulas in Table 2-1. The following examples illustrate the analysis of base biased circuits. Study them carefully.

Mode	Original Formula	Approximate Formula	Comment
Cutoff	$I_B = 0$ $I_C = I_E = I_{CEO}$ $V_{CE(cut)} = V_{CC} - I_{CEO} R_C$	$I_C = I_E = 0$ $V_{CE(cut)} = V_{CC}$	Collector and emitter terminals approximate an open circuit.
Saturation	$I_B > I_{B(sat)}$ $I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$ $V_{CE} = V_{CE(sat)}$	$I_{C(sat)} = \frac{V_{CC}}{R_C}$ $V_{CE(sat)} = 0$	Collector and emitter terminals approximate a short circuit.
Active	$I_B = \frac{V_{BB} - V_{BE}}{R_B}$ $I_C \approx \beta I_B = I_E$ $V_{CE} = V_{CC} - I_C R_C$	 	Operating point is usually near the middle of the load line.

TABLE 2-1

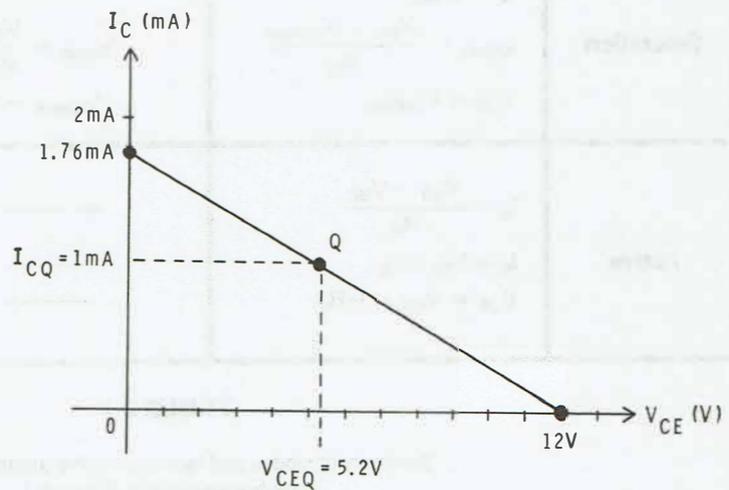
Summary of modes and formulas for the common-emitter base-biased circuit in Figure 2-1.

(A)



CIRCUIT

(B)



DC LOAD LINE

Figure 2-3

Circuit and load line for Example 2-1.

- A. Circuit.
- B. DC load line.

Example 2-1

The silicon transistor in Figure 2-3A has a negligible value of I_{CEO} . Estimate the DC collector current and DC collector-to-emitter voltage. Also sketch the DC load line and indicate the location of the DC operating point.

First calculate the DC base current. Keep in mind that for a silicon transistor the turn-on voltage, V_T , is $.7V$. In our circuit, $V_{BE} = V_T$.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{6.7V - 0.7V}{1.2M\Omega} = 5\mu A$$

Since $h_{FE} = \beta$, the DC collector current is:

$$I_C \approx \beta I_B \approx 200(5\mu A) = 1mA$$

The collector-to-emitter voltage equals the V_{CC} supply voltage minus the drop across R_C . Thus:

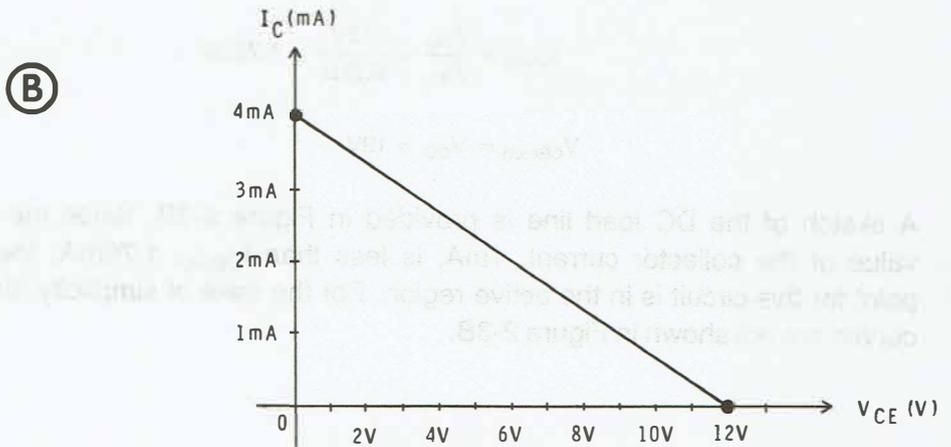
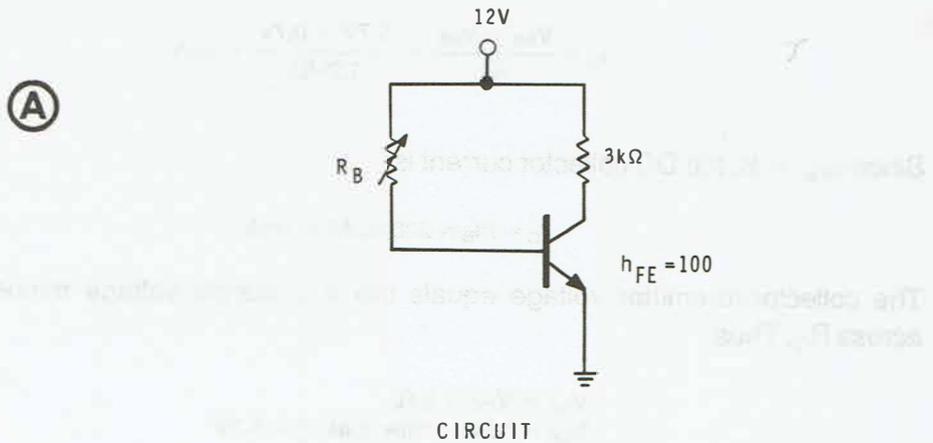
$$\begin{aligned} V_{CE} &= V_{CC} - I_C R_C \\ V_{CE} &= 12V - 1mA(6.8k\Omega) = 5.2V \end{aligned}$$

The coordinates of the Q point are $I_{CQ} = 1mA$, and $V_{CEQ} = 5.2V$. The intercepts of the DC load line correspond, approximately, to $I_{C(sat)}$ and $V_{CE(cut)}$. Therefore:

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{12V}{6.8k\Omega} = 1.76mA$$

$$V_{CE(cut)} = V_{CC} = 12V$$

A sketch of the DC load line is provided in Figure 2-3B. Since the calculated value of the collector current, 1mA, is less than $I_{C(sat)}$, 1.76mA, the operating point for this circuit is in the active region. For the sake of simplicity, the collector curves are not shown in Figure 2-3B.



DC LOAD LINE

Figure 2-4

Circuit and load line for Example 2-2.

- A. Circuit.
- B. DC load line.

Example 2-2

Sketch the DC load line for the circuit shown in Figure 2-4A. Work out the coordinates of the Q point for the following values where $R_B = \infty, 565k\Omega, 282.5k\Omega$ and $100k\Omega$.

The circuit examined previously used two DC sources to bias the transistor. One source, V_{BB} , forward biased the emitter-base junction and the second source, V_{CC} , reverse biased the collector-base junction. The circuit in Figure 2-4A is an example of a **single-supply** base-bias circuit. The single-supply circuit can be treated as a "special case" of the two-supply circuit, where $V_{BB} = V_{CC}$. Consequently, the formulas derived previously are applicable to the single-supply circuit.

To sketch the DC load line, you must first determine the intercept values as follows:

$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C} = \frac{12\text{V}}{3\text{k}\Omega} = 4\text{mA}$$

$$V_{CE(\text{cut})} = V_{CC} = 12\text{V}$$

Consequently, the load line appears as shown in Figure 2-4B. Note that the maximum possible DC collector current is 4mA.

$$R_B = \infty$$

When $R_B = \infty$, it is obvious that $I_B = 0$. Assuming I_{CEO} is negligible, I_C also equals zero, which places the transistor in the cutoff mode. Thus, the coordinates of the Q point are:

$$\left. \begin{array}{l} I_{CQ} = 0 \\ V_{CEQ} = V_{CE(\text{cut})} = 12\text{V} \end{array} \right\} R_B = \infty$$

When $R_B = 565\text{k}\Omega$, you have:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{12\text{V} - 0.7\text{V}}{565\text{k}\Omega} = 20\mu\text{A}$$

$$I_C = \beta I_B = 100(20\mu\text{A}) = 2\text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = 12\text{V} - 2\text{mA}(3\text{k}\Omega) = 6\text{V}$$

Note that the calculated value of I_C , 2mA, is less than $I_{C(\text{sat})}$, 4mA. Thus, the operating point is in the active region at:

$$\left. \begin{array}{l} I_{CQ} = 2\text{mA} \\ V_{CEQ} = 6\text{V} \end{array} \right\} R_B = 565\text{k}\Omega$$

$$R_B = 282.5\text{k}\Omega$$

In this case:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{12\text{V} - 0.7\text{V}}{282.5\text{k}\Omega} = 40\mu\text{A}$$

$$I_C = \beta I_B = 100(40\mu\text{A}) = 4\text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = 12\text{V} - 4\text{mA}(3\text{k}\Omega) = 0\text{V}$$

Reducing R_B from 565k Ω to 282.5k Ω increased the base current just enough to place the operating point in the saturated region. Therefore, the coordinates of the Q point are:

$$\left. \begin{array}{l} I_{CQ} = I_{C(\text{sat})} = 4\text{mA} \\ V_{CEQ} = V_{CE(\text{sat})} \approx 0\text{V} \end{array} \right\} R_B = 282.5\text{k}\Omega$$

$$R_B = 100\text{k}\Omega$$

Proceeding as before you have:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{12\text{V} - 0.7\text{V}}{100\text{k}\Omega} = 113\mu\text{A}$$

$$I_C = \beta I_B = 100(113\mu\text{A}) = 11.3\text{mA} ?$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = 12\text{V} - 11.3\text{mA}(3\text{k}\Omega) = -21.9\text{V} ?$$

Note that the calculated value of I_C , 11.3mA, is larger than $I_{C(sat)}$, which is 4mA. Also note that the calculated value of V_{CE} is negative. Since the maximum possible DC collector current cannot exceed 4mA, something is clearly wrong. Also, it should be apparent that V_{CE} cannot be negative since the DC supply voltage, V_{CC} , is positive with respect to ground. Specifically:

When the calculated value of I_C is larger than $I_{C(sat)}$, the calculated value of V_{CE} for an NPN transistor will be negative. This indicates that the transistor is saturated. Consequently, the actual values of I_C and V_{CE} respectively, are $I_C = I_{C(sat)}$ and $V_{CE} = V_{CE(sat)} \approx 0V$.

Recall that when R_B was 282.5k Ω , I_B was 40 μ A; which was just enough to saturate the transistor. If R_B is less than 282.5k Ω , I_B will naturally be larger than 40 μ A. However, since $I_{C(sat)}$, or 4mA, is the maximum possible DC collector current, values of R_B less than 282.5k Ω **cannot** produce values of I_C larger than 4mA. Consequently, once the transistor is saturated, the approximation $I_C = \beta I_B$ is no longer valid. In any event, when $R_B = 100k\Omega$, the Q point values are:

$$\left. \begin{array}{l} I_{CQ} = I_{C(sat)} = 4\text{mA} \\ V_{CEQ} = V_{CE(sat)} \approx 0\text{V} \end{array} \right\} R_B = 100\text{k}\Omega$$

Figure 2-5 shows how the operating point moves from cutoff to saturation as R_B is decreased from ∞ to 100k Ω .

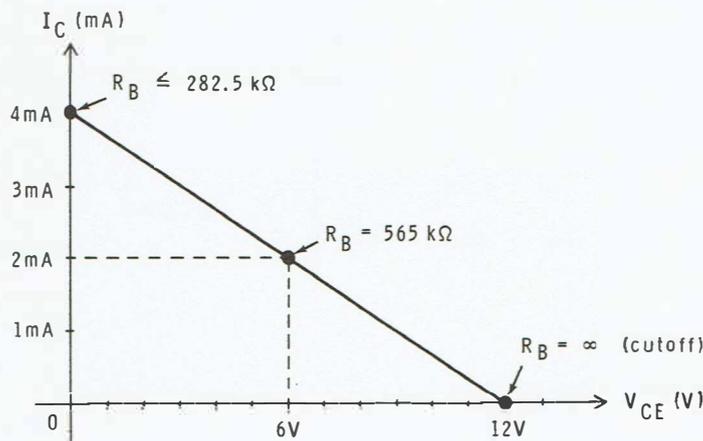


Figure 2-5

Operating points for various values of R_B in Example 2-2.

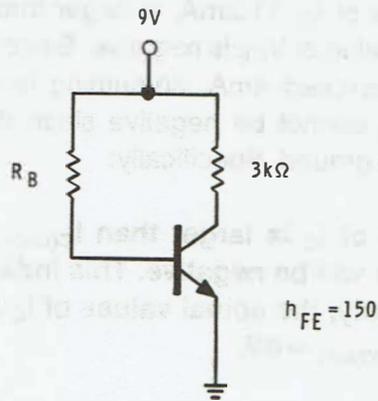


Figure 2-6

Circuit for Example 2-3.

Example 2-3

In Figure 2-6, what value of R is required to just saturate the transistor?

When saturated, I_C equals V_{CC}/R_C , or 3mA . Since $h_{FE} = 150$, the minimum base current required to produce saturation is:

$$I_{B(\text{sat})} = \frac{I_{C(\text{sat})}}{h_{FE}} = \frac{3\text{mA}}{150} = 20\mu\text{A}$$

Since $V_{BB} = 9V$ and V_{BE} is approximately $0.7V$, the required value of R_B via Ohm's law is:

$$R_{B(\text{sat})} = \frac{V_{BB} - V_{BE}}{I_{B(\text{sat})}} \quad (\text{Eq. 2-8})$$

$$R_{B(\text{sat})} = \frac{9V - 0.7V}{20\mu A} = 415k\Omega$$

$415k\Omega$ is the maximum value of R_B that saturates the transistor. Naturally, values of R_B less than $415k\Omega$ also produce saturation.

Switching Circuits

As you will soon see, the simple base bias that we have just discussed is rarely used in linear transistor circuits. Recall that in linear transistor circuits, the Q point is in the active, or linear, region.

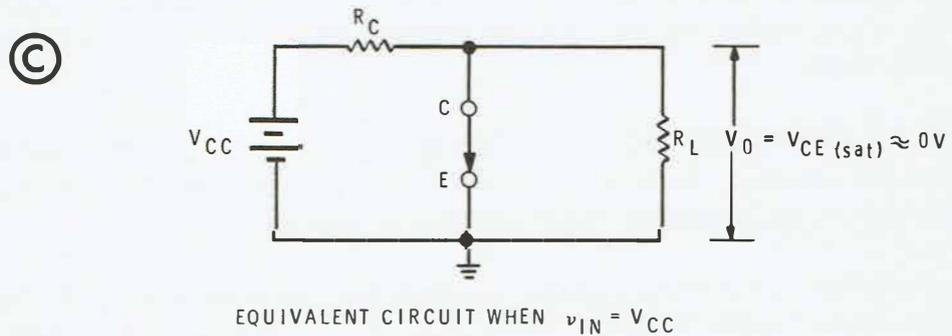
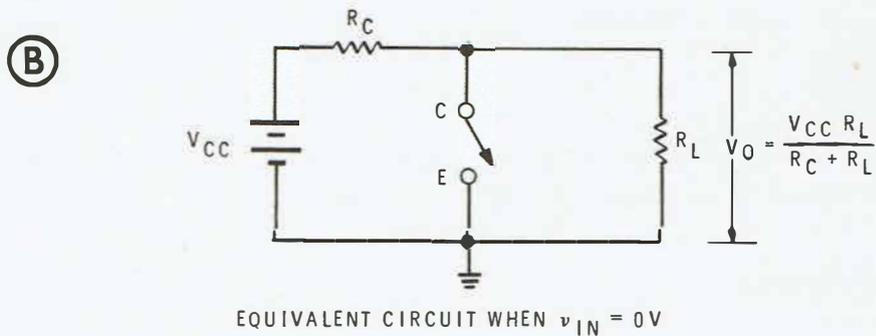
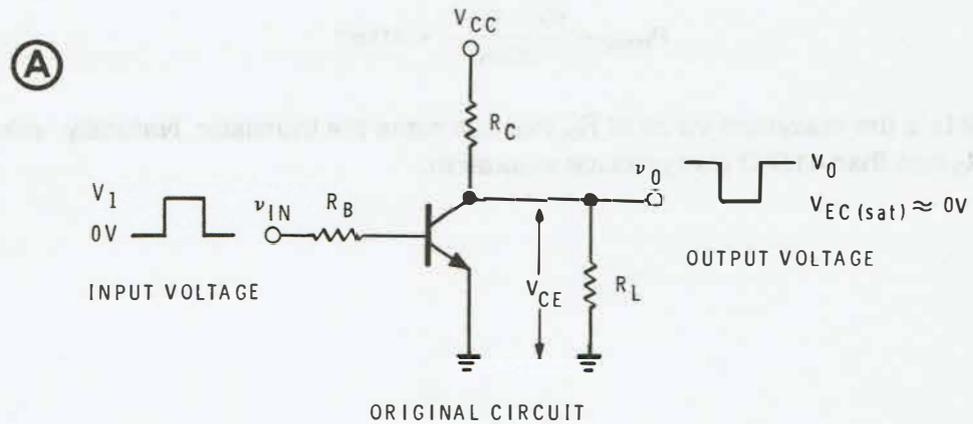


Figure 2-7

An elementary BJT switching circuit.

- A. Original circuit.
- B. Equivalent circuit when $v_{in} = 0V$.
- C. Equivalent circuit when $v_{in} = V_{CC}$.

Applications for base bias are usually restricted to switching or digital circuits — where the transistor functions as an electronic switch. To illustrate this concept, consider the circuit shown in Figure 2-7A. Here, the DC voltage source, V_{BB} , has been replaced by an input voltage, v_{IN} , whose value is restricted to either 0 volts or V_1 volts.

The operation of the circuit in Figure 2-7A is straightforward and can be summarized as follows:

1. When $v_{IN} = 0V$, $I_B = 0$ and the transistor is cut off. Since no collector current flows, the transistor acts like an open switch as shown in Figure 2-7B. In this case, the output voltage via the voltage division principle is:

$$V_o = \frac{V_{CC}R_L}{R_C + R_L}$$

2. When $v_{IN} = V_1$, sufficient base current flows to saturate the transistor. Thus, the transistor acts like a closed switch as shown in Figure 2-7C. Here, note that:

$$V_o = V_{CE(sat)} \approx 0V$$

Since the output voltage is high when the input voltage is low, and vice versa, the circuit in Figure 2-7A is usually referred to as an inverter.

Switching Speed

One of the most important characteristics of a switching circuit is its ability to switch rapidly between the cutoff and saturation modes. Factors that affect switching speed include: component values, stray capacitance and inductance, the specific circuit configuration, the type of transistor used, and the current and voltage levels in the circuit.

The time required to switch from cutoff to saturation is primarily determined by the particular transistor characteristics and the amount of base drive. A large base current, $I_B > I_{B(sat)}$, helps to minimize the turn-on time.

The turn-off time is the time required to switch from saturation to cutoff. Due to storage time, it takes longer to turn a transistor off than it does to turn it on. In any event, by using transistors specifically designed for switching applications — appropriately called switching transistors — it is possible to obtain switching speeds in the nanosecond range.

Designing Simple Switching Circuits

The inverter circuit discussed previously has the load connected in parallel with the transistor. In Figure 2-8, the load is connected in **series** with the transistor. Note that the LED is the series-connected load in Figure 2-8A.

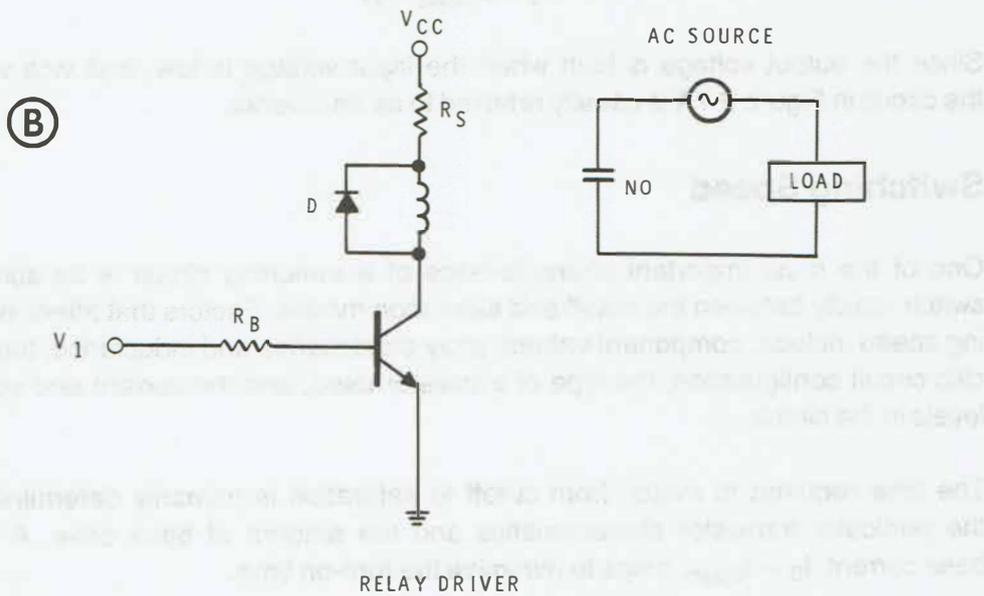
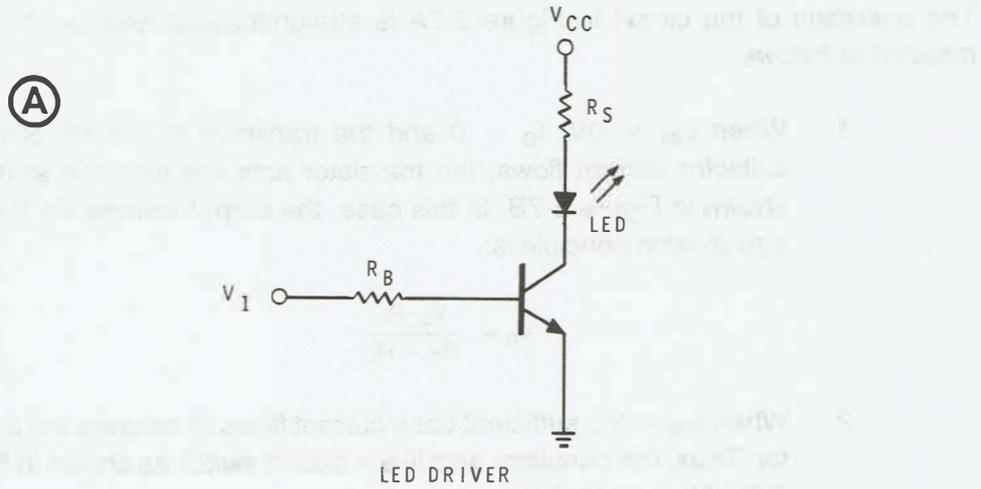


Figure 2-8

- Typical BJT switching applications.
- A. LED driver.
 - B. Relay driver.

The following examples illustrate how to design each circuit.

Example 2-4

Design an LED driver similar to the one shown in Figure 2-8A. The LED has a forward voltage drop of 2V, and requires approximately 35mA to obtain normal brilliance. The transistor used for the design is a type MPS-A20 BJT, whose minimum value of h_{FE} is 40. The DC supply voltage, V_{CC} , is 12V. The input voltage, V_1 , that should light the LED is 5V.

The design involves selecting appropriate values for R_S and R_B . Since the LED voltage drop, 2V, is less than the DC supply voltage, 12V, R_S serves as a series dropping resistor. The function of R_B is to ensure that sufficient base current flows to produce saturation when $V_1 = 5V$.

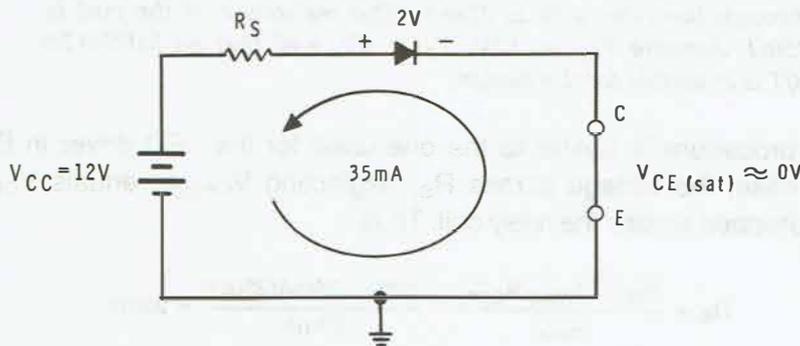


Figure 2-9

Equivalent circuit when $V_1 = 5V$ for Example 2-4.

Assuming $V_1 = 5V$, the transistor is saturated. Consequently, when viewed from the collector-emitter terminals, the circuit appears as shown in Figure 2-9. Here, the voltage across R_S equals the supply voltage minus the voltage across the LED and transistor. Assuming $V_{CE(sat)}$ is negligible, you can calculate R_S via Ohm's law as follows:

$$R_S = \frac{V_{CC} - V_{LED}}{I_{C(sat)}} = \frac{12V - 2V}{35mA} = 285.7\Omega$$

A standard value 270 Ω resistor is acceptable. In order to produce saturation, I_B must at least equal $I_{B(sat)}$ when $V_1 = 5V$. To ensure that saturation occurs under "worst case" conditions, we will select R_B so that:

$$I_B = 2 I_{B(sat)} = \frac{2 I_{C(sat)}}{h_{FE(min)}}$$

Thus, the required value of I_B is:

$$I_B = \frac{2(35\text{mA})}{40} = 1.75\text{mA}$$

Therefore, the required value of R_B is:

$$R_B = \frac{V_1 - V_{BE}}{I_B} = \frac{5\text{V} - 0.7\text{V}}{1.75\text{mA}} = 2.46\text{k}\Omega$$

A standard value $2.2\text{k}\Omega$ resistor is acceptable.

Example 2-5

Design a relay driver similar to the one shown in Figure 2-8B. The normally open, N.O., relay contacts close when the current through the relay coil is 25mA . The resistance of the coil is 250Ω . Assume $V_{CC} = 12\text{V}$, $V_1 = 5\text{V}$, and that an MPS-A20 BJT is available for the design.

The design procedure is similar to the one used for the LED driver in Example 2-4. In this case, the voltage across R_S , neglecting $V_{CE(\text{sat})}$, equals V_{CC} minus the voltage dropped across the relay coil. Thus:

$$R_S = \frac{V_{CC} - I_{C(\text{sat})} R_{\text{COIL}}}{I_{C(\text{sat})}} = \frac{12\text{V} - 25\text{mA}(250\Omega)}{25\text{mA}} = 230\Omega$$

A standard value 220Ω resistor is acceptable.

The required value of I_B is:

$$I_B = \frac{2 I_{C(\text{sat})}}{h_{FE(\text{min})}} = \frac{2(25\text{mA})}{40} = 1.25\text{mA}$$

Therefore, the required value of R_B is:

$$R_B = \frac{V_1 - V_{BE}}{I_B} = \frac{5\text{V} - 0.7\text{V}}{1.25\text{mA}} = 3.44\text{k}\Omega$$

A standard value $3.3\text{k}\Omega$ is acceptable.

By using a transistor switch and relay, you can control a large amount of AC power with a small amount of DC power. For this reason, relay drivers are frequently used in industrial control circuits.

Incidentally, the diode in Figure 2-8B is used to suppress arcing across the relay when the transistor switches from the saturated to the cutoff mode. From your knowledge of passive circuit design, recall that a diode is selected so that:

1. The diodes PIV rating $\geq 2 V_{CC}$.
2. The diodes peak current rating $> \frac{V_{CC}}{R_S + R_{COIL}}$

Due to their excellent switching characteristics, Schottky barrier-type diodes are often used in arc suppression circuits.

Limitations Of Base Bias

To illustrate why base bias is not very well suited for linear transistor circuits, we will illustrate the design and subsequent analysis of a typical circuit. The circuit to be designed should satisfy the following requirements:

1. Operate from a 10V DC supply voltage.
2. Provide a DC operating point for typical values of h_{FE} such that:

$$\begin{aligned} I_{CQ} &= 1\text{mA} \\ V_{CEQ} &= 5\text{V} \end{aligned}$$

The transistor available for the design is a general purpose, silicon, NPN-type. For this type transistor, the minimum, typical, and maximum values of h_{FE} are 50, 150, and 300 respectively.

The circuit we wish to design is illustrated in Figure 2-10A. You can find the required value of R_C by solving the following equation:

$$V_{CE} = V_{CC} - I_C R_C$$

$$I_C R_C = V_{CC} - V_{CE}$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C}$$

Substituting the desired Q point, value of I_C , and value of V_{CE} into Equation 2-9 yields:

$$R_C = \frac{10\text{V} - 5\text{V}}{1\text{mA}} = 5\text{k}\Omega$$

Assuming a typical value of h_{FE} , 150, the required base current is:

$$I_B = \frac{I_C}{h_{FE}} = \frac{1\text{mA}}{150} = 6.7\mu\text{A}$$

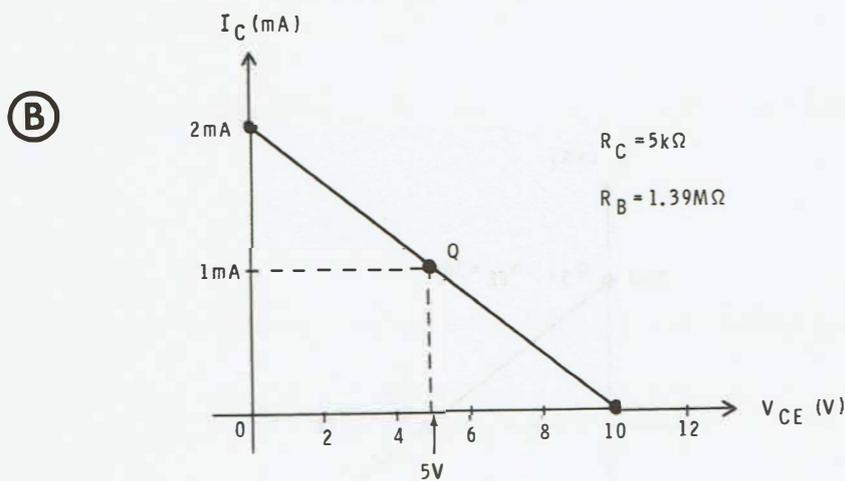
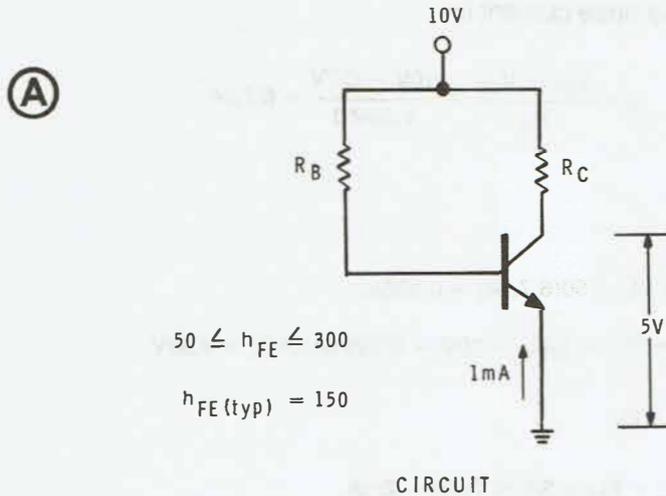
Therefore, the required value for R_B is:

$$R_B = \frac{V_{BB} - V_{BE}}{I_B} = \frac{10\text{V} - 0.7\text{V}}{6.67\mu\text{A}} = 1.39\text{M}\Omega$$

The DC load line for the circuit, indicating the operating point when $h_{FE} = 150$, is shown in Figure 2-10B. Note that the intercept values are:

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{10V}{5k\Omega} = 2mA$$

$$V_{CE(out)} = V_{CC} = 10V$$



DC LOAD LINE INDICATING THE Q POINT WHEN $h_{FE} = 150$

Figure 2-10

Circuit and DC load line for the design problem discussed in the text.

- A. Circuit.
- B. DC load line indicating the Q point when $h_{FE} = 150$.

The value of R_B is selected for our design on the assumption that the transistor has a typical value of h_{FE} . If this is the case, the actual values of I_C and V_{CE} will be very close to 1 mA and 5V respectively.

However, for a given transistor, the actual value of h_{FE} can be as low as 50 or as high as 300. For this reason, we need to examine what happens if the transistor has a minimum (50) or maximum (300) value of h_{FE} .

For any value of h_{FE} , the base current is:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10V - 0.7V}{1.39M\Omega} = 6.7\mu A$$

Thus when $h_{FE} = 50$.

$$I_C = \beta I_B = 50(6.7\mu A) = 0.335\text{mA}$$

$$V_C = V_{CC} - I_C R_C = 10V - 0.335\text{mA}(5k\Omega) = 8.32V$$

Similarly, when $h_{FE} = 300$.

$$I_C = \beta I_B = 300(6.7\mu A) = 2\text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 10V - 2\text{mA}(5k\Omega) = 0V$$

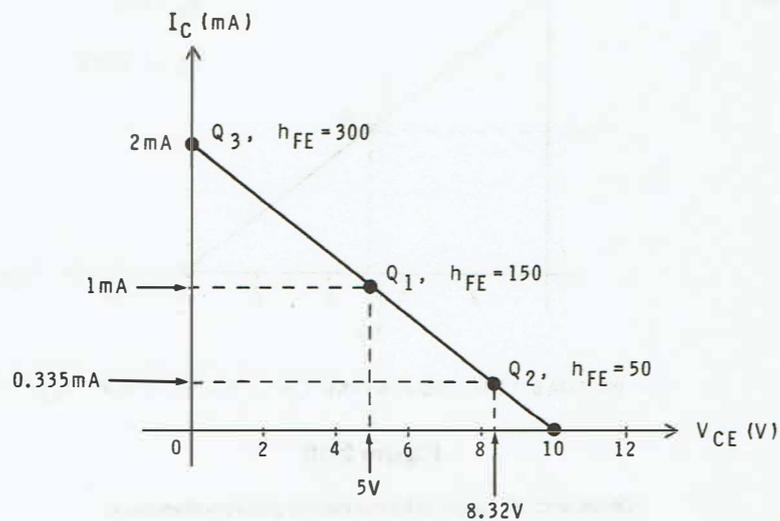


Figure 2-11

Possible operating points for the design problem discussed in the text.

Clearly, variations in B between 50 and 300 produce **drastic** changes in the operating point of the base bias circuit in Figure 2-10A. This is illustrated by the possible operating points shown in Figure 2-11. Note that:

1. When $h_{FE} = 150$, the operating point, Q_1 , is in the middle of the load line.
2. When $h_{FE} = 50$, the operating point, Q_2 , is on the lower end of the load line. For small values of h_{FE} , you can see that the operating point moves closer to cutoff.
3. When $h_{FE} = 300$, the operating point, Q_3 , corresponds to saturation.

Therefore, merely by changing transistors, you can make drastic changes in the operating point of a base bias circuit. This is the reason why base bias is not normally used in linear transistor circuits. In addition, since h_{FE} is highly temperature dependent, for a given transistor the actual Q point will vary widely with temperature.

Self-Test Review

Refer to Figure 2-12 for questions 1 through 4. Use approximate formulas when possible.

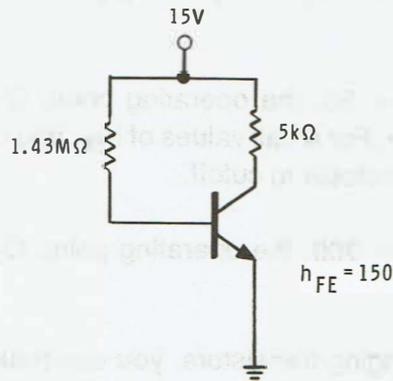


Figure 2-12

Circuit for Self-Test Review questions 1-4.

1. The intercepts of the DC load line are $I_{C(sat)} = \underline{\hspace{2cm}} \text{mA}$, and $V_{CE(cut)} = \underline{\hspace{2cm}} \text{V}$.
2. In the active mode, the collector-to-emitter voltage equals $\underline{\hspace{2cm}} \text{V}$.
3. Assuming the transistor is replaced with one whose $h_{FE} = 320$, the collector current is $\underline{\hspace{2cm}} \text{mA}$.
4. Assuming $h_{FE} = 150$, the value of R_B that just causes the transistor to saturate is $\underline{\hspace{2cm}} \text{k}\Omega$.

Refer to Figure 2-13 for questions 5 through 8.

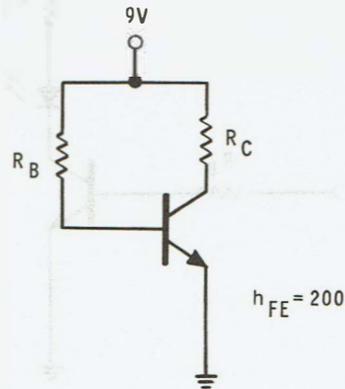


Figure 2-13

Circuit for Self-Test Review questions 5-8.

5. $I_{CQ} = 4\text{mA}$ and $V_{CEQ} = 5\text{V}$. The required value for R_C is therefore _____ $\text{k}\Omega$.
6. Assuming $h_{FE} = 200$, the required value of R_B is _____ $\text{k}\Omega$.
7. The power dissipated by a BJT under quiescent conditions is given by:

$$P_{DQ} = V_{CEQ}I_{CQ} \quad (\text{Eq. 2-10})$$

Therefore, the power dissipated by the transistor in Figure 2-13 is _____ mW .

8. The data sheet for the transistor in Figure 2-13 lists $V_{CE(\text{sat})} = 0.2\text{V}$ and $I_{CEO} = 0.01\mu\text{A}$. By using the Equation 2-10, you can calculate the power dissipated by the transistor for the saturated and cutoff modes. Consequently, $P_{D(\text{sat})}$ _____ mW , and $P_{D(\text{cut})}$ _____ μW .

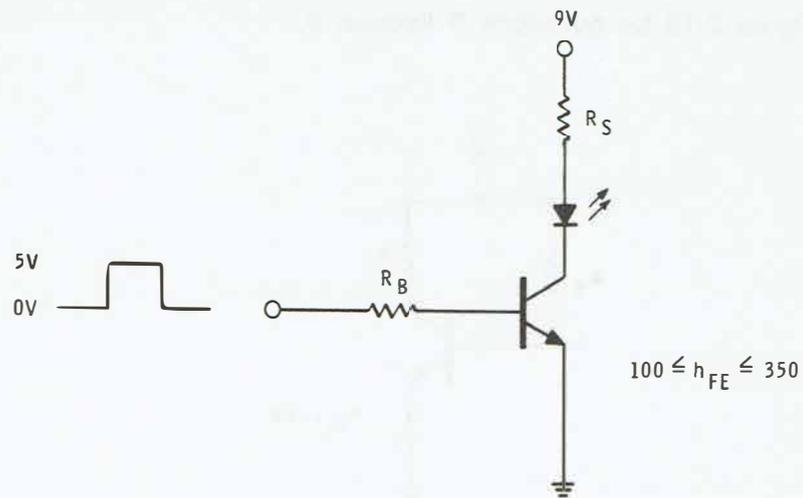


Figure 2-14

Circuit for Self-Test Review questions 9 and 10.

Refer to Figure 2-14 for questions 9 and 10.

9. The LED provides normal brilliance when the current through it is approximately 20mA. Under these conditions, the voltage drop across the LED is 1.7V. Assuming $V_{CE(sat)}$ is negligible, R_S should equal _____ Ω .
10. A reasonable value for R_B is _____ k Ω .

Answers

- | | |
|------------------|------------------------|
| 1. 3mA, 15V | 6. 415k Ω |
| 2. 7.5V | 7. 20mW |
| 3. 3mA | 8. 1.8mW, 0.09 μ W |
| 4. 715k Ω | 9. 365 Ω |
| 5. 1k Ω | 10. 10.75k Ω |

The solutions to questions 1-10 follow:

$$1. \quad I_{C(\text{sat})} = \frac{V_{CC}}{R_C} = \frac{15V}{5k\Omega} = 3mA$$

$$V_{CE(\text{cut})} = V_{CC} = 15V$$

2. To calculate V_{CE} , you must first determine the values of I_B and I_C . Thus:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{15V - 0.7V}{1.43M\Omega} = 10\mu A$$

$$I_C = \beta I_B = 150(10\mu A) = 1.5mA$$

Since $V_{CE} = V_{CC} - I_C R_C$, we have:

$$V_{CE} = 15V - 1.5mA(5k\Omega)$$

$$V_{CE} = 15V - 7.5V = 7.5V$$

3. Since $I_B = 10\mu\text{A}$ and $h_{FE} = 320$, we have:

$$I_C = 320(10\mu\text{A}) = 3.2\text{mA}$$

The calculated value of I_C is larger than $I_{C(\text{sat})}$. This tells you that the transistor is saturated. Since $I_{C(\text{sat})}$ is the maximum possible DC collector current, $I_C = I_{C(\text{sat})}$ or 3mA when $h_{FE} = 320$.

4. Since $I_C = I_{C(\text{sat})}$ or 3mA, and $h_{FE} = 150$, the base current required to just produce saturation is:

$$I_{B(\text{sat})} = \frac{I_{C(\text{sat})}}{h_{FE}} = \frac{3\text{mA}}{150} = 20\mu\text{A}$$

The required value of R_B is therefore:

$$R_B = \frac{V_{BB} - V_{BE}}{I_{B(\text{sat})}} = \frac{15\text{V} - 0.7\text{V}}{20\mu\text{A}} = 715\text{k}\Omega$$

5. $R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{9\text{V} - 5\text{V}}{4\text{mA}} = 1\text{k}\Omega$

6. Since $I_C = 4\text{mA}$ and $h_{FE} = 200$, the base current, I_B , is:

$$I_B = \frac{I_C}{h_{FE}} = \frac{4\text{mA}}{200} = 20\mu\text{A}$$

Therefore, the required value of R_B is:

$$R_B = \frac{V_{BB} - V_{BE}}{I_B} = \frac{9\text{V} - 0.7\text{V}}{20\mu\text{A}} = 415\text{k}\Omega$$

7. $P_{DQ} = V_{CEQ}I_{CQ} = 5\text{V}(4\text{mA}) = 20\text{mW}$

8. When the transistor is saturated, $V_{CE} = V_{CE(\text{sat})}$ and $I_C = I_{C(\text{sat})}$. Since $V_{CC} = 9\text{V}$ and $R_C = 1\text{k}\Omega$, $I_{C(\text{sat})}$ is essentially 9mA. Thus:

$$P_{D(\text{sat})} = V_{CE(\text{sat})}I_{C(\text{sat})} = 0.2\text{V}(9\text{mA}) = 1.8\text{mW}$$

When the transistor is cutoff, $I_C = I_{C(\text{EO})}$ and $V_{CE} \approx V_{CC}$ or 9V. Thus:

$$P_{D(\text{cut})} = V_{CE(\text{cut})}I_{C(\text{EO})} = 9\text{V}(0.01\mu\text{A}) = 0.09\mu\text{W}$$

Note that a transistor that is at saturation or cutoff dissipates very little power.

9.
$$R_S = \frac{V_{CC} - V_{LED}}{I_{C(sat)}} = \frac{9V - 1.7V}{20mA} = 365\Omega$$

10. In order to ensure that saturation occurs under worst case conditions, R_B is chosen so that:

$$I_B = \frac{2 I_{C(sat)}}{h_{FE(min)}} = \frac{2(20mA)}{100} = 0.4mA$$

Consequently, the required value of R_B is:

$$R_B = \frac{V_1 - V_{BE}}{I_B} = \frac{5V - 0.7V}{0.4mA} = 10.75k\Omega$$

In practice, standard value resistors close to the calculated values would be used for the design.

QUASI-STABLE BIASING SCHEMES

In linear transistor circuits, the biasing scheme must accomplish two things. First, the desired operating point must be established. Second, once established, the operating point must be stabilized against temperature changes and unit-to-unit variations in h_{FE} . In this section, you will examine a number of biasing schemes that are somewhat more stable than the base bias scheme discussed previously.

Emitter Feedback

A single-supply, base-bias circuit that uses emitter feedback is illustrated in Figure 2-15A. To emphasize the base and collector loops, the circuit can be redrawn as shown in Figure 2-15B. By starting at point A and going counterclockwise around the base loop, you obtain:

$$-V_{CC} + I_B R_B + V_{BE} + I_E R_E = 0 \quad (\text{loop 1})$$

Since $I_C = \beta I_B$ and I_E is approximately equal to I_C , it follows that I_E is approximately equal to βI_B . Thus, substituting βI_B for I_E in the base loop equation yields:

$$-V_{CC} + I_B R_B + V_{BE} + \beta I_B R_E = 0$$

Solving for the base current, I_B , you obtain:

$$I_B R_B + \beta I_B R_E = V_{CC} - V_{BE}$$

$$I_B [R_B + \beta R_E] = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_E} \quad (\text{Eq. 2-11})$$

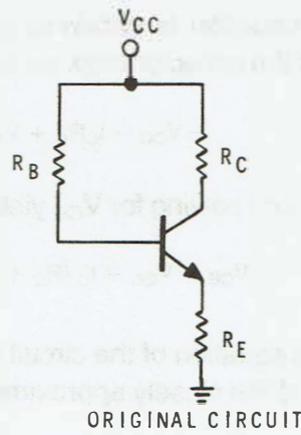
Also, since I_C equals βI_B , we have:

$$I_C = \frac{\beta (V_{CC} - V_{BE})}{R_B + \beta R_E}$$

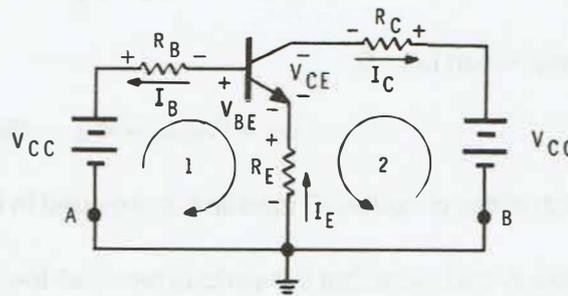
Dividing numerator and denominator by β yields:

$$I_C = \frac{V_{CC} - V_{BE}}{R_E + \frac{R_B}{\beta}} \approx I_E \quad (\text{Eq. 2-12})$$

(A)



(B)



(C)

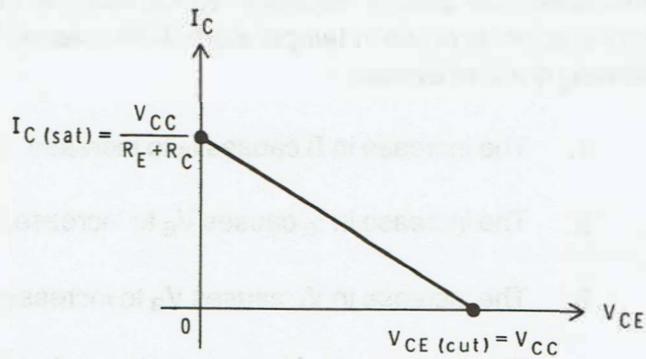


Figure 2-15

A base bias circuit which uses emitter feedback.

- A. Original circuit.
- B. Redrawing the circuit.
- C. DC load line.

The collector loop equation is obtained by starting at point B and going counterclockwise around the collector loop, as follows:

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0$$

Substituting I_C for I_E and solving for V_{CE} yields:

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \quad (\text{Eq. 2-13})$$

Equation 2-13 is the equation of the circuit's DC load line. Recall that the intercept values of the DC load line closely approximate $I_{C(\text{sat})}$ and $V_{CE(\text{cut})}$. Thus:

When $V_{CE} = 0$

$$I_C = I_{C(\text{sat})} = \frac{V_{CC}}{R_C + R_E} \quad (\text{Eq. 2-14})$$

Similarly, when $I_C = 0$:

$$V_{CE} = V_{CE(\text{cut})} = V_{CC} \quad (\text{Eq. 2-15})$$

A sketch of the circuit's DC load line is provided in Figure 2-15C.

In Figure 2-15B, note that the various terminal-to-ground voltages are as follows:

$$V_E = I_E R_E \approx I_C R_E$$

$$V_B = V_{BE} + V_E$$

$$V_C = V_{CC} - I_C R_C$$

To understand how emitter feedback works, assume that as a result of changing transistors, or an increase in temperature, β increases. This increase in β initiates the following chain of events.

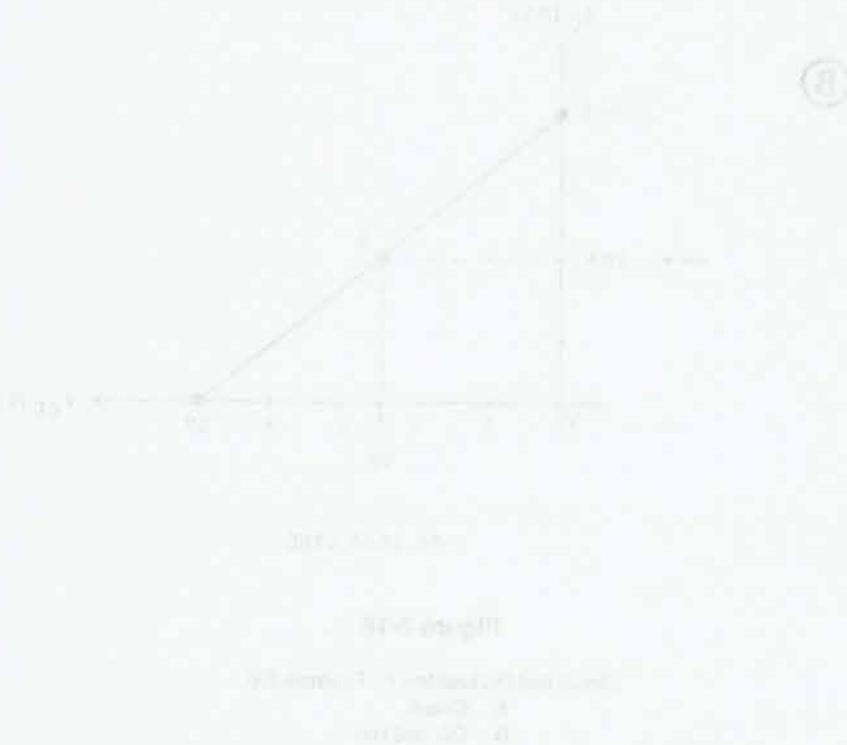
1. The increase in β causes I_E to increase.
2. The increase in I_E causes V_E to increase, since $V_E = I_E R_E$.
3. The increase in V_E causes V_B to increase, since $V_B = V_{BE} + V_E$.
4. The increase in V_B causes the voltage across R_B to decrease, since $V_{R_B} = V_{BB} - V_B$.
5. With less voltage across R_B , the base current must decrease, which tends to reduce I_E and I_C towards their original values.

By using the symbol \uparrow to mean "an increase in", \downarrow to mean "a decrease in", and the symbol \Rightarrow to mean "produce", we can summarize the sequence of events just described as follows:

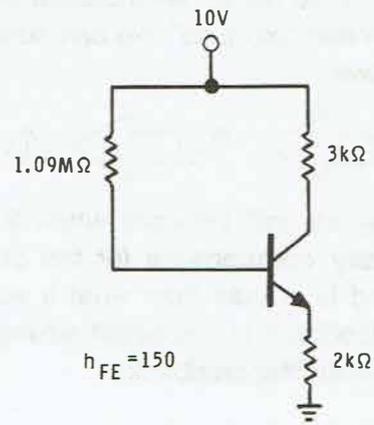


In practice, I_C and I_E will still increase when I_B increases since the decrease in I_B can only **partially compensate** for the original increase in I_B . However, the increase in I_C and I_E is **less** than what it would be if no feedback is used. Moreover, since the feedback in this circuit arrangement originates at the emitter, the circuit is said to use emitter feedback.

Incidentally, since this type of feedback opposes an increase in I_C and I_E , it is called **degenerative** feedback. This is true for any type of feedback that opposes amplifier gain.

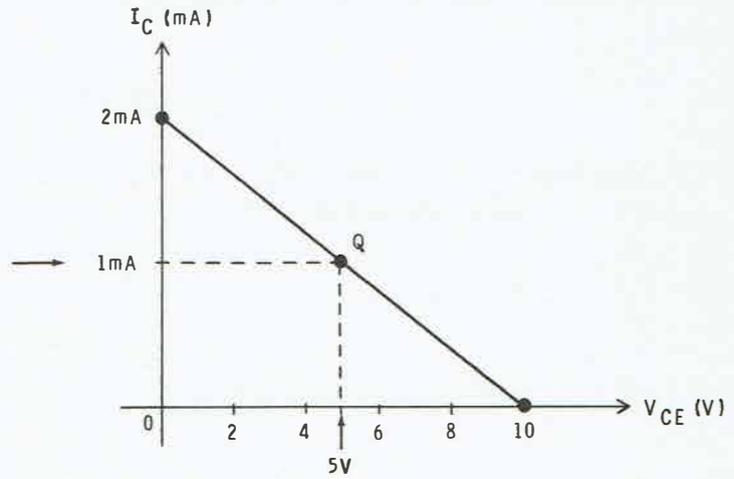


(A)



CIRCUIT

(B)



DC LOAD LINE

Figure 2-16

Circuit and DC load line for Example 2-6.

- A. Circuit.
- B. DC load line.

Example 2-6

Calculate the DC currents and voltages for the emitter feedback circuit in Figure 2-16.

$$I_B = \frac{V_{CC} - V_{BE}}{BR_E + R_B} = \frac{10V - 0.7V}{150(2k\Omega) + 1.09M\Omega} = \frac{9.3V}{1.39M\Omega} = 6.7\mu A$$

$$I_C = \beta I_B = 150(6.7\mu A) = 1mA \approx I_E$$

$$V_C = V_{CC} - I_C R_C = 10V - 1mA(3k\Omega) = 7V$$

$$V_E = I_E R_E \approx 1mA(2k\Omega) = 2V$$

$$V_B = V_{BE} + V_E = 0.7V + 2V = 2.7V$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E) = 10V - 1mA(3k\Omega + 2k\Omega) = 5V$$

Having calculated values of V_C and V_E previously, you could also calculate V_{CE} as follows:

$$V_{CE} = V_C - V_E = 7V - 2V = 5V$$

The DC load line for the circuit is sketched in Figure 2-16B. Here, values for $I_{C(sat)}$, and $V_{CE(cut)}$ were obtained as follows:

$$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E} = \frac{10V}{3k\Omega + 2k\Omega} = 2mA$$

$$V_{CE(cut)} = V_{CC} = 10V$$

Example 2-7

Illustrate how to design the circuit in Figure 2-16A. Prior to designing the circuit, the following information was known:

$$V_{CC} = 10V$$

$$h_{FE} = 150$$

The desired Q point is $I_{CQ} = 1mA$, and $V_{CEQ} = 5V$.

When you are designing a biasing scheme that uses emitter feedback, the first step is to select an appropriate value for the emitter to ground voltage V_E . As a guide, V_{EQ} is chosen so that it is between 10% and 20% of the DC supply voltage, V_{CC} . Once this is done, you can calculate values for R_E , R_C , and R_B as follows:

$$V_{EQ} = 20\% V_{CC} = 0.2(10V) = 2V$$

Since $I_{CQ} = 1mA \approx I_{EQ}$ we have:

$$R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{2V}{1mA} = 2k\Omega$$

The voltage across R_C equals V_{CC} minus the collector to ground voltage, V_C . Since $V_C = V_{CEQ} + V_{EQ}$ and the current through R_C is I_{CQ} , R_C can be calculated via Ohm's law. Thus:

$$R_C = \frac{V_{CC} - (V_{EQ} + V_{CEQ})}{I_{CQ}} = \frac{10V - (2V + 5V)}{1mA} = 3k\Omega$$

With $I_{CQ} = 1mA$ and $h_{FE} = 150$ the base current, I_{BQ} is:

$$I_{BQ} = \frac{1mA}{150} = 6.7\mu A$$

The voltage across R_B equals V_{CC} minus the base-to-ground voltage, V_B . Since $V_B = V_{BE} + V_E$, we have:

$$R_B = \frac{V_{CC} - (V_{BE} + V_E)}{I_{BQ}} = \frac{10V - (0.7V + 2V)}{6.7\mu A} = 1.09M\Omega$$

Observations

The only difference between the base bias and emitter feedback circuits is that the emitter feedback circuit employs an emitter resistor, R_E . Consequently, base bias may be considered a special case of emitter feedback where $R_E = 0$. For this reason, if you set $R_E = 0$ in the equations for the emitter feedback circuit, you obtain the equations, derived previously, for the base bias circuit. For example, the base current in an emitter feedback circuit is given by:

$$I_B = \frac{V_{BB} - V_{BE}}{BR_E + R_B} \quad (\text{emitter feedback})$$

Clearly, when $R_E = 0$, $I_B = \frac{V_{BB} - V_{BE}}{R_B}$, which is the formula for base bias circuit.

In circuit analysis, the ability to recognize that one circuit is a variation of another circuit is quite useful. For example, rather than independently analyzing two circuits, you can analyze the more general case and then derive the equations for the special case. Often this approach involves considerably less work than analyzing each circuit separately.

Collector Feedback

The circuit in Figure 2-17A is an example of **collector feedback**. As with emitter feedback, collector feedback provides a Q point that is slightly more stable than base bias.

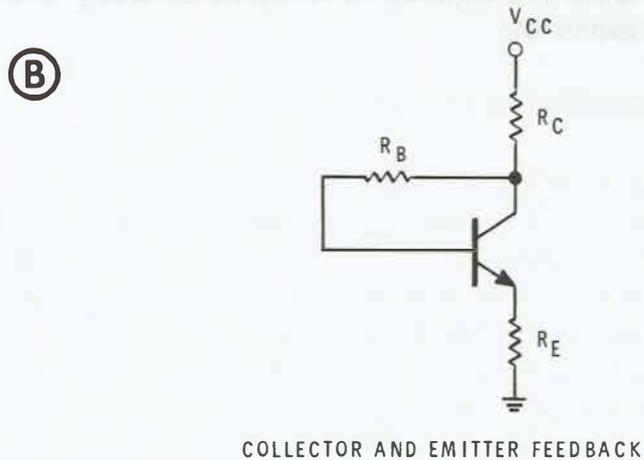
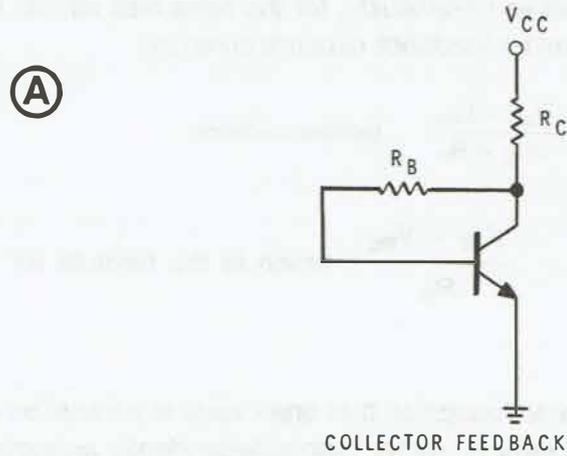


Figure 2-17

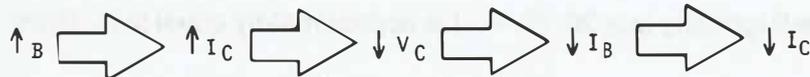
Biasing schemes utilizing collector feedback, and collector and emitter feedback.

- A. Collector feedback.
- B. Collector and emitter feedback.

To understand how collector feedback functions, assume that B increases. The increase in B initiates the following chain of events:

1. The increase in B causes I_C to increase.
2. The increase in I_C causes V_C to decrease, since $V_C = V_{CC} - I_C R_C$.
3. The decrease in V_C causes the voltage across R_B to decrease, since $V_{R_B} = V_C - V_{BE}$.
4. With less voltage across R_B , the base current must decrease, which tends to reduce I_E and I_C towards their original values.

Represented symbolically:



Since the feedback originates at the collector, the circuit in Figure 2-17A is said to use collector feedback. Again, this type of feedback can be called degenerative feedback.

Collector And Emitter Feedback

A circuit that uses **both** collector and emitter feedback is illustrated in Figure 2-17B. As you can see, the only difference between the collector feedback and the collector and emitter feedback circuit is that the collector and emitter feedback circuit uses an emitter resistor. Therefore, the collector feedback circuit is a special case of the collector and emitter feedback circuit. For this reason, we will first analyze the general case, collector and emitter feedback, and then derive formulas for the special case of just collector feedback.

Collector And Emitter Feedback Analysis

The collector and emitter feedback circuit in Figure 2-17B can be redrawn as shown in Figure 2-18A. Here, by starting at point A and following the indicated path around the outside loop, you obtain the following loop equation:

$$-V_{CC} + (I_B + I_C)R_C + I_B R_B + V_{BE} + I_E R_E = 0$$

Substituting BI_B for I_C and I_E yields:

$$(I_B + BI_B)R_C + I_B R_B + BI_B R_E = V_{CC} - V_{BE}$$

Factoring out the I_B term:

$$I_B [(B + 1)R_C + R_B + BR_E] = V_{CC} - V_{BE}$$

Since B typically is ≥ 20 , $(B + 1)$ is approximately equal to B . Thus:

$$I_B [BR_C + R_B + BR_E] = V_{CC} - V_{BE}$$

$$I_B [B(R_C + R_E) + R_B] = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{B(R_C + R_E) + R_B} \quad (\text{Eq. 2-15})$$

Since $I_C = BI_B$ we have:

$$I_C = \frac{B(V_{CC} - V_{BE})}{B(R_C + R_E) + R_B}$$

Dividing numerator and denominator by B yields:

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + R_E + \frac{R_B}{B}} \approx I_E \quad (\text{Eq. 2-16})$$

In Figure 2-18, the various terminal-to-ground voltages are as follows:

$$V_C = V_{CC} - I_C R_C$$

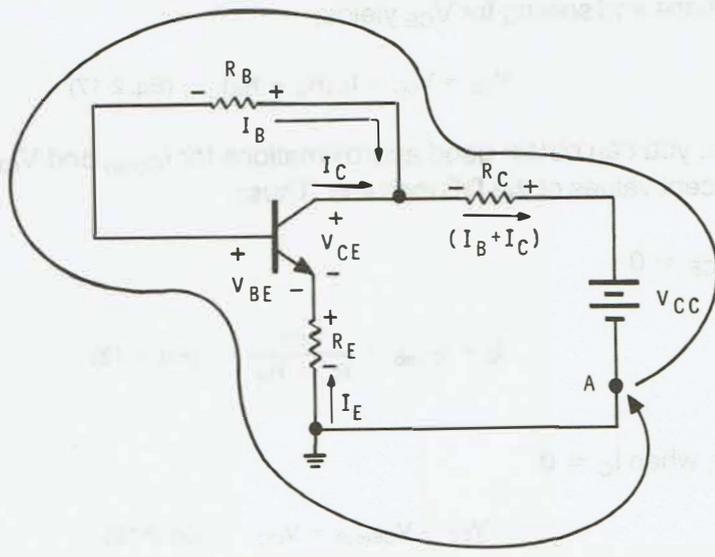
$$V_E = I_E R_E$$

$$V_B = V_{BE} + V_E$$

As with the circuit previously analyzed, the equation for the circuit's DC load line is obtained by writing a loop equation in the collector circuit. Referring to Figure 2-18B we have:

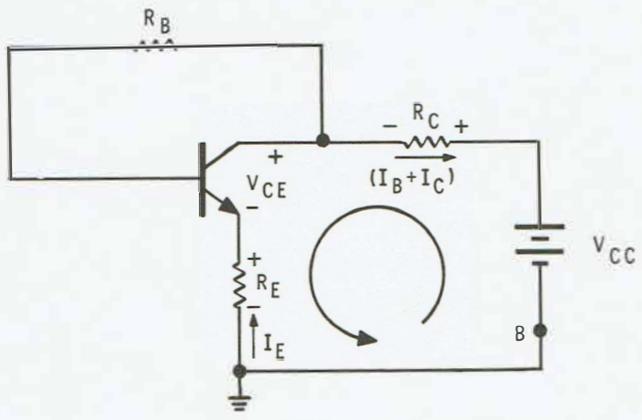
$$-V_{CC} + (I_B + I_C)R_C + V_{CE} + I_E R_E = 0$$

(A)



OUTSIDE LOOP

(B)



COLLECTOR LOOP

Figure 2-18

Outside and collector loops in the collector and emitter feedback circuits.
 A. Outside loop.
 B. Collector loop.

Since $I_C \gg I_B$, the expression $(I_B + I_C) \approx I_C$. Also, $I_E \approx I_C$. Making these substitutions and solving for V_{CE} yields:

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \quad (\text{Eq. 2-17})$$

As usual, you can obtain good approximations for $I_{C(\text{sat})}$ and $V_{CE(\text{sat})}$ by calculating the intercept values of the DC load line. Thus:

When $V_{CE} = 0$

$$I_C = I_{C(\text{sat})} = \frac{V_{CC}}{R_C + R_E} \quad (\text{Eq. 2-18})$$

Similarly, when $I_C = 0$

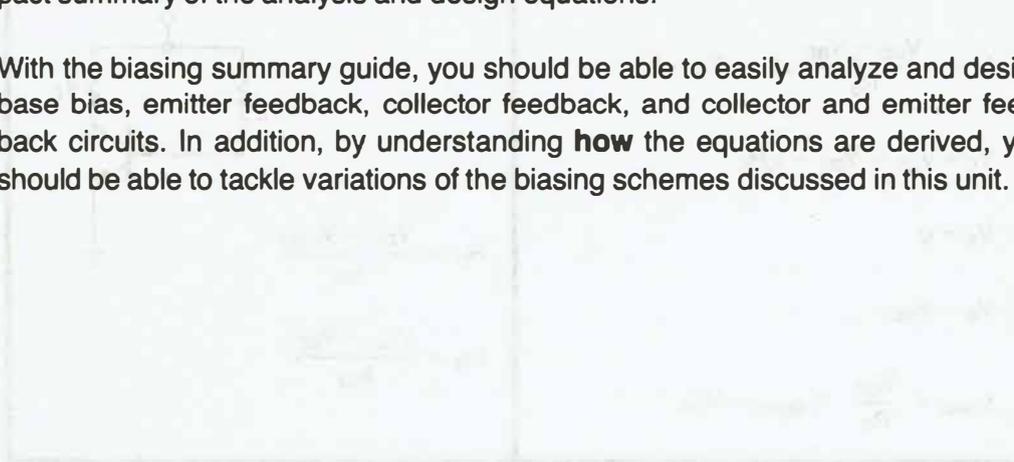
$$V_{CE} = V_{CE(\text{cut})} = V_{CC} \quad (\text{Eq. 2-19})$$

Recall that when $R_E = 0$ you have collector feedback. Therefore, by setting $R_E = 0$ in the various equations just derived, you will obtain the formulas that describe the DC currents and voltages in a collector feedback circuit.

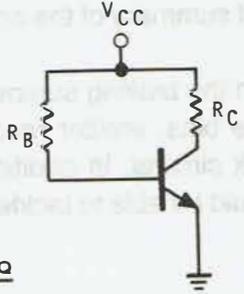
Setting It All Together

In this unit, our primary objective is to learn how to analyze and design a number of frequently encountered biassing schemes. The following section provides a compact summary of the analysis and design equations.

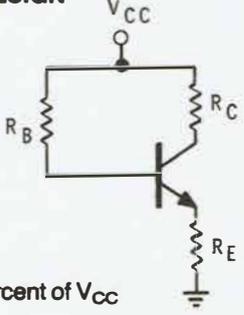
With the biassing summary guide, you should be able to easily analyze and design base bias, emitter feedback, collector feedback, and collector and emitter feedback circuits. In addition, by understanding **how** the equations are derived, you should be able to tackle variations of the biassing schemes discussed in this unit.



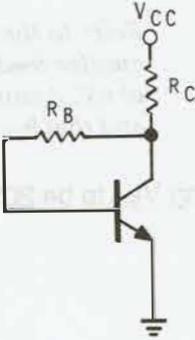
BIASING SUMMARY GUIDE

ANALYSIS	DESIGN
$I_B = \frac{V_{CC} - V_{BE}}{R_B}, I_C = \beta I_B \approx I_E$ $V_C = V_{CE} = V_{CC} - I_C R_C$ $V_E = 0$ $V_B = V_{BE}$ $I_{C(sat)} = \frac{V_{CC}}{R_C}, V_{CE(cut)} = V_{CC}$	 $R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}}$ $R_B = \frac{V_{CC} - V_{BE}}{I_{BQ}}$

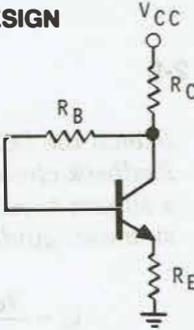
Base Bias

ANALYSIS	DESIGN
$I_B = \frac{V_{CC} - V_{BE}}{\beta R_E + R_B}$ $I_C = \frac{V_{CC} - V_{BE}}{R_E + R_{B/\beta}} \approx I_E$ $V_C = V_{CC} - I_C R_C, V_E = I_E R_E$ $V_B = V_{BE} + V_E$ $V_{CE} = V_{CC} - I_C (R_C + R_E)$ $I_{C(sat)} = \frac{V_{CC}}{R_C + R_E}, V_{CE(cut)} = V_{CC}$	 $V_{EQ} = 10 \text{ to } 20 \text{ percent of } V_{CC}$ $R_E = \frac{V_{EQ}}{I_{CQ}}$ $R_C = \frac{V_{CC} - (V_{EQ} + V_{CEQ})}{I_{CQ}}$ $R_B = \frac{V_{CC} - (V_{BE} + V_{EQ})}{I_{BQ}}$

Emitter Feedback

ANALYSIS	DESIGN
$I_B = \frac{V_{CC} - V_{BE}}{\beta R_C + R_E}$	
$I_C = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta}} = I_E$	$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}}$
$V_C = V_{CC} - I_C R_C, V_E = 0$	$R_B = \frac{V_{CEQ} - V_{BE}}{I_{BQ}}$
$V_B = V_{BE}$	
$V_{CE} = V_{CC} - I_C R_C$	
$I_{C(sat)} = \frac{V_{CC}}{R_C}, V_{CE(alt)} = V_{CC}$	

Collector Feedback

ANALYSIS	DESIGN
$I_B = \frac{V_{CC} - V_{BE}}{\beta(R_C + R_E) + R_B}$	
$I_C = \frac{V_{CC} - V_{BE}}{R_C + R_E + \frac{R_B}{\beta}} \approx I_E$	$V_{EQ} = 10 \text{ to } 20 \text{ percent of } V_{CC}$
$V_C = V_{CC} - I_C R_C, V_E = I_E R_E$	$R_E = \frac{V_{EQ}}{I_{CQ}}$
$V_B = V_{BE} + V_E$	$R_C = \frac{V_{CC} - (V_{EQ} + V_{CEQ})}{I_{CQ}}$
$V_{CE} = V_{CC} - I_C(R_C + R_E)$	$R_B = \frac{V_{CEQ} - V_{BE}}{I_{BQ}}$
$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E}, V_{CE(alt)} = V_{CC}$	

Collector and Emitter Feedback

Example 2-8

Refer to the biasing summary guide and design a collector and emitter feedback circuit to provide an I_{CQ} of 2mA and a V_{CEQ} of 6V. Assume that a 12V DC supply is available for the design, and that $h_{FE} = 200$.

Selecting V_{EQ} to be 20% of V_{CC} , we have:

$$V_{EQ} = 0.2(12V) = 2.4V$$

The various resistor values are calculated as follows:

$$R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{2.4V}{2mA} = 1.2k\Omega$$

$$R_C = \frac{V_{CC} - (V_{EQ} + V_{CEQ})}{I_{CQ}} = \frac{12V - (2.4V + 6V)}{2mA} = 1.8k\Omega$$

Since $I_{CQ} = 2mA$ and $h_{FE} = 200$, $I_{BQ} = 2mA/200$ or $10\mu A$. Thus:

$$R_B = \frac{V_{CEQ} - V_{BE}}{I_{BQ}} = \frac{6V - 0.7V}{10\mu A} = 530k\Omega$$

Example 2-9

Sketch the DC load line, and operating point for the collector feedback circuit in Figure 2-19A. Again, assume you are using a silicon transistor. Referring to the collector feedback biasing summary guide:

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{B}} = \frac{10V - 0.7V}{5k\Omega + \frac{645k\Omega}{150}} = \frac{9.3V}{9.3k\Omega} = 1mA$$

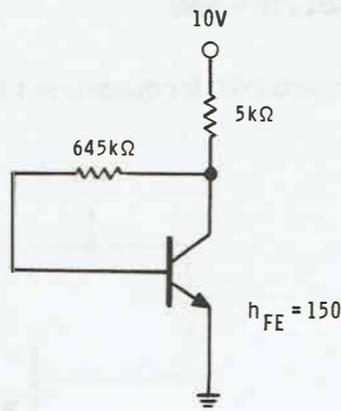
$$V_{CE} = V_{CC} - I_C R_C = 10V - 1mA(5k\Omega) = 5V$$

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{10V}{5k\Omega} = 2mA$$

$$V_{CE(cut)} = V_{CC} = 10V$$

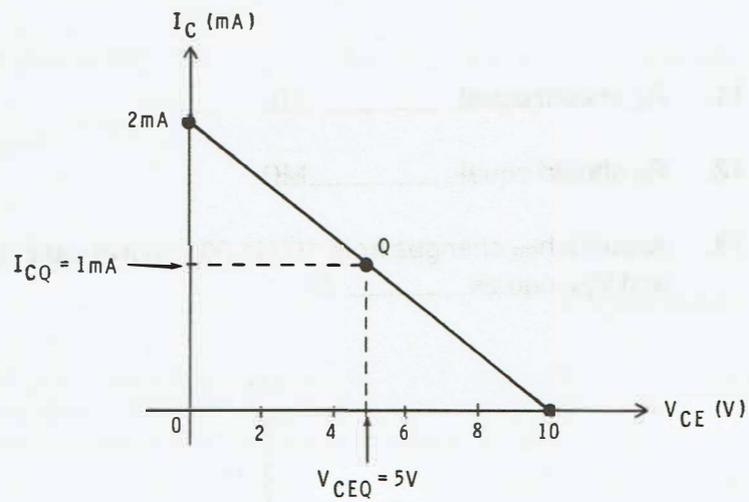
A sketch of the DC load line and operating point is provided in Figure 2-19B.

(A)



COLLECTOR FEEDBACK CIRCUIT

(B)



DC LOAD LINE

Figure 2-19

Circuit and DC load line for Example 2-9.

- A. Collector feedback circuit.
- B. DC load line.

Self-Test Review

Refer to Figure 2-20 for questions 11 through 13.

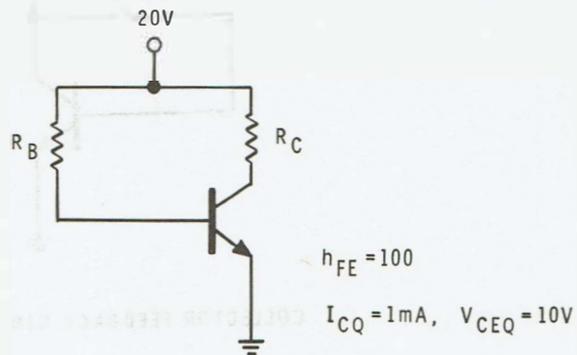


Figure 2-20

Circuit for Self-Test Review questions 11-13.

11. R_C should equal _____ $\text{k}\Omega$.
12. R_B should equal _____ $\text{M}\Omega$.
13. Assume h_{FE} changes from 100 to 200. In this case, I_C equals _____ mA and V_{CE} equals _____ V .

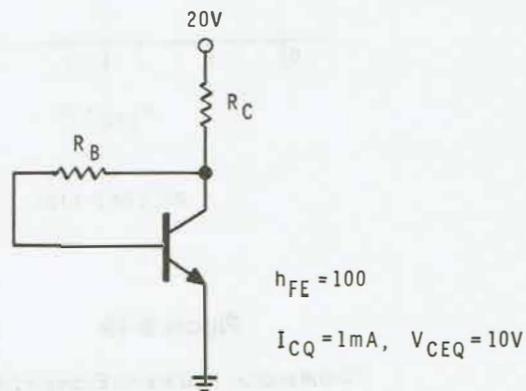


Figure 2-21

Circuit for Self-Test Review questions 14-16.

Refer to Figure 2-21 for questions 14 through 16.

14. R_C should equal _____ $k\Omega$.
15. R_B should equal _____ $k\Omega$.
16. If h_{FE} changes from 100 to 200 I_C would equal _____ mA and V_{CE} would equal _____ V.

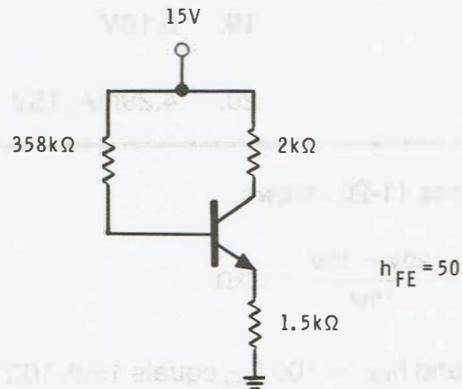


Figure 2-22

Circuit for Self-Test Review questions 17-20.

Refer to Figure 2-22 for questions 17 through 20.

17. The collector-to-ground voltage equals _____ V.
18. The emitter-to-ground voltage equals _____ V.
19. The base-to-ground voltage equals _____ V.
20. The values of $I_{C(\text{sat})}$ and $V_{CE(\text{cut})}$ are _____ mA and _____ V respectively.

ANSWERS

- | | |
|--------------------|------------------|
| 11. 10k Ω | 16. 1.32mA, 6.8V |
| 12. 1.93M Ω | 17. 11.7V |
| 13. 2mA, 0V | 18. 2.48V |
| 14. 10k Ω | 19. 3.18V |
| 15. 930k Ω | 20. 4.29mA, 15V |

The solutions to questions 11-20 follows:

$$11. R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{20V - 10V}{1mA} = 10k\Omega$$

12. Since $I_C = 1mA$ and $h_{FE} = 100$, I_{BQ} equals $1mA/100$ or $10\mu A$. Thus:

$$R_B = \frac{V_{CC} - V_{BE}}{I_{BQ}} = \frac{20V - 0.7V}{10\mu A} = 1.93M\Omega$$

13. When $h_{FE} = 200$:

$$I_C = \beta I_B = 200(10\mu A) = 2mA$$

$$V_{CE} = V_{CC} - I_C R_C = 20V - 2mA(10k\Omega) = 0V$$

Since $V_{CE} = 0V$, the transistor is saturated.

$$14. R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{20V - 10V}{1mA} = 10k\Omega$$

15. Since $I_C = 1mA$ and $h_{FE} = 100$, I_{BQ} equals $1mA/100$ or $10\mu A$. Thus:

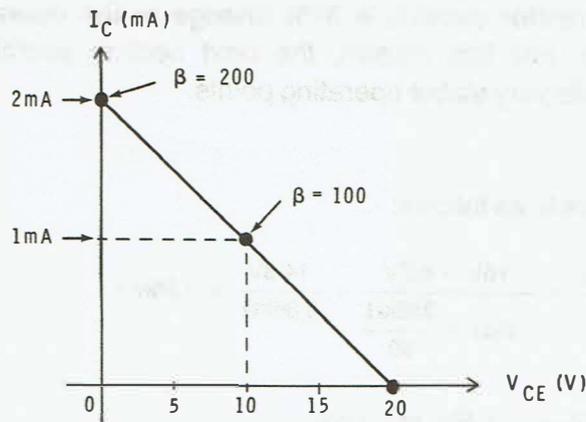
$$R_B = \frac{V_{CEQ} - V_{BE}}{I_{BQ}} = \frac{10V - 0.7V}{10\mu A} = 930k\Omega$$

16. When $h_{FE} = 200$:

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta}} = \frac{20V - 0.7V}{10k\Omega + \frac{930k\Omega}{200}} = \frac{19.3V}{14.65k\Omega} = 1.32mA$$

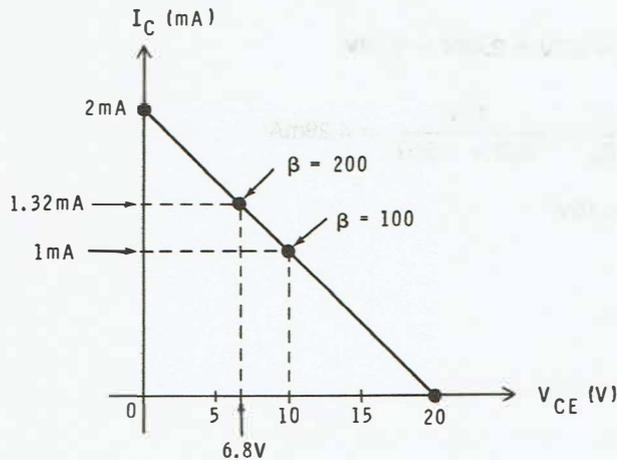
$$V = V_{CC} - I_C R_C = 20V - 1.32mA(10k\Omega) = 6.8V$$

(A)



LOAD LINE FOR THE CIRCUIT IN FIGURE 2-20

(B)



LOAD LINE FOR THE CIRCUIT IN FIGURE 2-21

Figure 2-23

Comparing the results obtained in questions 13 and 16.

- A. Load line for the circuit in Figure 2-20.
- B. Load line for the circuit in Figure 2-21.

Let's compare the results obtained in question 13 with those obtained in question 16. When B changed by 100% in the base bias circuit, question 13, I_C also changed by 100%. This caused the operating point to shift from the center of the load line to saturation, as shown in Figure 2-23A.

When B changed by 100% in the collector feedback circuit, question 16, the corresponding change in I_C was only 32%. This is a considerable improvement over the base bias circuit. Figure 2-23B indicates the shift in the operating point due to the increase in B . A comparison of the two load lines in Figure 2-23 illustrates the effectiveness of collector feedback.

In many linear transistor circuits, a 32% change in the operating point would not be acceptable. For this reason, the next section examines two biasing schemes that provide very stable operating points.

17. First, calculate I_C as follows:

$$I_C = \frac{V_{CC} - V_{BE}}{R_E + \frac{R_B}{\beta}} = \frac{15V - 0.7V}{1.5k\Omega + \frac{358k\Omega}{50}} = \frac{14.3V}{8.66k\Omega} = 1.65mA$$

Since $V_C = V_{CC} - I_C R_C$, we have:

$$V_C = 15V - 1.65mA(2k\Omega) = 11.7V$$

18. $V_E = I_E R_E = 1.65mA(1.5k\Omega) = 2.48V$

19. $V_B = V_{BE} + V_E = 0.7V + 2.48V = 3.18V$

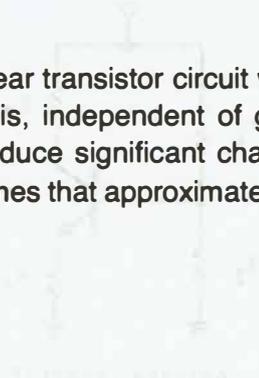
20. $I_{C(sat)} = \frac{V_{CC}}{R_C + R_E} = \frac{15V}{2k\Omega + 1.5k\Omega} = 4.29mA$

$$V_{CE(cut)} = V_{CC} = 15V$$

STABLE BIASING SCHEMES

In a base bias circuit, the percent change in I_C equals the percent change in B . By employing emitter feedback, collector feedback, or both emitter and collector feedback, the percent change in I_C will be less than the percent change in B . However, as you saw in the previous section, large changes in B still produce significant changes in I_C .

The ideal biasing scheme for a linear transistor circuit would provide an operating point that is B independent; that is, independent of gain. In other words, even large changes in B would not produce significant changes in I_C . In this section, you will examine two biasing schemes that approximate this ideal biasing scheme.



- 1. Base bias
- 2. Collector feedback
- 3. Emitter feedback
- 4. Collector-emitter feedback

Voltage Divider Bias

The circuit illustrated in Figure 2-24A is the most popular, single-supply, biasing scheme for discrete linear transistor circuits. Since resistors R_1 and R_2 form a simple voltage divider, the biasing scheme is referred to as voltage divider bias.

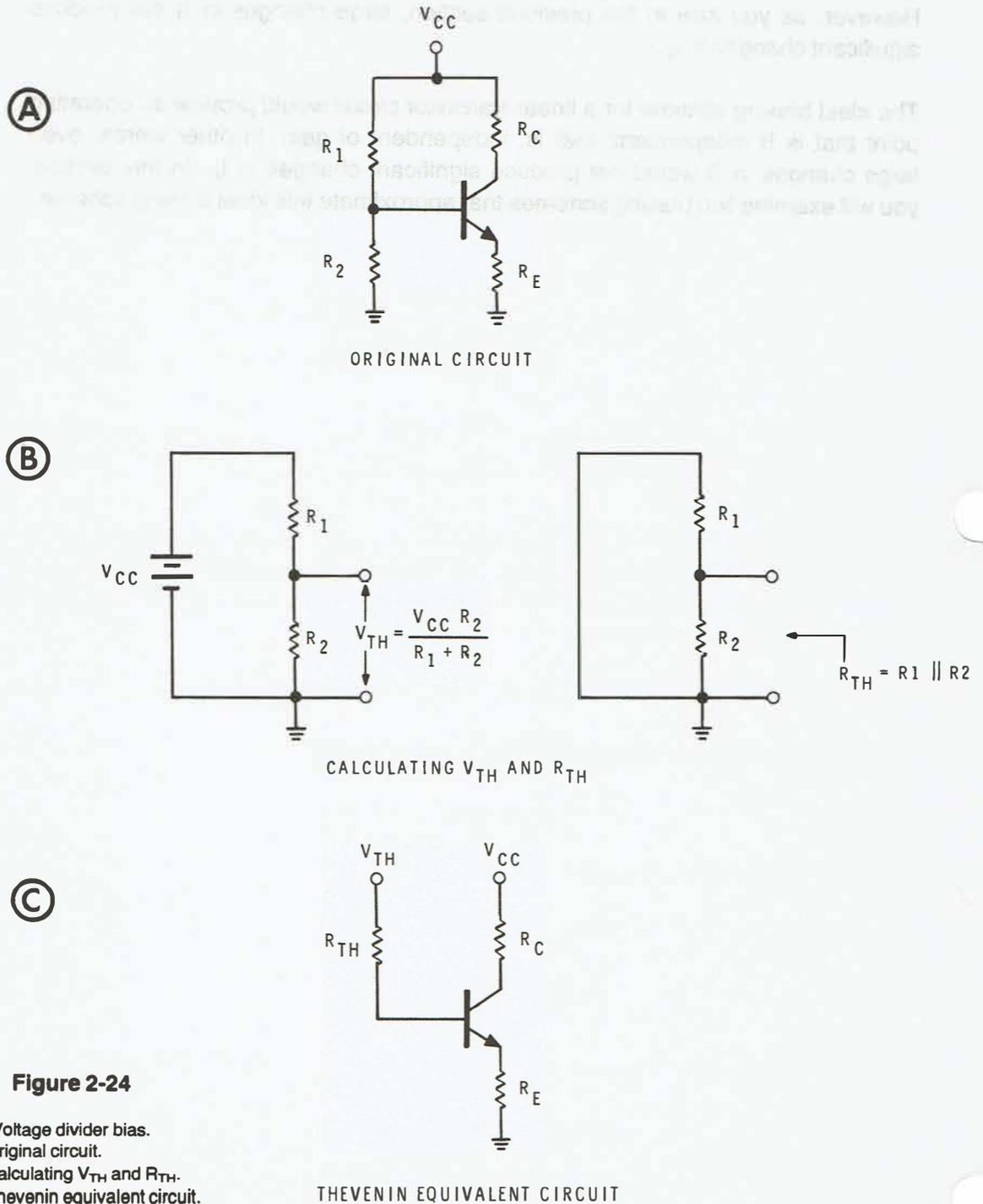


Figure 2-24

Voltage divider bias.

A. Original circuit.

B. Calculating V_{TH} and R_{TH} .

C. Thevenin equivalent circuit.

To analyze the circuit in Figure 2-24A, you begin by mentally opening the base lead. This permits you to apply Thevenin's theorem to the voltage divider as shown in Figure 2-24B. Here note that:

$$V_{TH} = \frac{V_{CC} R_2}{R_1 + R_2} \quad (\text{Eq. 2-20})$$

$$R_{TH} = R_1 \parallel R_2 \quad (\text{Eq. 2-21})$$

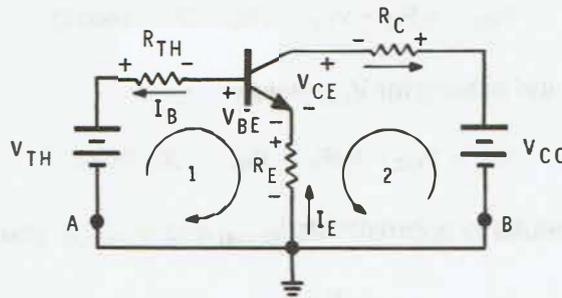


Figure 2-25

Redrawing the Thevenin equivalent circuit in Figure 2-24C.

The Thevenin equivalent circuit is illustrated in Figure 2-24C. In order to emphasize the base and collector loops, the Thevenin equivalent circuit can be redrawn as shown in Figure 2-25. Here, by starting at point A and going clockwise around the base loop, you obtain:

$$-V_{TH} + I_B R_{TH} + V_{BE} + I_E R_E = 0 \quad (\text{loop 1})$$

Substituting the approximate relationship $B I_B$ for I_E yields:

$$-V_{TH} + I_B R_{TH} + V_{BE} + B I_B R_E = 0$$

Solving for the base current, I_B you obtain:

$$I_B (B R_E + R_{TH}) = V_{TH} - V_{BE}$$

$$I_B = \frac{V_{TH} - V_{BE}}{B R_E + R_{TH}} \quad (\text{Eq. 2-22})$$

Since $I_C = B I_B$ we have:

$$I_C = B I_B = \frac{B(V_{TH} - V_{BE})}{B R_E + R_{TH}}$$

Dividing numerator and denominator by B yields:

$$I_C = \frac{V_{TH} - V_{BE}}{R_E + \frac{R_{TH}}{B}} \approx I_E \quad (\text{Eq. 2-23})$$

As usual, the equation for the circuit's DC load line is obtained through the collector loop equation. By starting at point B in Figure 2-25 and going counterclockwise, you obtain:

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0 \quad (\text{loop 2})$$

Substituting I_C for I_E and solving for V_{CE} yields:

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \quad (\text{Eq. 2-24})$$

Using the intercept values to approximate $I_{C(\text{sat})}$ and $V_{CE(\text{cut})}$, you have:

$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C + R_E} \quad (\text{Eq. 2-25})$$

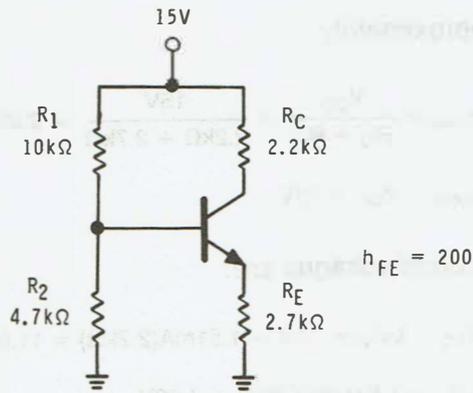
$$V_{CE(\text{cut})} = V_{CC} \quad (\text{Eq. 2-26})$$

Finally, the various terminal-to-ground voltages are:

$$V_C = V_{CC} - I_C R_C$$

$$V_E = I_E R_E$$

$$V_B = V_{BE} + V_E$$


Figure 2-26

Circuit for Example 2-10.

Example 2-10

Calculate the various DC currents and voltages for the circuit shown in Figure 2-26.

First calculate the Thevenin quantities:

$$V_{TH} = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{15V(4.7k\Omega)}{10k\Omega + 4.7k\Omega} = 4.8V$$

$$R_{TH} = R_1 \parallel R_2 = 10k\Omega \parallel 4.7k\Omega = 3.2k\Omega$$

Using these values, you obtain:

$$\begin{aligned} I_B &= \frac{V_{TH} - V_{BE}}{R_{TH} + R_E} = \frac{4.8V - 0.7V}{200(2.7k\Omega) + 3.2k\Omega} \\ &= \frac{4.1V}{543.2k\Omega} = 7.55\mu A \end{aligned}$$

Since $I_C = \beta I_B$, $I_C = 200(7.55\mu A) = 1.51mA \approx I_E$.

The collector-to-emitter voltage, V_{CE} equals:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$V_{CE} = 15V - 1.51mA(2.2k\Omega + 2.7k\Omega) = 7.6V$$

$I_{C(\text{sat})}$ and $V_{CE(\text{cut})}$ are approximately:

$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C + R_E} = \frac{15\text{V}}{2.2\text{k}\Omega + 2.7\text{k}\Omega} = 3.06\text{mA}$$

$$V_{CE(\text{cut})} = V_{CC} = 15\text{V}$$

Finally, the terminal-to-ground voltages are:

$$V_C = V_{CC} - I_C R_C = 15\text{V} - 1.51\text{mA}(2.2\text{k}\Omega) = 11.68\text{V}$$

$$V_E = I_E R_E = 1.51\text{mA}(2.7\text{k}\Omega) = 4.08\text{V}$$

$$V_B = V_{BE} + V_E = 0.7\text{V} + 4.08\text{V} = 4.78\text{V}$$

Example 2-11

Rework Example 2-10 assuming a 300% increase in the value of h_{FE} .

In this case, $h_{FE} = 600$. Therefore:

$$I_B = \frac{V_{TH} - V_{BE}}{BR_E + R_{TH}} = \frac{4.1\text{V}}{1\,622.2\text{k}\Omega} = 2.53\mu\text{A}$$

$$I_C = \beta I_B = 600(2.53\mu\text{A}) = 1.52\text{mA} \approx I_E$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$V_{CE} = 15\text{V} - 1.52\text{mA}(4.9\text{k}\Omega) = 7.55\text{V}$$

$$V_C = V_{CC} - I_C R_C = 15\text{V} - 1.52\text{mA}(2.2\text{k}\Omega) = 11.66\text{V}$$

$$V_E = I_E R_E = 1.52\text{mA}(2.7\text{k}\Omega) = 4.1\text{V}$$

$$V_B = V_{BE} + V_E = 0.7\text{V} + 4.1\text{V} = 4.8\text{V}$$

The values of $I_{C(sat)}$ and $V_{CE(cut)}$ are the same as in Example 2-11, since they do not depend upon the value of B . Table 2-2 compares the values of the DC currents and voltages for the two values of h_{FE} .

$h_{FE} (B)$	200	600
I_B	$7.55\mu A$	$2.53\mu A$
$I_C \approx I_E$	$1.51mA$	$1.52mA$
V_{CE}	$7.6V$	$7.55V$
V_C	$11.68V$	$11.66V$
V_E	$4.08V$	$4.1V$
V_B	$4.78V$	$4.8V$

TABLE 2-2

Comparing The Results Of Examples 2-10 And 2-11.

Table 2-2 indicates that even for a 300% change in B there is very little change in I_{CQ} and V_{CEQ} . Clearly, the operating point in Figure 2-26 is very stable with respect to variations in B .

Approximate Analysis

A commonly used rule of thumb for designing a voltage-divider bias circuit is to make R_2 equal to or less than ten times the value of R_E . This ensures that the equivalent resistance between the base of the transistor and ground is large compared to the value of R_2 , as shown in Figure 2-27. Assuming this is the case, the parallel combination of R_2 and $R_{IN(BASE)}$ approximately equals R_2 . For this reason, the voltage divider may be considered unloaded and the circuit quickly analyzed as follows:

Via voltage division, the base voltage, V_B , is:

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2} \quad (\text{Eq. 2-27})$$

Since $V_B = V_{BE} + V_E$ the emitter voltage, V_E is:

$$V_E = V_B - V_{BE}$$

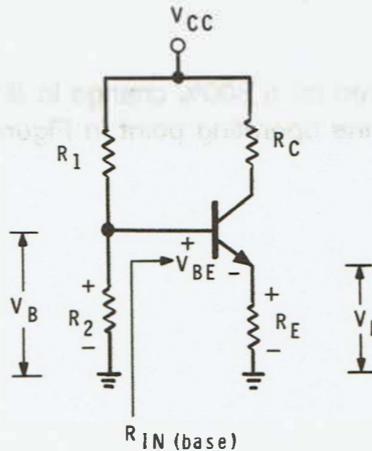


Figure 2-27

A voltage divider bias circuit where $R_{IN(BASE)} \gg R_2$.

Via Ohm's law, the emitter current, I_E , is:

$$I_E = \frac{V_E}{R_E} \approx I_C \quad (\text{Eq. 2-28})$$

By following the three-step procedure just presented, you can quickly estimate the value of the collector current, I_C , in a voltage-divider bias circuit. Once you know I_C , you can quickly calculate the other quantities as previously illustrated.

Example 2-12

Use the three-step procedure to analyze the circuit in Figure 2-26.

$$V_B = V_{R_2} = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{15V (4.7k\Omega)}{10k\Omega + 4.7k\Omega} = 4.8V$$

$$V_E = V_B - V_{BE} = 4.8V - 0.7V = 4.1V$$

$$I_E = \frac{V_E}{R_E} = \frac{4.1V}{2.7k\Omega} = 1.52mA \approx I_C$$

Assuming $\beta = 200$

$$I_B = \frac{1.52mA}{200} = 7.6\mu A$$

With $I_C = 1.52mA$

$$V_C = V_{CC} - I_C R_C = 15V - 1.52mA(2.2k\Omega) = 11.66V$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$V_{CE} = 15V - 1.52mA(2.2k\Omega + 2.7k\Omega) = 7.55V$$

Comparing the approximate answers with those obtained in Example 2-10 indicates that the simple three-step procedure is quite accurate. For this reason, you should use the three-step method to analyze voltage-divider bias circuits.

To explain why the Q point in a voltage-divider bias circuit is stable, we will first consider why the Q point is unstable in a base bias circuit.

Recall that in a base bias circuit that the value of I_B is fixed by the values of the DC supply voltage and R_B . Since I_B is constant, I_C automatically assumes the value dictated by the formula $I_C = \beta I_B$. Consequently, I_C is directly proportional to β . This results in a very unstable Q point.

In a voltage-divider bias circuit just the opposite happens. In this case, the base voltage, V_B , is fixed by the DC supply voltage and the ratio of R_1 to R_2 in the voltage divider. Since $V_E = V_B - V_{BE}$, the emitter voltage, V_E , is essentially constant. A constant emitter voltage produces a constant emitter and collector current. Since I_C is constant, I_B automatically assumes the value dictated by the formulas $I_B = I_C/\beta$. For this reason, I_C is largely independent of the value of β . The result is a very stable Q point.

Example 2-13

Design a voltage-divider bias circuit to provide an I_{CQ} of 2mA, and a V_{CEQ} of 10V. Assume a 20VDC supply voltage is available for the design.

As a guide, V_{EQ} is chosen so that it is between 20% and 30% of the DC supply voltage, V_{CC} . Once this is done, you can calculate appropriate resistance values as follows:

$$V_{EQ} = 30\% V_{CC} = 0.3(20V) = 6V$$

Since $I_{CQ} = 2mA \approx I_{EQ}$ we have:

$$R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{6V}{2mA} = 3k\Omega$$

Via Ohm's law the required value of R_C is:

$$R_C = \frac{V_{CC} - (V_{EQ} + V_{CEQ})}{I_{CQ}} = \frac{20V - (6V + 10V)}{2mA} = 2k\Omega$$

As mentioned previously, the value of R_2 is chosen so that:

$$R_2 \leq 10R_E$$

Selecting $R_2 = 10R_E$ yields:

$$R_2 = 10R_E = 10(3k\Omega) = 30k\Omega$$

Since $V_{EQ} = 6V$ the required base voltage, V_B , is:

$$V_B = V_{EQ} + V_{BE} = 6V + 0.7V = 6.7V$$

Recall that $V_B = \frac{V_{CC} R_2}{R_1 + R_2}$. Solving this equation for R_1 yields:

$$R_1 = \frac{R_2(V_{CC} - V_B)}{V_B}$$

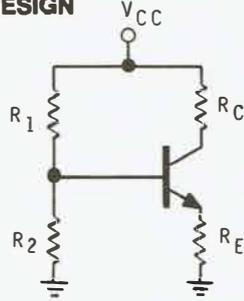
Therefore, in this case:

$$R_1 = \frac{30k\Omega(20V - 6.7V)}{6.7V} = 59.5k\Omega$$

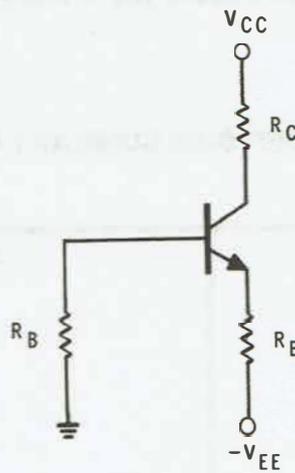
In practice, standard value resistors close to the calculated values would be chosen for the final design.

The following summary guide should assist you in analyzing or designing voltage-divider bias circuits.

VOLTAGE DIVIDER BIAS SUMMARY GUIDE

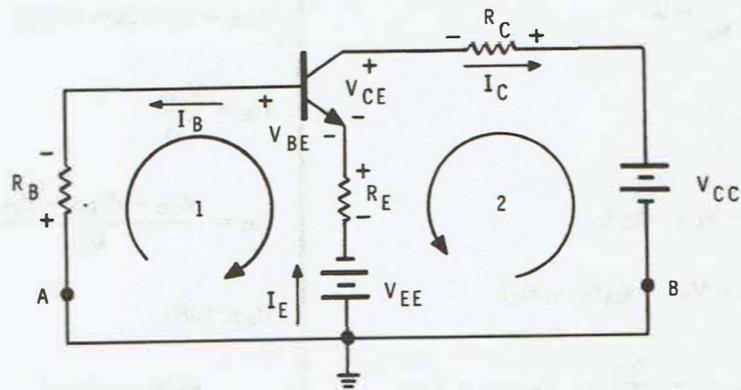
ANALYSIS	DESIGN
$V_B = \frac{V_{CC} R_2}{R_1 + R_2}$	
$V_E = V_B - V_{BE}$	$V_{EQ} = 20 \text{ to } 30\% \text{ of } V_{CC}$
$I_E = \frac{V_E}{R_E} \approx I_C$	$R_E = \frac{V_{EQ}}{I_{CQ}}$
$I_B = \frac{I_C}{\beta}$	$R_C = \frac{V_{CC} - (V_{EQ} + V_{CEQ})}{I_{CQ}}$
$V_C = V_{CC} - I_C R_C$	$R_2 \leq 10R_E$
$V_{CE} = V_{CC} - I_C(R_C + R_E)$	$R_1 = \frac{R_2(V_{CC} - V_{BQ})}{V_{BQ}}$
$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E}, V_{CE(out)} = V_{CC}$	

(A)



ORIGINAL CIRCUIT

(B)



REDRAWING THE CIRCUIT

Figure 2-28

- Emitter bias.
- A. Original circuit.
- B. Redrawing the circuit.

Emitter Bias

The circuit illustrated in Figure 2-28A provides a very stable operating point. Because this biasing scheme requires two power supplies, it is a popular choice in dual supply systems.

The analysis of the circuit proceeds in the usual manner. First, the circuit is redrawn as shown in Figure 2-28B. Next, the base loop equation is written, starting at point A and going clockwise around the loop.

Specifically:

$$I_B R_B + V_{BE} + I_E R_E - V_{EE} = 0 \quad (\text{loop-1})$$

Substituting the approximate relationship βI_B for I_E yields:

$$I_B R_B + \beta I_B R_E + V_{BE} - V_{EE} = 0$$

$$I_B (\beta R_E + R_B) = V_{EE} - V_{BE}$$

$$I_B = \frac{V_{EE} - V_{BE}}{\beta R_E + R_B} \quad (\text{Eq. 2-29})$$

Since $I_C = \beta I_B$ we have:

$$I_C = \beta I_B = \frac{\beta (V_{EE} - V_{BE})}{\beta R_E + R_B}$$

Dividing numerator and denominator by β yields:

$$I_C = \frac{V_{EE} - V_{BE}}{R_E + \frac{R_B}{\beta}} \approx I_E \quad (\text{Eq. 2-30})$$

As you will see when designing an emitter bias circuit, R_E is shown so that:

$$R_E \gg \frac{R_B}{\beta}$$

Assuming this is the case, Equation 2-30 is closely approximated by:

$$I_C \approx I_E = \frac{V_{EE} - V_{BE}}{R_E} \quad (\text{Eq. 2-31})$$

Equation 2-31 indicates that the value of the collector and emitter currents are essentially fixed by the values of V_{EE} and R_E . This is why the circuit is referred to as an emitter bias circuit.

To obtain an equation for the circuit's DC load line, the collector loop equation is written. Thus, by starting at point B and going around the loop in a counterclockwise direction, you obtain:

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E - V_{EE} = 0$$

Substituting I_C for I_E and solving for V_{CE} yields:

$$V_{CE} = (V_{CC} + V_{EE}) - I_C(R_C + R_E) \quad (\text{Eq. 2-32})$$

Using the intercept values to approximate $I_{C(\text{sat})}$ and $V_{CE(\text{cut})}$, you have:

$$I_{C(\text{sat})} = \frac{V_{CC} + V_{EE}}{R_C + R_E} \quad (\text{Eq. 2-33})$$

$$V_{CE(\text{cut})} = V_{CC} + V_{EE} \quad (\text{Eq. 2-34})$$

Finally, the various terminal-to-ground voltages are:

$$V_C = V_{CC} - I_C R_C$$

$$V_E = I_E R_E - V_{EE}$$

$$V_B = V_{BE} + V_E$$

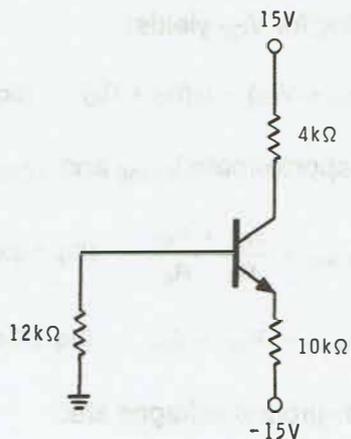
The following examples illustrate the analysis and design of emitter bias circuits.



Example 2-14
 Design an emitter bias circuit for a common-emitter amplifier. The load resistor is $R_L = 10\text{ k}\Omega$. The collector resistor is $R_C = 10\text{ k}\Omega$. The emitter resistor is $R_E = 1\text{ k}\Omega$. The supply voltages are $V_{CC} = 10\text{ V}$ and $V_{EE} = -10\text{ V}$. The transistor has a $\beta = 100$. Determine the values of R_1 and R_2 for a $V_{CE} = 5\text{ V}$ and $I_C = 1\text{ mA}$.

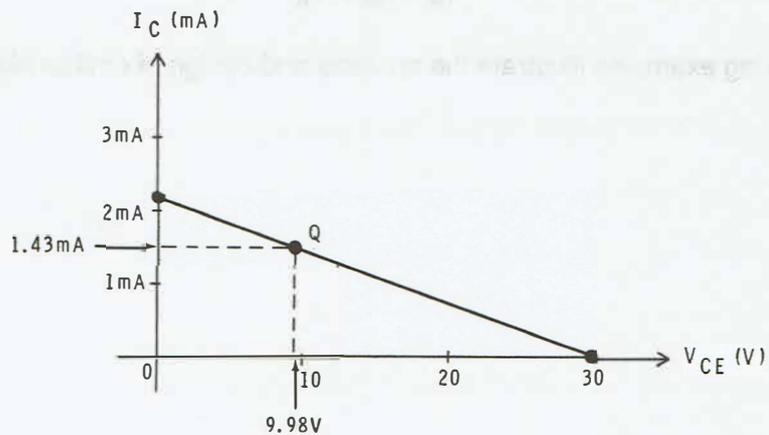
Solution: The load resistor R_L is connected in parallel with the collector resistor R_C . The equivalent collector resistor is $R_{C'} = R_C \parallel R_L = 5\text{ k}\Omega$. The emitter resistor R_E is connected in series with the emitter terminal. The base resistor network is connected to the base terminal. The base-emitter junction is forward-biased. The collector current I_C is approximately equal to the emitter current I_E . The collector-emitter voltage V_{CE} is the voltage across the collector resistor network and the emitter resistor. The base voltage V_B is the voltage across the base-emitter junction plus the voltage across the emitter resistor. The base current I_B is the current through the base resistor network. The collector current I_C is βI_B . The emitter current I_E is $(\beta + 1) I_B$. The collector current I_C is 1 mA . The emitter current I_E is 1.01 mA . The collector-emitter voltage V_{CE} is 5 V . The collector voltage V_C is $V_{CC} - I_C R_{C'} = 10\text{ V} - (1\text{ mA})(5\text{ k}\Omega) = 5\text{ V}$. The emitter voltage V_E is $I_E R_E - V_{EE} = (1.01\text{ mA})(1\text{ k}\Omega) - (-10\text{ V}) = 10.101\text{ V}$. The base voltage V_B is $V_{BE} + V_E = 0.7\text{ V} + 10.101\text{ V} = 10.801\text{ V}$. The base resistor network is connected to V_{CC} and V_{EE} . The base current I_B is $I_C / \beta = 1\text{ mA} / 100 = 10\text{ }\mu\text{A}$. The emitter current I_E is $(\beta + 1) I_B = 101 \times 10\text{ }\mu\text{A} = 1.01\text{ mA}$. The collector current I_C is $\beta I_B = 100 \times 10\text{ }\mu\text{A} = 1\text{ mA}$. The collector-emitter voltage V_{CE} is 5 V . The collector voltage V_C is 5 V . The emitter voltage V_E is 10.101 V . The base voltage V_B is 10.801 V . The base resistor network is connected to V_{CC} and V_{EE} . The base current I_B is $10\text{ }\mu\text{A}$. The emitter current I_E is 1.01 mA . The collector current I_C is 1 mA . The collector-emitter voltage V_{CE} is 5 V . The collector voltage V_C is 5 V . The emitter voltage V_E is 10.101 V . The base voltage V_B is 10.801 V .

(A)



CIRCUIT

(B)



DC LOAD LINE

Figure 2-29

Circuit and DC load line for Example 2-14.

- A. Circuit.
- B. DC load line.

Example 2-14

Sketch the DC load line and operating point for the circuit shown in Figure 2-29A. Also, estimate the emitter-to-ground voltage, V_E .

First, calculate the intercept values of the load line.

$$I_{C(\text{sat})} = \frac{V_{CC} + V_{EE}}{R_C + R_E} = \frac{15V + 15V}{4k\Omega + 10k\Omega} = 2.14\text{mA}$$

$$V_{CE(\text{cut})} = V_{CC} + V_{EE} = 15V + 15V = 30V$$

The approximate formula for I_C is quite accurate if $R_E \gg R_B/B$. Even though a value for B is not given in Figure 2-29A, you know that B rarely has a value less than 20. Consequently, you can feel confident in using the approximate formula for I_C since, in this case:

$$10k\Omega \gg \frac{12k\Omega}{20}$$

Thus:

$$I_C = \frac{V_{CC} - V_{BE}}{R_E} = \frac{15V - 0.7V}{10k\Omega} = 1.43\text{mA} \approx I_E$$

With $I_C = 1.43\text{mA}$ the collector to emitter voltage V_{CE} is:

$$V_{CE} = (V_{CC} + V_{EE}) - I_C(R_C + R_E)$$

$$V_{CE} = (15V + 15V) - 1.43\text{mA}(4k\Omega + 10k\Omega)$$

$$V_{CE} = 30V - 20.02V = 9.98V$$

The circuit's DC load line is illustrated in Figure 2-29B.

Finally, the emitter-to-ground voltage, V_E , is:

$$V_E = I_E R_E - V_{EE}$$

$$V_E = 1.43\text{mA}(10k\Omega) - 15V = -0.7V$$

Note that the emitter-to-ground voltage is negative. Typically, in an NPN emitter bias circuit, V_E has a magnitude slightly less than 1V and is negative.

Example 2-15

Design an emitter bias circuit to provide an I_{CQ} of 2mA and a V_{CEQ} of 10V. Assume supply voltages of $\pm 20V$ are available for the design.

Solving Equation 2-31 for R_E yields:

$$R_E = \frac{V_{EE} - V_{BE}}{I_C}$$

In this case, then:

$$R_E = \frac{20V - 0.7V}{2mA} = 9.65k\Omega$$

To ensure an operating point that is B independent, R_B is chosen so that:

$$R_E \gg \frac{R_B}{\beta}$$

This condition is satisfied if the value selected for R_B is on the same order of magnitude as the value of R_E . Many circuit designers simply select a value of R_B equal to the value calculated for R_E . Thus:

$$R_B = R_E = 9.65\text{k}\Omega$$

Solving Equation 2-32 for R_C yields the following useful formulas:

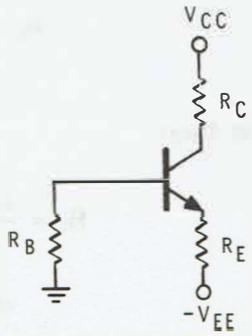
$$R_C = \frac{(V_{CC} + V_{EE}) - [V_{CEQ} + I_{CQ}R_E]}{I_{CQ}}$$

In this case, then:

$$\begin{aligned} R_C &= \frac{(20\text{V} + 20\text{V}) - [10\text{V} + 2\text{mA}(9.65\text{k}\Omega)]}{2\text{mA}} \\ &= \frac{40\text{V} - 29.3\text{V}}{2\text{mA}} = 5.35\text{k}\Omega \end{aligned}$$

The following summary guide for the emitter bias circuit provides the formulas necessary for analysis and design.

EMITTER BIAS SUMMARY GUIDE

ANALYSIS	DESIGN
$I_C = \frac{V_{EE} - V_{BE}}{R_E} \approx I_E \quad (R_E \gg \frac{R_B}{\beta})$	
$I_B = \frac{I_C}{\beta}$	$R_E = \frac{V_{EE} - V_{BE}}{I_{CQ}}$
$V_C = V_{CC} - I_C R_C$	$R_B \approx R_E$
$V_E = I_E R_E - V_{EE}$	$R_C = \frac{(V_{CC} + V_{EE}) - (V_{CEQ} + I_{CQ} R_E)}{I_{CQ}}$
$V_B = V_{BE} + V_E$	
$V_{CE} = (V_{CC} + V_{EE}) - I_C (R_C + R_E)$	
$I_{C(sat)} = \frac{V_{CC} + V_{EE}}{R_C + R_E}, \quad V_{CE(out)} = V_{CC} + V_{EE}$	

PNP Biasing Schemes

The current directions and voltage polarities in PNP circuits are just the opposite of those in NPN circuits. For this reason, PNP circuits are said to be **complements** of NPN circuits, and vice versa.

This concept is illustrated in Figure 2-30. Here, note that the only difference between the two circuits is the fact that the current directions, and voltage polarities are reversed. On most schematics, the PNP circuit in Figure 2-30B would **not** be drawn the way it is in Figure 2-30B. Before illustrating how the circuit would be drawn, let's first consider the concept of a reference, or ground point.

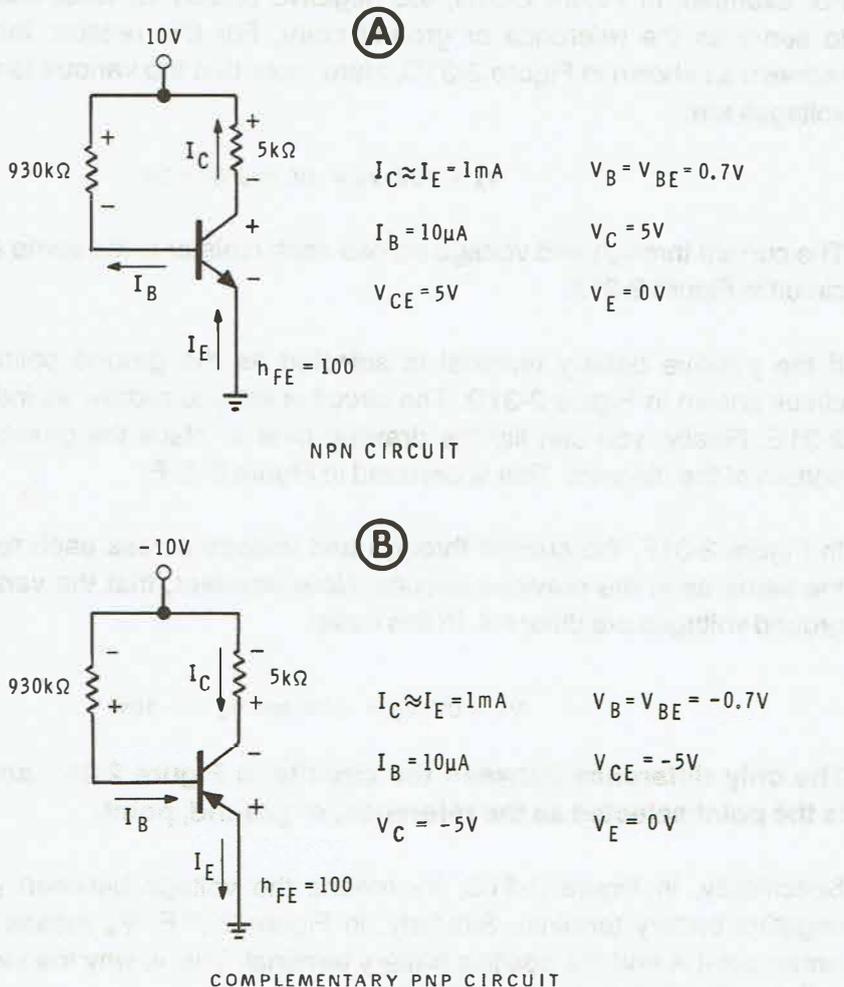


Figure 2-30

The complementary nature of NPN and PNP circuits.

- A. NPN circuit.
- B. Complementary PNP circuit.

The Ground Point

In Figure 2-31A, the current flowing in the circuit is 1mA. Consequently, the voltage across the 6k Ω resistor, V_{AB} , is 6V and the voltage across the 4k Ω resistor, V_{BC} , is 4V.

In a given circuit, voltages can be measured between any two points. Usually, however, one point is selected as a reference point. This reference point is referred to as the common, or ground, point. On a schematic diagram, a voltage is "called out" by indicating what the voltage is between the point of interest and the ground point.

For example, in Figure 2-31B, the negative battery terminal has been selected to serve as the reference or ground point. For this reason, the circuit can be redrawn as shown in Figure 2-31C. Here, note that the various terminal-to-ground voltages are:

$$V_A = 10V, V_B = 4V, \text{ and } V_C = 0V$$

The current through and voltage across each resistor is the same as in the original circuit in Figure 2-31A.

If the positive battery terminal is selected as the ground point, you have the circuit shown in Figure 2-31D. The circuit is easy to redraw as indicated in Figure 2-31E. Finally, you can flip the drawing over to place the ground symbol at the bottom of the diagram. This is depicted in Figure 2-31F.

In Figure 2-31F, the current through and voltage across each resistor is exactly the same as in the previous circuits. Note however, that the various terminal-to-ground voltages are different. In this case:

$$V_A = 0V, V_B = -6V, \text{ and } V_C = -10V$$

The only difference between the circuits in Figure 2-31C and Figure 2-31F is the point selected as the reference, or ground, point.

Specifically, in Figure 2-31C, V_A means the voltage between point A and the negative battery terminal. Similarly, in Figure 2-31F, V_A means the voltage between point A and the positive battery terminal. This is why the terminal to ground voltages are different in the two Figures.

It is important to realize that Figure 2-31C and Figure 2-31F each represent **the same** physical circuit. Only the ground point and the manner in which each circuit is drawn is different.

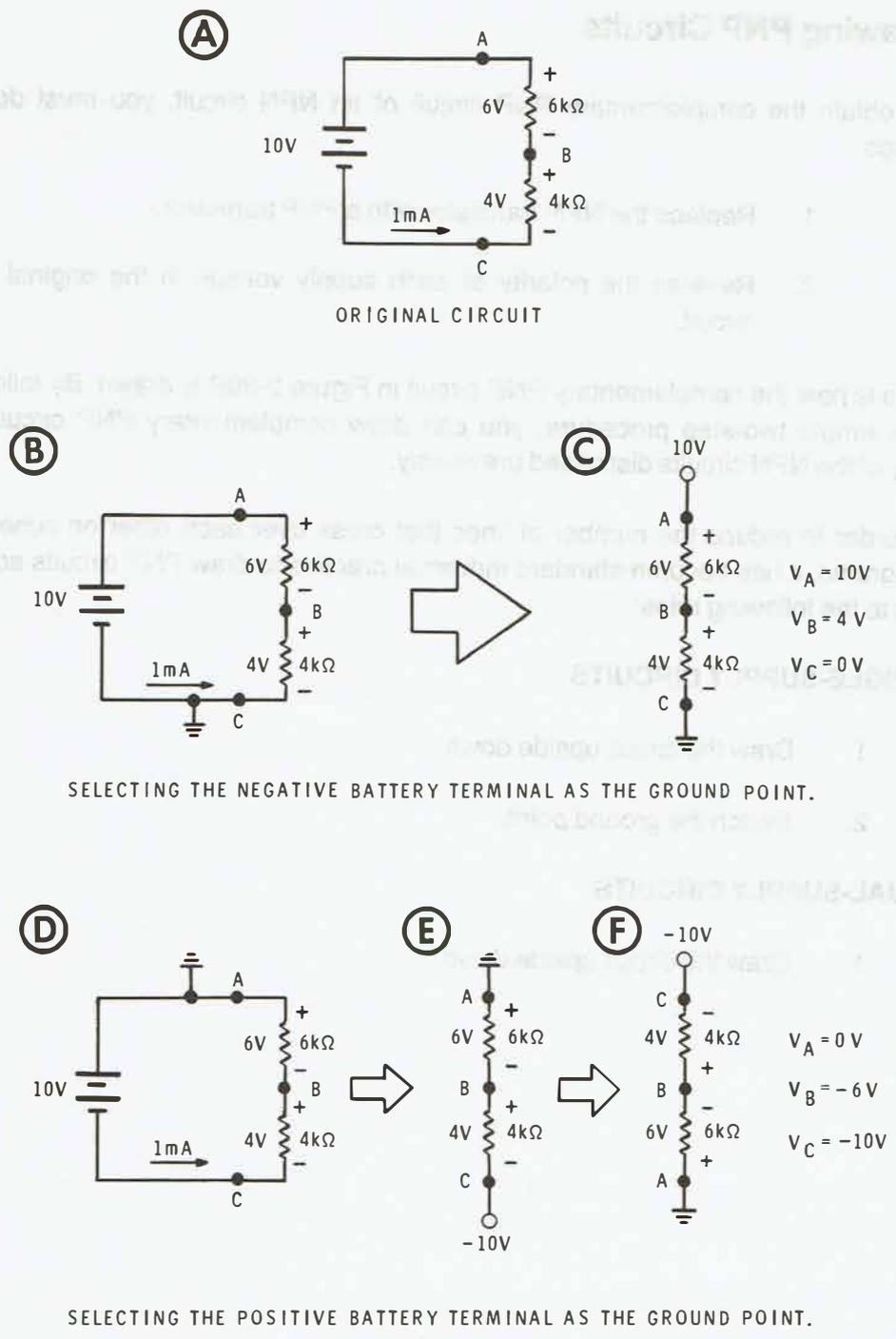


Figure 2-31

The concept of a ground or reference point. Note that terminal-to-ground voltages depend upon which point is selected as the ground, or reference, point. Also note that the terminal-to-terminal voltages are not effected by the choice of the ground point.

- A. Original circuit.
- B, C. Selecting the negative battery terminal as the ground point.
- D, E, F. Selecting the positive battery terminal as the ground point.

Drawing PNP Circuits

To obtain the complementary PNP circuit of an NPN circuit, you must do two things:

1. Replace the NPN transistor with a PNP transistor.
2. Reverse the polarity of each supply voltage in the original NPN circuit.

This is how the complementary PNP circuit in Figure 2-30B is drawn. By following this simple two-step procedure, you can draw complementary PNP circuits for any of the NPN circuits discussed previously.

In order to reduce the number of lines that cross over each other on schematic diagrams, it has become standard industrial practice to draw PNP circuits according to the following rules:

SINGLE-SUPPLY CIRCUITS

1. Draw the circuit upside down.
2. Switch the ground point.

DUAL-SUPPLY CIRCUITS

1. Draw the circuit upside down.

As an example, consider the PNP circuit in Figure 2-32A. If you draw the circuit upside down, you obtain the circuit shown in Figure 2-32B. Similarly, by switching the ground point, you obtain the circuit shown in Figure 2-32C. This is the way the circuit is drawn on most schematic diagrams.

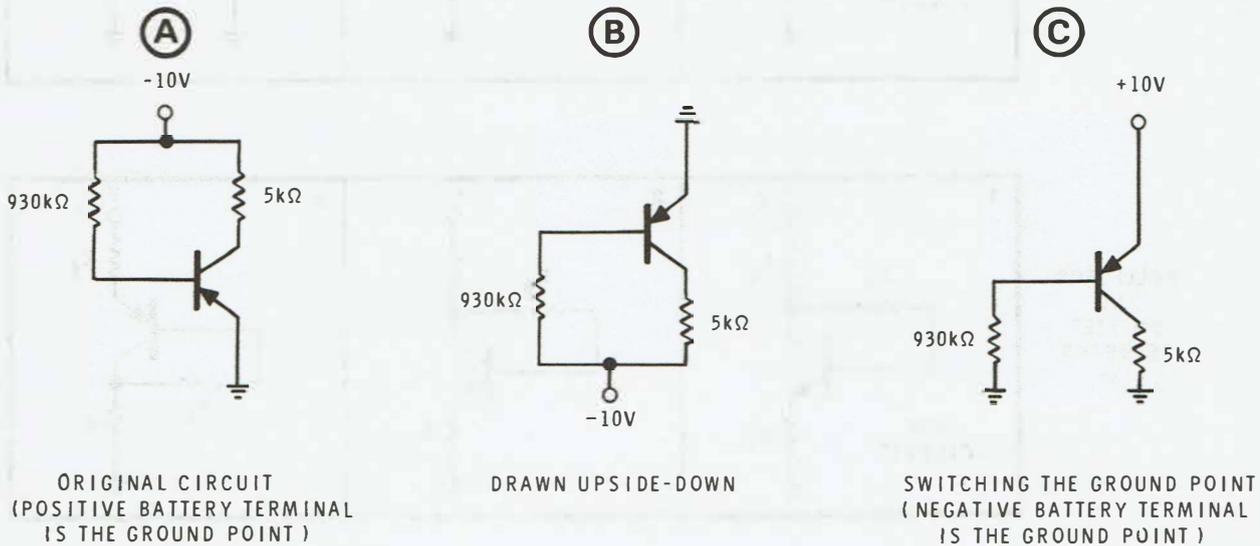


Figure 2-32

Drawing PNP circuits.

The circuit in A would normally appear on a schematic diagram as shown in C. See text for details.

- A. Original circuit. (Positive battery terminal is the ground point).
- B. Drawn upside-down.
- C. Switching the ground point. (Negative battery terminal is the ground point.)

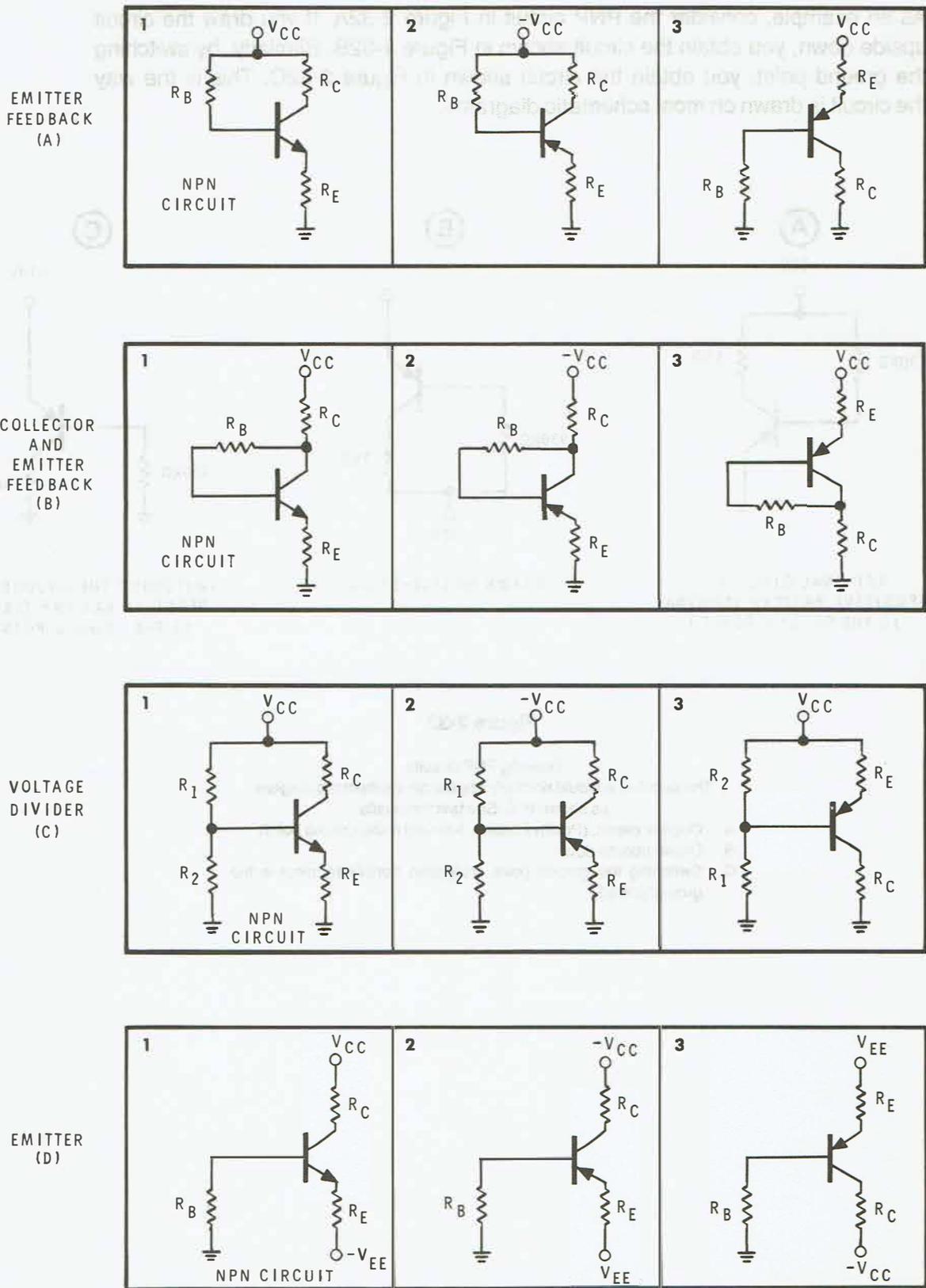


Figure 2-33

NPN and complementary PNP circuits for typical biasing schemes.
 Box 3 shows how the PNP circuit appears on most schematic diagrams.

- A. Emitter Feedback.
- B. Collector and Emitter Feedback.
- C. Voltage Divider.
- D. Emitter.

Figure 2-33 illustrates how additional PNP circuits usually appear on schematic diagrams. Note that for each biasing scheme:

1. Box 1 illustrates an NPN circuit.
2. Box 2 illustrates the complementary circuits.
3. Box 3 illustrates how the complementary PNP circuit would be drawn on most schematic diagrams.

In Figure 2-33, the circuits in boxes 2 and 3 represent the same physical circuit. Consequently, the transistor currents (I_B , I_C , and I_E) and terminal-to-terminal voltages (V_{BE} , V_{CE} , and V_{CB}) are identical.

In the single-supply circuits, the ground point in box 2 (positive battery terminal) is different from the ground point in box 3 (negative battery terminal). For this reason, the terminal-to-ground voltages (V_B , V_E , and V_C) of the single-supply circuits in box 2 are **not** the same as the terminal-to-ground voltages in box 3.

Analyzing and Designing Circuits

In Figure 2-33, the only difference between the NPN circuits in box 1 and the complementary PNP circuits in box 2 is the fact that the current directions and voltage polarities are reversed.

For this reason, by working with **magnitudes**, you can also use the NPN analysis and design equations given previously to analyze or design the PNP circuits in box 2 of Figure 2-33.

Similarly, the NPN equations for the transistor currents (I_B , I_C , and I_E) and terminal-to-terminal voltage (V_{BE} , V_{CE} , and V_{CB}) are also valid for the PNP circuits in box 3. Naturally, the NPN equations for terminal-to-ground voltages (V_B , V_C , and V_E) do **not** apply to the single-supply circuits in box 3.

In any event, the following procedure will be used for the design and analysis of PNP circuits:

DESIGN

1. Calculate the required component values via the NPN design formulas on the appropriate biasing summary guide.
2. Sketch the circuit as shown in the appropriate box 3 in Figure 2-33.

ANALYSIS

1. Use the appropriate NPN analysis formula to calculate values for I_C and V_{CE} .
2. Once you know the value of I_C , you should be able to deduce values for the terminal-to-ground voltages by simply looking at the PNP circuit.

The following examples illustrate the design and analysis of several PNP circuits.

Example 2-16

Design an emitter feedback circuit using a PNP transistor whose $h_{FE} = 100$. The desired Q point is $I_{CQ} = 1\text{mA}$ and $V_{CEQ} = -6\text{V}$. Assume the available DC supply voltage is 12V .

Referring to the emitter feedback NPN biasing summary guide:

$$V_{EQ} = 0.2 V_{CC} = 0.2(12\text{V}) = 2.4\text{V}$$

$$R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{2.4\text{V}}{1\text{mA}} = 2.4\text{k}\Omega$$

$$R_C = \frac{V_{CC} - (V_{EQ} + V_{CEQ})}{I_{CQ}} = \frac{12\text{V} - (2.4\text{V} + 6\text{V})}{1\text{mA}} = 3.6\text{k}\Omega$$

Since $I_{CQ} = 1\text{mA}$ and $h_{FE} = 100$, $I_{BQ} = 1\text{mA}/100$ or $10\mu\text{A}$. Thus:

$$R_B = \frac{V_{CC} - (V_{BE} + V_{EQ})}{I_{BQ}} = \frac{12\text{V} - (0.7\text{V} + 2.4\text{V})}{10\mu\text{A}} = 890\text{k}\Omega$$



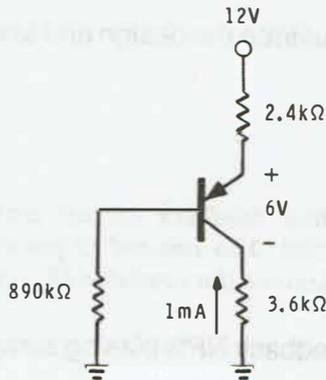


Figure 2-34

Circuit for Example 2-16.

Figure 2-34 illustrates the circuit.

Example 2-17

Work out values for V_C , V_E , and V_B for the circuit in Figure 2-34.

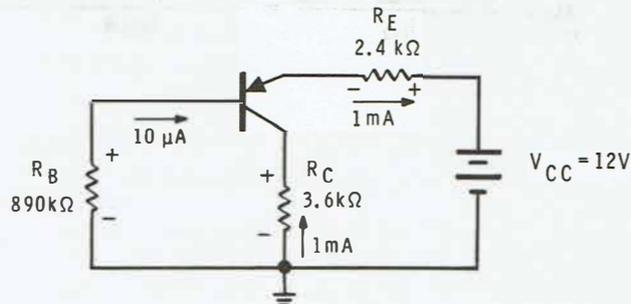


Figure 2-35

Redrawing the circuit in Figure 2-34.

If it is not obvious to you how to calculate a particular voltage, redraw the circuit as shown in Figure 2-35. By inserting known values, you can calculate the terminal-to-ground voltages by writing appropriate loop equations. Therefore:

$$V_C = I_C R_C = 1\text{mA}(3.6\text{k}\Omega) = 3.6\text{V}$$

$$V_E = -I_E R_E + V_{CC} = -1\text{mA}(2.4\text{k}\Omega) + 12\text{V} = 9.6\text{V}$$

Note that $V_{CC} = V_C - V_E = -6\text{V}$, which is what the circuit was designed for in Example 2-16.

Finally:

$$V_B = I_B R_B = 10\mu\text{A}(890\text{k}\Omega) = 8.9\text{V}$$

Self-Test Review

Refer to Figure 2-36 for questions 21 through 23.

21. Calculated values for the resistors are:

$$R_E = \text{_____k}\Omega, R_C = \text{_____k}\Omega, R_2 = \text{_____k}\Omega, \text{ and } R_1 = \text{_____k}\Omega.$$

22. The terminal-to-ground voltages are:

$$V_B = \text{_____V}, V_C = \text{_____V}, \text{ and } V_E = \text{_____V}.$$

23. The transistor is dissipating approximately _____mW.

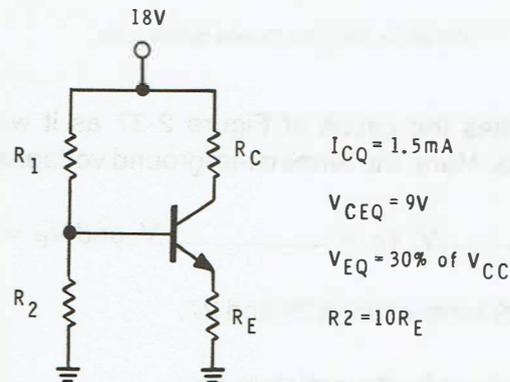


Figure 2-36

Circuit for Self-Test Review questions 21-23.

Figure 2-37 illustrates the complementary PNP circuit for the circuit designed in question 21. Here, the terminal to ground voltages are:

24. $V_B = \text{_____V}$, $V_C = \text{_____V}$, and $V_E = \text{_____V}$.

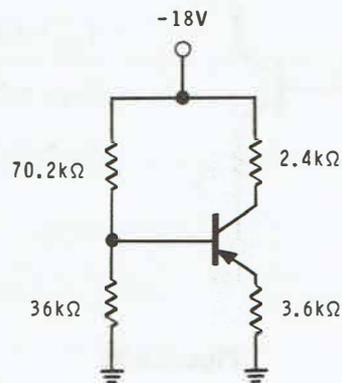


Figure 2-37

Circuit for Self-Test Review questions 24.

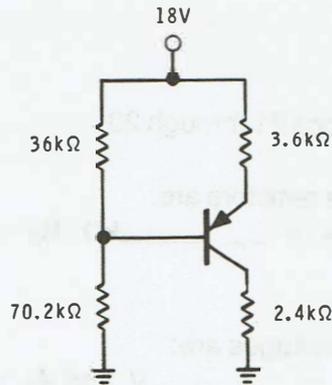


Figure 2-38

Circuit for Self-Test Review question 25.

Figure 2-38 illustrates the circuit of Figure 2-37 as it would be drawn on most schematic diagrams. Here, the terminal-to-ground voltages are:

25. $V_B = \text{_____} \text{V}$, $V_C = \text{_____} \text{V}$, and $V_E = \text{_____} \text{V}$.

Refer to Figure 2-39 for questions 26 and 27.

26. Calculated values for the resistors are:
 $R_E = R_B = \text{_____} \text{k}\Omega$ and $R_C = \text{_____} \text{k}\Omega$.

27. The collector-to-ground voltage is $\text{_____} \text{V}$.

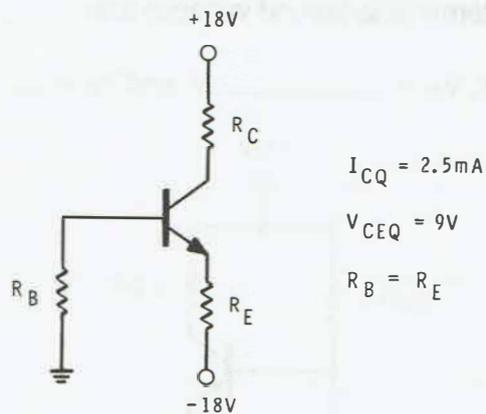


Figure 2-39

Circuit for Self-Test Review questions 26 and 27.

Answers

21. $R_E = 3.6\text{k}\Omega$, $R_C = 2.4\text{k}\Omega$, $R_2 = 36\text{k}\Omega$, and $R_1 = 70.2\text{k}\Omega$
22. $V_B = 6.1\text{V}$, $V_C = 14.4\text{V}$, and $V_E = 5.4\text{V}$
23. 13.5mW
24. $V_B = -6.1\text{V}$, $V_C = -14.4\text{V}$ and $V_E = -5.4\text{V}$
25. $V_B = 11.9\text{V}$, $V_C = 3.6\text{V}$, and $V_E = 12.6\text{V}$
26. $R_E = R_B = 6.92\text{k}\Omega$, $R_C = 3.88\text{k}\Omega$
27. $V_C = 8.3\text{V}$

The solution to questions 21-27 follows:

21. Referring to the voltage-divider biasing summary guide:

$$V_{EQ} = 0.3V_{CC} = 0.3(18\text{V}) = 5.4\text{V}$$

$$R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{5.4\text{V}}{1.5\text{mA}} = 3.6\text{k}\Omega$$

$$R_C = \frac{V_{CC} - (V_{EQ} + V_{CEQ})}{I_{CQ}} = \frac{18\text{V} - (5.4\text{V} + 9\text{V})}{1.5\text{mA}} = 2.4\text{k}\Omega$$

$$R_2 = 10R_E = 10(3.6\text{k}\Omega) = 36\text{k}\Omega$$

Since: $V_{EQ} = 5.4\text{V}$, $V_{BQ} = 0.7\text{V} + 5.4\text{V} = 6.1\text{V}$ Thus:

$$R_1 = \frac{R_2(V_{CC} - V_{BQ})}{V_{BQ}} = \frac{36\text{k}\Omega(18\text{V} - 6.1\text{V})}{6.1\text{V}} = 70.2\text{k}\Omega$$

22. The value of $V_B = V_{BQ}$ or 6.1V . Similarly, $V_E = V_{EQ}$ or 5.4V . The collector-to-ground voltage, V_C , is:

$$V_C = V_{CC} - I_C R_C = 18\text{V} - 1.5\text{mA}(2.4\text{k}\Omega) = 14.4\text{V}$$

23. The power dissipated by the transistor is:

$$P_{DQ} = V_{CEQ} I_{CQ}$$

$$P_{DQ} = 9\text{V}(1.5\text{mA}) = 13.5\text{mW}$$

24. The only differences between the NPN circuit in Figure 2-36 and the complementary PNP circuit in Figure 2-37 are the current directions, and voltage polarities.

Thus:

$$V_B = -6.1V, V_E = -5.4V, \text{ and } V_C = -14.4V$$

25. The circuit in Figure 2-38 is identical to the circuit in Figure 2-37. However, it is drawn differently. In this case the circuit is drawn upside down, with the reference (ground) terminal switched. Here, note that:

$$V_B = V_{70.2k\Omega} = \frac{18V(70.2k\Omega)}{70.2k\Omega + 36k\Omega} = 11.9V$$

$$V_C = I_C R_C = 1.5mA(2.4k\Omega) = 3.6V$$

$$V_E = V_{CC} - I_E R_E = 18V - 1.5mA(3.6k\Omega) = 12.6V$$

26. Referring to the emitter bias summary guide:

$$R_E = \frac{V_{EE} - V_{BE}}{I_{CQ}} = \frac{18V - 0.7V}{2.5mA} = 6.92k\Omega = R_B$$

$$R_C = \frac{(V_{CC} + V_{EE}) - (V_{CEQ} + I_{CQ}R_E)}{I_{CQ}} = \frac{36V - [9V + 2.5mA(6.92k\Omega)]}{2.5mA}$$

$$R_C = 3.88k\Omega$$

27. $V_C = V_{CC} - I_C R_C = 18V - 2.5mA(3.88k\Omega) = 8.3V$

SUMMARY

The purpose of a biasing circuit is to establish an appropriate operating point for a transistor. This simply means obtaining the desired values of I_{CQ} and V_{CEQ} .

BJT's can be biased to operate in the cutoff, saturation, or active regions. In the cutoff and saturation regions, the transistor approximates an open and closed switch respectively. For this reason, the transistors in digital circuits are biased to operate in either the cutoff or saturation modes. Several examples illustrating the design of simple switching circuits are provided in the unit.

In linear transistor circuits, the transistors should be biased to operate in the active region. Here, the emitter and collector currents are directly proportional to the base current since, in this region, $I_E \approx I_C = \beta I_B$.

Table 2-3 summarizes the characteristics of the six biasing schemes discussed in this unit.

Biasing Scheme	Advantages	Disadvantages	
Base	Few components required.	B dependent Q point.	
Emitter Feedback Collector Feedback Collector and Emitter Feedback	} Quasi-stable Q point.		
Voltage Divider		B independent Q point.	Requires four resistors.
Emitter		B independent Q point.	Requires dual supply voltages.

TABLE 2-3

Characteristics Of Typical Biasing Schemes.

Since base bias has an inherently unstable Q point, it is, generally speaking, not suitable for linear transistor circuits. Consequently, base bias circuits are primarily limited to digital and switching circuit applications.

Emitter feedback, collector feedback, and collector and emitter feedback circuits provide a quasi-stable Q point. This means that, in a given circuit, the actual Q point is partially dependent on the transistor's B value. Since this represents an improvement over base bias, it can be considered an advantage. However, the Q points in these circuits are not nearly as stable as those in voltage divider and emitter bias circuits. In this sense, a quasi-stable Q point represents a disadvantage. Consequently, these circuits are not the preferred biasing schemes for linear operation.

Voltage divider and emitter bias circuits provide very stable Q points. For this reason, they are the preferred biasing schemes for linear transistor circuits.

The analysis and design of the various biasing schemes is simplified by the biasing summary guides provided in the unit. By referring to the appropriate summary guide, you should be able to analyze and design all of the biasing schemes discussed in this unit. Also, by referring to Figure 2-33 and the examples in the text, you should be able to analyze and design complementary PNP biasing circuits.

UNIT EXAMINATION

The following multiple choice examination is designed to test your understanding of the material presented in this unit. Place a check beside the multiple choice answer (A, B, C or D) that you feel is most correct. When you have completed the examination, compare your answers with the correct ones that appear after the exam.

1. In Figure 2-40, R_S should equal:

- A. 80Ω .
- B. $0.5k\Omega$.
- C. $Zero\Omega$.
- D. $2.67k\Omega$.

2. In Figure 2-40, R_B should equal:

- A. $10.75k\Omega$.
- B. 80Ω .
- C. $16M\Omega$.
- D. $334k\Omega$.

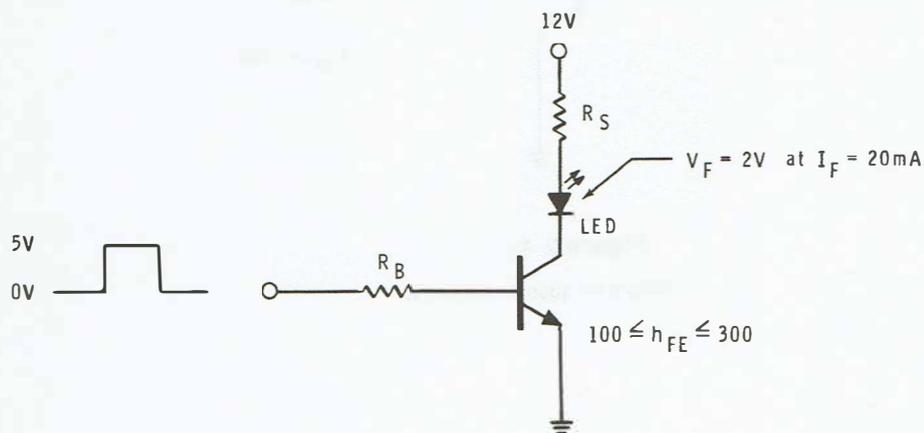


Figure 2-40

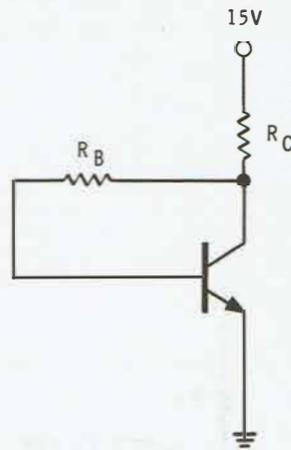
Circuit for questions 1 and 2.

3. In Figure 2-41, R_C should equal:

- A. $15k\Omega$.
- B. $10k\Omega$.
- C. $8k\Omega$.
- D. $7k\Omega$.

4. In Figure 2-41, R_B should equal:

- A. $7k\Omega$.
- B. $730k\Omega$.
- C. $2M\Omega$.
- D. $1.63M\Omega$.



$$I_{CQ} = 1\text{mA}$$

$$V_{CEQ} = 8\text{V}$$

$$h_{FE} = 100$$

Figure 2-41

Circuit for questions 3 and 4.

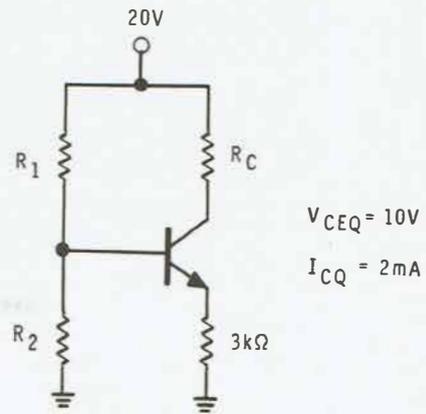


Figure 2-42

Circuit for questions 5-8.

Refer to Figure 2-42 for questions 5 through 8.

5. R_C should equal:
 - A. $1k\Omega$.
 - B. $2k\Omega$.
 - C. $3k\Omega$.
 - D. $4k\Omega$.

6. The maximum value recommended for R_2 is:
 - A. $2k\Omega$.
 - B. $3k\Omega$.
 - C. $20k\Omega$.
 - D. $30k\Omega$.

7. Assuming R_2 equals the value in question 6, R_1 should equal:
 - A. $39.7k\Omega$.
 - B. $59.5k\Omega$.
 - C. $100k\Omega$.
 - D. $220k\Omega$.

8. The collector-to-ground voltage is:
 - A. $16V$.
 - B. $10V$.
 - C. $6.7V$.
 - D. $5.3V$.

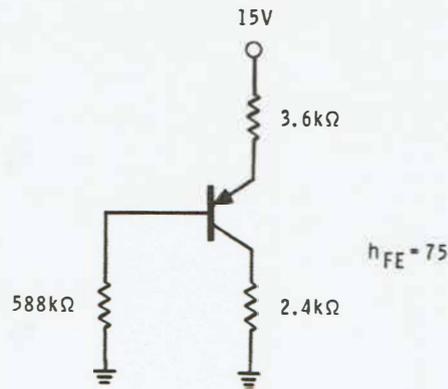
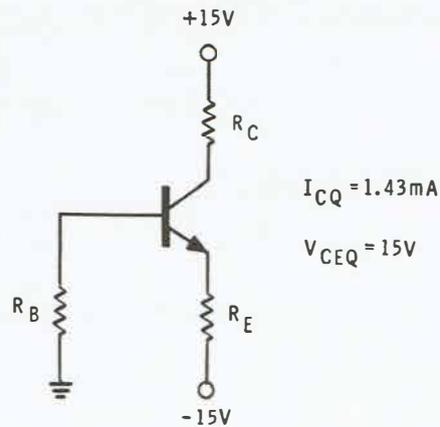


Figure 2-43

Circuit for questions 9-12.

Refer to Figure 2-43 for questions 9 through 12.

9. The emitter current is approximately:
- 4.17mA.
 - 6.25mA.
 - 1.25mA.
 - 2.5mA.
10. The emitter-to-ground voltage is:
- 10.5V.
 - 15V.
 - 3V.
 - 3V.
11. The collector-to-ground voltage is:
- 10.5V.
 - 15V.
 - 3V.
 - 3V.
12. The collector-to-emitter voltage, V_{CE} , is:
- 7.5V.
 - 7.5V.
 - 3V.
 - 3V.

**Figure 2-44**

Circuit for questions 13-15.

Refer to Figure 2-44 for questions 13 through 15.

13. A reasonable value for R_B is:

- A. $10\text{M}\Omega$.
- B. $1\text{M}\Omega$.
- C. $106.03\text{M}\Omega$.
- D. $10\text{k}\Omega$.

14. R_C should equal:

- A. $10\text{k}\Omega$.
- B. $5.7\text{k}\Omega$.
- C. $14.7\text{k}\Omega$.
- D. $22\text{k}\Omega$.

15. $I_{C(\text{sat})}$ is approximately:

- A. 2.7mA .
- B. 1.21mA .
- C. 1.5mA .
- D. 1.91mA .



AP Sample

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Refer to Figure 2-44 for questions 13 through 15.

13. A resistor is labeled with the following color bands:

- A. 100Ω
- B. 10Ω
- C. 1000Ω
- D. 10kΩ

14. A resistor is labeled with the following color bands:

- A. 100Ω
- B. 10kΩ
- C. 10kΩ
- D. 100Ω

15. A resistor is labeled with the following color bands:

- A. 2.2kΩ
- B. 22kΩ
- C. 2.2Ω
- D. 22Ω

EXAMINATION ANSWERS

1. B — Since $I_{C(\text{sat})} = I_F$ or 20mA, and $V_{\text{LED}} = 2\text{V}$, the required value of R_S is:

$$R_S = \frac{V_{CC} - V_{\text{LED}}}{I_{C(\text{sat})}} = \frac{12\text{V} - 2\text{V}}{20\text{mA}} = 0.5\text{k}\Omega$$

2. A — First, calculate the required base current:

$$I_B = 2I_{B(\text{sat})} = \frac{2I_{C(\text{sat})}}{h_{FE(\text{MIN})}} = \frac{2(20\text{mA})}{100} = 0.4\text{mA}$$

Next, calculate the required value of R_B :

$$R_B = \frac{V_1 - V_{BE}}{I_B} = \frac{5\text{V} - 0.7\text{V}}{0.4\text{mA}} = 10.75\text{k}\Omega$$

3. D — Referring to the collector feedback summary guide:

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{15\text{V} - 8\text{V}}{1\text{mA}} = 7\text{k}\Omega$$

4. B — Since $I_{CQ} = 1\text{mA}$ and $h_{FE} = 100$, $I_{BQ} = 1\text{mA}/100$ or $10\mu\text{A}$. Thus:

$$R_B = \frac{V_{CEQ} - V_{BE}}{I_{BQ}} = \frac{8\text{V} - 0.7\text{V}}{10\mu\text{A}} = 730\text{k}\Omega$$

5. B — Referring to the voltage divider summary guide:

$$R_C = \frac{V_{CC} - (V_{EQ} + V_{CEQ})}{I_{CQ}}$$

Since $R_F = 3\text{k}\Omega$ and $I_{CQ} = 2\text{mA}$, V_{EQ} is $2\text{mA}(3\text{k}\Omega)$ or 6V . Thus:

$$R_C = \frac{20\text{V} - (6\text{V} + 10\text{V})}{2\text{mA}} = 2\text{k}\Omega$$

6. D — R_2 is selected so that $R_2 = 10R_E$. Therefore, the maximum value for R_2 is $10R_E$ or $30\text{k}\Omega$.

$$7. \quad B \text{ — } R_1 = \frac{R_2(V_{CC} - V_{BQ})}{V_{BQ}}$$

Since $V_{EQ} = 6V$, $V_{BQ} = (0.7 + 6)V$ or $6.7V$. Thus:

$$R_1 = \frac{30k\Omega(20V - 6.7V)}{6.7V} = 59.5k\Omega$$

$$8. \quad A \text{ — } V_C = V_{CC} - I_C R_C$$

$$V_C = 20V - 2mA(2k\Omega) = 16V$$

9. C — Referring to the emitter feedback summary guide and working with magnitude, since we are analyzing a PNP circuit:

$$I_C = \frac{V_{CC} - V_{BE}}{R_E + \frac{R_B}{B}} = \frac{15V - 0.7V}{3.6k\Omega + \frac{588k\Omega}{75}} = 1.25mA \approx I_E$$

10. A — In Figure 2-43, $V_E = V_{CC} - I_E R_E$. Thus:

$$V_E = 15V - 1.25mA(3.6k\Omega) = 10.5V$$

11. C — In Figure 2-43, $V_C = I_C R_C$. Thus:

$$V_C = 1.25mA(2.4k\Omega) = 3V$$

12. B — The **magnitude** of V_{CE} via the NPN emitter feedback summary guide is $V_{CC} - I_C(R_C + R_E)$. Thus:

$$V_{CE} = 15V - 1.25mA(2.4k\Omega + 3.6k\Omega) = 7.5V$$

However, since the terminal-to-terminal voltages in a PNP transistor are just the opposite polarity of those in a NPN transistor, $V_{CE} = -7.5V$.

Note that this agrees with our previous calculations since:

$$V_{CE} = V_C - V_E$$

$$V_{CE} = 3V - 10.5V = -7.5V$$

13. D — Referring to the emitter bias summary guide, you can see that $R_B \approx R_E$. Thus:

$$R_E = \frac{V_{EE} - V_{BE}}{I_{CQ}} = \frac{15V - 0.7V}{1.43mA} = 10k\Omega \approx R_B$$

14. B — $R_C = \frac{(V_{CC} + V_{EE}) - (V_{CEQ} + I_{CQ}R_E)}{I_{CQ}}$
- $$= \frac{(15V + 15V) - [7.5V + 1.43mA(10k\Omega)]}{1.43mA} = 5.7k\Omega$$

15. D — $I_{C(sat)} = \frac{V_{CC} + V_{EE}}{R_C + R_E} = \frac{15V + 15V}{5.7k\Omega + 10k\Omega} = 1.91mA$

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UNIT 3

**COMMON-EMITTER
VOLTAGE AMPLIFIERS**

CONTENTS

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INTRODUCTION

Unit 2 discussed the analysis and design of typical common-emitter biasing circuits. By adding coupling and bypass capacitors to these circuits, you can construct practical voltage amplifiers. Therefore, in this unit, you will learn how to analyze and design a number of common-emitter voltage amplifiers.

The amplifiers discussed in this unit are referred to as small-signal amplifiers. In a small signal amplifier, the AC input voltage normally produces collector current variations that are small compared to the quiescent collector current. Amplifiers specifically designed for large signal operation will be discussed in a later unit.

UNIT OBJECTIVES

When you have completed this unit, you should be able to:

1. Calculate voltage, current, power gain, input resistance, and output resistance for common-emitter voltage amplifiers.
2. Sketch the AC load line for common-emitter voltage amplifiers.
3. Predict clipping levels for low gain, common-emitter voltage amplifiers.
4. Design both low gain, and large gain, common-emitter voltage amplifiers.

UNIT ACTIVITY GUIDE

- Read section on “Fundamental Concepts.”
- Answer Self-Test Review Questions 1-10.
- Read section on “Analysis of Common-Emitter Amplifiers.”
- Answer Self-Test Review Questions 11-20.
- Read section on “AC Load Lines and the Design of Common-Emitter Voltage Amplifiers.”
- Answer Self-Test Review Questions 21-30.
- Perform Experiment 4 in Unit 9.
- Perform Experiment 5 in Unit 9.
- Study Summary.
- Complete Unit Examination.
- Check Examination Answers.

FUNDAMENTAL CONCEPTS

Generally speaking, the analysis and design of amplifier circuits consist of three stages. For example, when you analyze an amplifier, you must first determine the appropriate values of DC currents and voltage. You can do this by using the methods introduced in Unit 2. Once you know the DC responses, you must calculate the AC responses. The methods available for doing this will be discussed in this unit. Finally, you can obtain the actual responses by determining the algebraic sums of the DC and AC responses. Once you have mastered each stage in the process just described, you will be able to analyze and design a number of useful amplifier circuits.

Amplification

A small AC voltage applied between the base of a properly biased BJT and ground, produces a small change in the base current, I_B . Since $I_C = \beta I_B$, the corresponding change in the collector current, I_C , is much larger. For this reason, BJTs are inherently current amplifying devices.

BJTs can also be used to provide voltage amplification. For example, if the collector current, which is an amplified version of the base current, flows through a relatively large collector resistor, R_C , the voltage developed across the resistor will be an amplified version of the original small AC input voltage.

Gain

In a discussion of amplifiers, you will frequently encounter the terms current gain, voltage gain, and power gain. From your knowledge of basic electronics, recall that the gain of a circuit is simply a ratio of the output signal to the input signal. Consequently, gain indicates the amount of signal amplification.

To avoid confusing one type of gain with another, we will adopt the following notation:

$$\text{Current Gain} \quad A_i = \frac{i_o}{i_{IN}} \quad (\text{Eq. 3-1})$$

$$\text{Voltage Gain} \quad A_v = \frac{v_o}{v_{IN}} \quad (\text{Eq. 3-2})$$

$$\text{Power Gain} \quad A_p = \frac{P_o}{P_{IN}} = A_i A_v \quad (\text{Eq. 3-3})$$

Note that the power gain equals the product of the current and voltage gains.

The following formulas are used to convert current, voltage, and power gains to their decibel, dB, equivalents.

For a current or voltage gain, the equivalent dB gain is:

$$A_{dB} = 20 \log A \quad (\text{Eq. 3-4})$$

Similarly, for a power gain, the equivalent dB gain is:

$$A_{pdB} = 10 \log A \quad (\text{Eq. 3-5})$$

Example 3-1

An amplifier has a voltage gain of 200. Calculate the dB voltage gain.

$$A_{vdB} = 20 \log A_v = 20 \log 200 = 46\text{dB}$$

Example 3-2

What is the voltage gain of an amplifier whose dB voltage gain is 52?

$$A_{v\text{dB}} = 20 \log A_v$$

$$52 = 20 \log A_v$$

Solving for $\log A_v$:

$$\log A_v = \frac{52}{20} = 2.6$$

Therefore:

$$A_v = 10^{2.6} = 398.1$$

Conceptual Amplifier Models

A block diagram of a voltage amplifier is provided in Figure 3-1A. Here, the signal to be amplified, v_{IN} , is applied to the input terminal, and the amplified output signal, v_{O} , appears at the output terminal. Since the amplifier has a voltage gain, A_v , the output voltage equals v_{IN} times A_v .

A voltage source model for the amplifier in Figure 3-1A is shown in Figure 3-1B. Note that:

1. The amplifier is driven by a signal source whose Thevenin source resistance equals R_S .
2. The amplifier drives a load device, whose resistance equals R_L .
3. The amplifier has an effective input resistance R_{IN} . This is the load seen by the signal source when it is connected to the amplifier.
4. The amplifier has an effective output resistance, R_{O} . When viewed from the load device, the amplifier acts like a voltage source whose Thevenin voltage equals $A_v v_{\text{IN}}$ and whose Thevenin resistance equals R_{O} .

Since a voltage source can be converted to an equivalent current source, it is also possible to model the amplifier as shown in Figure 3-1C.

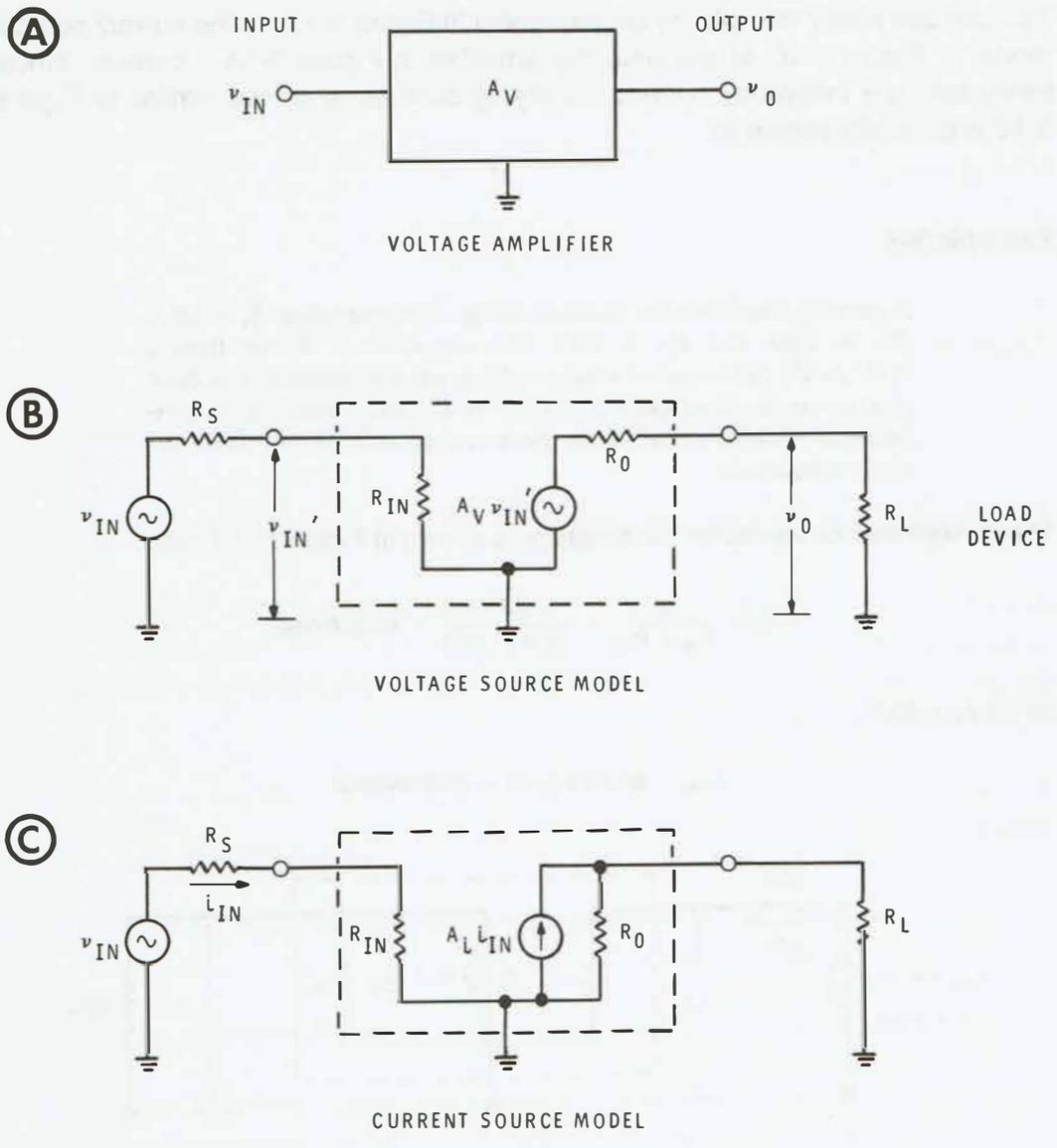


Figure 3-1

Voltage and current source models for a voltage amplifier.

- A. Voltage amplifier.
- B. Voltage source model.
- C. Current source model.

In this case, when viewed from the load device, the amplifier acts like a current source whose Norton current equals $A_i i_{IN}$, and whose Norton resistance equals R_O .

You can use either the voltage source model in Figure 3-1B, or the current source model in Figure 3-1C to evaluate the amplifier in Figure 3-1A. However, since transistors are inherently current amplifying devices, a model similar to Figure 3-1C is generally preferred.

Example 3-3

A certain amplifier has the following characteristics: $A_i = 66.7$, $R_{IN} = 2k\Omega$, and $R_O = 3k\Omega$. The amplifier is driven from a 0.1V peak, 1kHz signal source whose source resistance is 50Ω . Assuming the load device, driven by the amplifier, has a resistance of $100k\Omega$, calculate the peak output voltage and the effective voltage gain.

The current source model for the amplifier is shown in Figure 3-2. Here:

$$i_{IN} = \frac{v_{IN}}{R_S + R_{IN}} = \frac{0.1V}{50\Omega + 2k\Omega} = 48.8\mu A \text{ peak}$$

Since $A_i = 66.7$

$$A_i i_{IN} = 66.7(48.8\mu A) = 3.25mA \text{ peak}$$

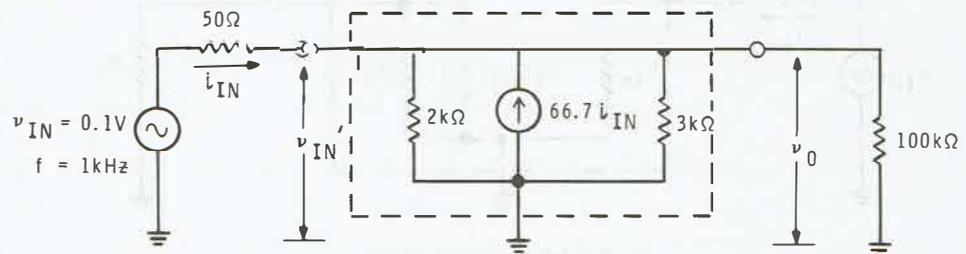


Figure 3-2

Circuit for Example 3-3.

The 3.25mA from the current source divides between the $3k\Omega$ output resistance, and the $100k\Omega$ load resistance. Using current division, the load current i_L is:

$$i_L = \frac{3.25\text{mA}(3k\Omega)}{103k\Omega} = 0.095\text{mA peak}$$

Thus, the load voltage is:

$$v_L = i_L R_L = 0.095\text{mA}(100k\Omega) = 9.5\text{V peak}$$

Since $v_{IN} = 0.1\text{V}$ and $v_O = 9.5\text{V} = v_L$ the effective voltage gain from the source to the load is:

$$A_V = \frac{v_O}{v_{IN}} = \frac{9.5\text{V}}{0.1\text{V}} = 95$$

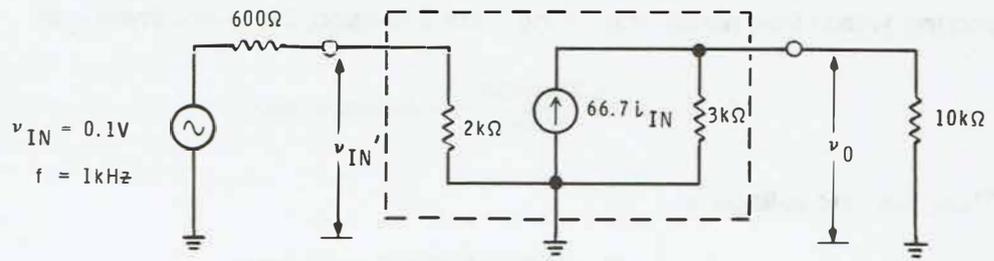


Figure 3-3

Circuit for Example 3-4.

Example 3-4

Rework Example 3-3 assuming $R_S = 600\Omega$, and $R_L = 10k\Omega$.

In this case, the current source model appears as shown in Figure 3-3. Here:

$$i_{IN} = \frac{v_{IN}}{R_S + R_{IN}} = \frac{0.1V}{600\Omega + 2k\Omega} = 38.5\mu A \text{ peak}$$

Since $A_i = 66.7$

$$A_i i_{IN} = 66.7(38.5\mu A) = 2.57mA \text{ peak}$$

The portion of the 2.57mA that flows through the 10kΩ load resistance is, via current division:

$$i_L = \frac{2.57mA(3k\Omega)}{13k\Omega} = 0.593mA \text{ peak}$$

The load voltage is therefore:

$$v_L = i_L R_L = 0.593mA(10k\Omega) = 5.93V \text{ peak}$$

Since $v_{IN} = 0.1V$ and $v_O = 5.93V$ the effective voltage gain from the source to the load is:

$$A_V = \frac{v_O}{v_{IN}} = \frac{5.93V}{0.1V} = 59.3$$

There are two reasons why the voltage gain from the signal source to the load in Example 3-4 is less than the corresponding voltage gain in Example 3-3. Let's consider each reason separately.

Input Resistance

The load seen by the signal source when it is connected to the input terminals of the amplifier is the amplifier's input resistance, R_{IN} . Since the signal source has an output resistance, R_S , the portion of the input voltage, v_{IN} , that is actually applied to the input terminals of the amplifier, v_{IN}' , is via voltage division:

$$v_{IN}' = \frac{v_{IN} R_{IN}}{R_S + R_{IN}} \quad (\text{Eq. 3-6})$$

If the amplifier's input resistance is small compared to the output resistance of the signal source, then only a fraction of the input voltage, v_{IN} , will actually be developed across the input terminals of the amplifier. In such a case, the amplifier is said to load the signal source.

To illustrate the concept, we will calculate the actual input voltages for the amplifiers in Figure 3-2 and Figure 3-3 respectively.

In Figure 3-2:

$$v_{IN}' = \frac{v_{IN} R_{IN}}{R_S + R_{IN}} = \frac{0.1\text{V}(2\text{k}\Omega)}{50\Omega + 2\text{k}\Omega} = 97.5\text{mV}$$

Since 97.5mV is 97.5% of 0.1V, it is obvious that most of the input voltage is developed across the amplifier's input terminals.

Similarly, in Figure 3-3.

$$v_{IN}' = \frac{v_{IN} R_{IN}}{R_S + R_{IN}} = \frac{0.1\text{V}(2\text{k}\Omega)}{600\Omega + 2\text{k}\Omega} = 76.9\text{mV}$$

In this case, only 76.9% of the input voltage is developed across the amplifier's input terminals. The remaining 24.1% is dropped across the output resistance of the signal source. Since the signal voltage is decreased, when the amplifier loads the signal source, the effective voltage gain from the signal source to the load also decreases.

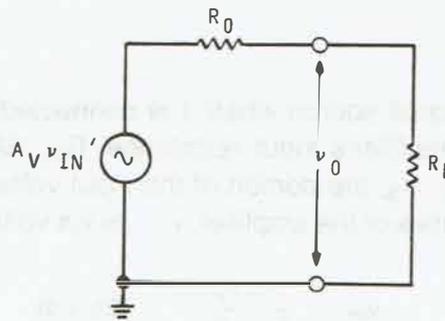


Figure 3-4

Voltage source model for the output portion of an amplifier.

Output Resistance

A voltage source model for an amplifier was provided earlier in Figure 3-1B. The output portion of this model is repeated in Figure 3-4. Note that the portion of the amplified signal voltage, $A_V v_{IN}'$, that is actually developed across the load terminals, v_O , is via voltage division:

$$v_O = \frac{A_V v_{IN}' (R_L)}{R_O + R_L} \quad (\text{Eq. 3-7})$$

If the load resistance is small compared to the amplifier's output resistance, only a fraction of the amplified signal voltage, $A_V v_{IN}'$, will actually be developed across the load terminals. In other words, a small value of R_L loads the amplifier output, in much the same way that a small value of R_{IN} loads the signal source. Naturally, this output loading effect reduces the effective voltage gain from the signal source to the load.

Based on the previous discussion, it is apparent that the following characteristics are desirable for a voltage amplifier.

1. **A large input resistance, R_{IN} .** This minimizes the loading of the signal source by the amplifier. In addition, a large value of R_{IN} reduces the current supplied by the signal source to the amplifier. This is also desirable.
2. **A small output resistance, R_O .** This minimizes the loading of the amplifier by the load resistance, R_L .
3. **High voltage gain, A_V .** This implies that the amplifier can be used to amplify small signal voltages with a minimum number of amplifying stages required.

Coupling Techniques

In practical amplifiers, some means must be used to connect the input signal to the amplifier and extract the amplified signal from the amplifier. The methods used to do this are called coupling techniques.

Possible coupling circuits are illustrated in Figure 3-5. A brief description of each circuit follows:

DIRECT COUPLING

As shown in Figure 3-5A, the signal source is connected directly to the amplifier's input terminal, and the load is connected directly to the amplifier's output terminal. Direct coupling is used in amplifiers designed to amplify DC, or low frequency AC signals.

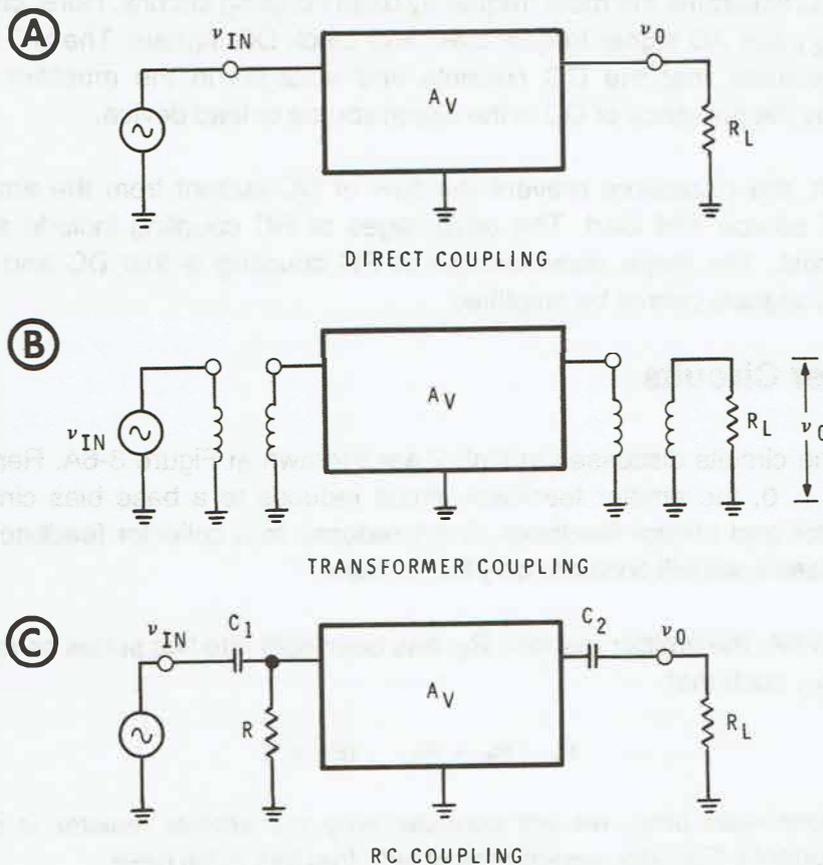


Figure 3-5

Coupling techniques.

- A. Direct coupling.
- B. Transformer coupling.
- C. RC coupling.

Since direct coupled amplifiers can amplify DC signals, changes in the DC supply voltage, V_{BE} , and other DC quantities tend to be amplified along with the signal voltage. Undesired amplification is termed **drift**. Drift is the principle disadvantage of direct coupling.

TRANSFORMER COUPLING

As shown in Figure 3-5B, the input and output signals can be coupled through transformers. Since transformers are highly efficient devices, this form of coupling is also very efficient. The disadvantages of transformer coupling include the relatively high cost, size, and weight of suitable transformers for audio frequency applications. In addition, the inductive characteristics of the transformer limit the range of frequencies that can be amplified.

RC COUPLING

Figure 3-5C illustrates the most frequently used coupling circuits. Here, capacitors C_1 and C_2 pass AC signal frequencies, and block DC signals. The DC blocking function ensures that the DC currents and voltages in the amplifier are not changed by the presence of DC in the signal source or load device.

In addition, the capacitors prevent the flow of DC current from the amplifier to the signal source and load. The advantages of RC coupling include simplicity and low cost. The major disadvantage of RC coupling is that DC and low frequency AC signals cannot be amplified.

Amplifier Circuits

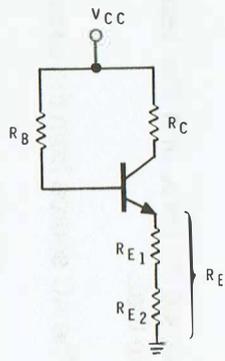
The biasing circuits discussed in Unit 2 are redrawn in Figure 3-6A. Remember, when $R_E = 0$, the emitter feedback circuit reduces to a base bias circuit, and the collector and emitter feedback circuit reduces to a collector feedback circuit. For this reason, we will consider only four circuits.

In Figure 3-6A, the emitter resistor, R_E , has been split into two series components, R_{E_1} and R_{E_2} , such that:

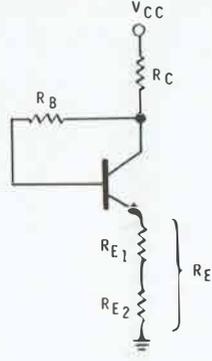
$$R_E = R_{E_1} + R_{E_2} \quad (\text{Eq. 3-8})$$

At the appropriate time, we will consider why the emitter resistor is split into two components. For now, we will simply note that this is the case.

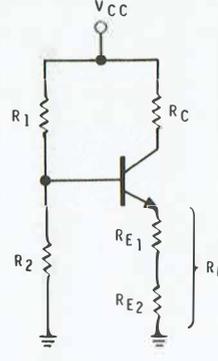
(A) TYPICAL BIASING CIRCUIT



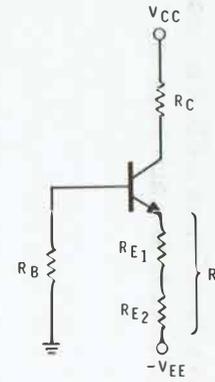
EMITTER FEEDBACK BIAS



COLLECTOR AND EMITTER FEEDBACK BIAS



VOLTAGE DIVIDER BIAS



EMITTER BIAS

(B) TYPICAL VOLTAGE AMPLIFIERS

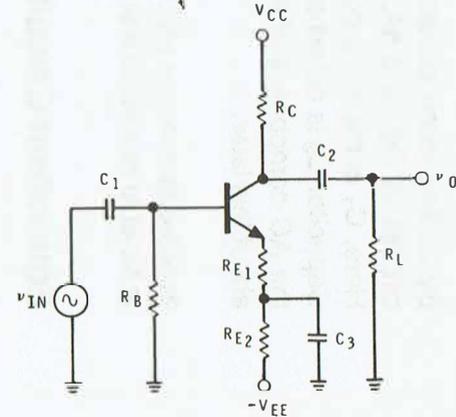
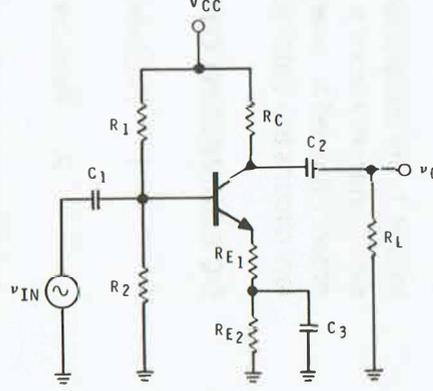
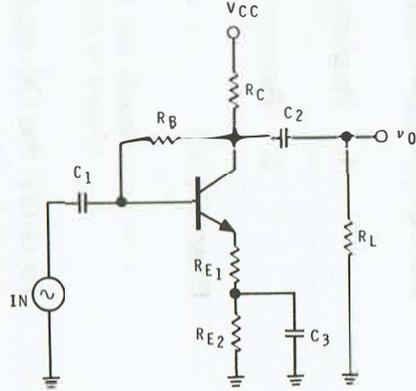
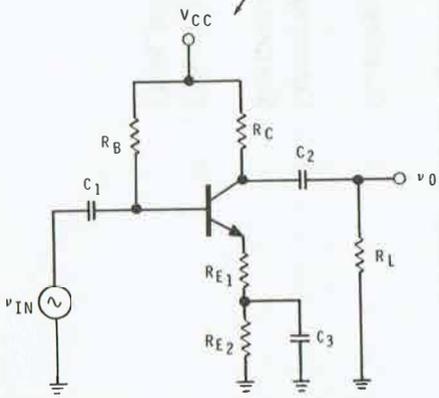


Figure 3-6

Common-emitter biasing and amplifier circuits.

- A. Typical biasing circuits.
- B. Typical voltage amplifiers.

By adding three capacitors, a signal source, and a load resistor to the biasing circuits in Figure 3-6A, you obtain the amplifier circuits shown in Figure 3-6B. Here, C_1 is the input coupling capacitor, and C_2 is the output coupling capacitor. Capacitor C_3 is called an **emitter bypass capacitor** because it is used to bypass the AC component of the emitter current around R_{E2} . We will have more to say about this later.

In order to analyze and design the amplifier circuits in Figure 3-6B, it is necessary to be able to visualize the DC and AC equivalent circuits for each amplifier.

Equivalent Circuits

In Unit 1, the superposition theorem was employed to analyze diode circuits driven simultaneously from a large DC and small AC source. Essentially the same approach is used to analyze transistor circuits. Specifically, the DC and AC equivalent circuits are obtained as follows:

DC EQUIVALENT CIRCUIT

1. Replace coupling and bypass capacitors by open circuits.
2. Reduce AC sources to zero.

AC EQUIVALENT CIRCUIT

1. Replace coupling and bypass capacitors by short circuits.
2. Reduce all DC sources to zero.

Example 3-5

Sketch the DC and AC equivalent circuits for the amplifier shown in Figure 3-7A.

To obtain the DC equivalent circuit v_{IN} is reduced to zero, and the capacitors are replaced by open circuits. In Figure 3-7A note that:

1. Opening C_1 effectively removes the AC source from the circuit.
2. Opening C_2 effectively removes the $10k\Omega$ load resistance from the circuit.
3. Opening C_3 places the $1k\Omega$ and $0.5k\Omega$ emitter resistors in series. Thus, the equivalent DC emitter resistance is $1.5k\Omega$.

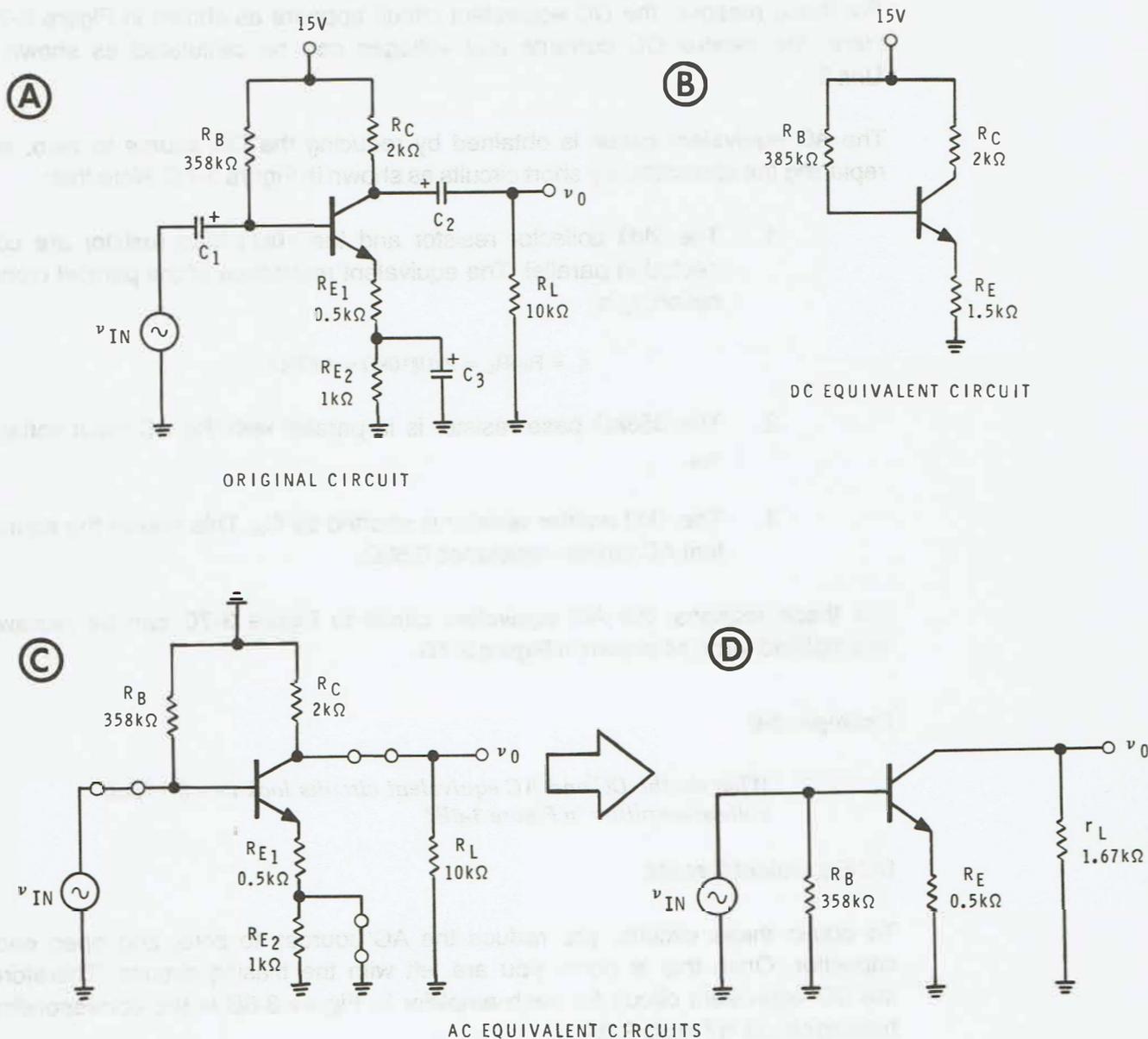


Figure 3-7

AC equivalent circuits.

- A. Original circuit.
- B. DC equivalent circuit.
- C. AC equivalent circuits.

For these reasons, the DC equivalent circuit appears as shown in Figure 3-7B. Here, the various DC currents and voltages can be calculated as shown in Unit 2.

The AC equivalent circuit is obtained by reducing the DC source to zero, and replacing the capacitors by short circuits as shown in Figure 3-7C. Note that:

1. The $2\text{k}\Omega$ collector resistor and the $10\text{k}\Omega$ load resistor are connected in parallel. The equivalent resistance of the parallel combination, r_L is:

$$r_L = R_C \parallel R_L = 2\text{k}\Omega \parallel 10\text{k}\Omega = 1.67\text{k}\Omega$$

2. The $358\text{k}\Omega$ base resistor is in parallel with the AC input voltage, v_{IN} .
3. The $1\text{k}\Omega$ emitter resistor is shorted by C_3 . This makes the equivalent AC emitter resistance $0.5\text{k}\Omega$.

For these reasons, the AC equivalent circuit in Figure 3-7C can be redrawn, in simplified form, as shown in Figure 3-7D.

Example 3-6

What do the DC and AC equivalent circuits look like for each voltage amplifier in Figure 3-6B?

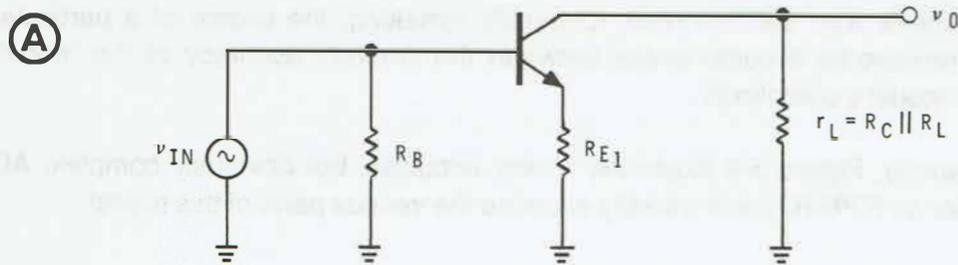
DC Equivalent Circuits

To obtain these circuits, you reduce the AC sources to zero, and open each capacitor. Once this is done, you are left with the biasing circuits. Therefore, the DC equivalent circuit for each amplifier in Figure 3-6B is the corresponding biasing circuit in Figure 3-6A.

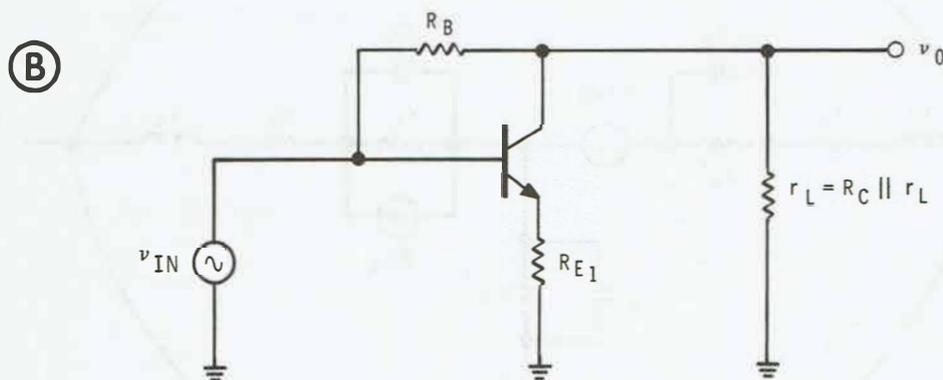
AC Equivalent Circuits

To obtain these circuits, you reduce the DC sources to zero, and replace the capacitors with short circuits. By following this procedure, you obtain the AC equivalent circuits shown in Figure 3-8. Notice that the emitter feedback, voltage divider, and emitter-bias amplifier circuits all reduce to the same AC equivalent circuit.

Once V_{CC} is reduced to zero in a voltage divider-type amplifier, the biasing resistors R_1 and R_2 are connected in parallel. For this reason, the value of R_B in the AC equivalent circuit equals $R_1 \parallel R_2$.



AC EQUIVALENT CIRCUIT FOR THE EMITTER FEEDBACK, VOLTAGE DIVIDER, AND EMITTER-BIAS AMPLIFIER CIRCUITS IN FIGURE 3-6B. IN THE CASE OF THE VOLTAGE DIVIDER-TYPE AMPLIFIER $R_B = R_1 || R_2$.



AC EQUIVALENT CIRCUIT FOR THE COLLECTOR AND EMITTER FEEDBACK AMPLIFIER CIRCUIT IN FIGURE 3-6B.

Figure 3-8

Common emitter amplifier AC equivalent circuits.

- A. AC equivalent circuit for the emitter feedback, voltage divider, and emitter-bias amplifier circuits in Figure 3-6B. In the case of the voltage divider-type amplifier $R_B = R_1 || R_2$.
- B. AC equivalent circuit for the collector and emitter feedback amplifier circuit in Figure 3-6B.

AC Transistor Models

In order to analyze transistor AC equivalent circuits, you need an AC model for the transistor. A large number of BJT AC models have been developed since the transistor was first invented. Generally speaking, the choice of a particular model represents a compromise between the inherent accuracy of the model, and the model's complexity.

For example, Figure 3-9 illustrates a very accurate, but obviously complex, AC model for an NPN BJT. Let's briefly examine the various parts of this model.

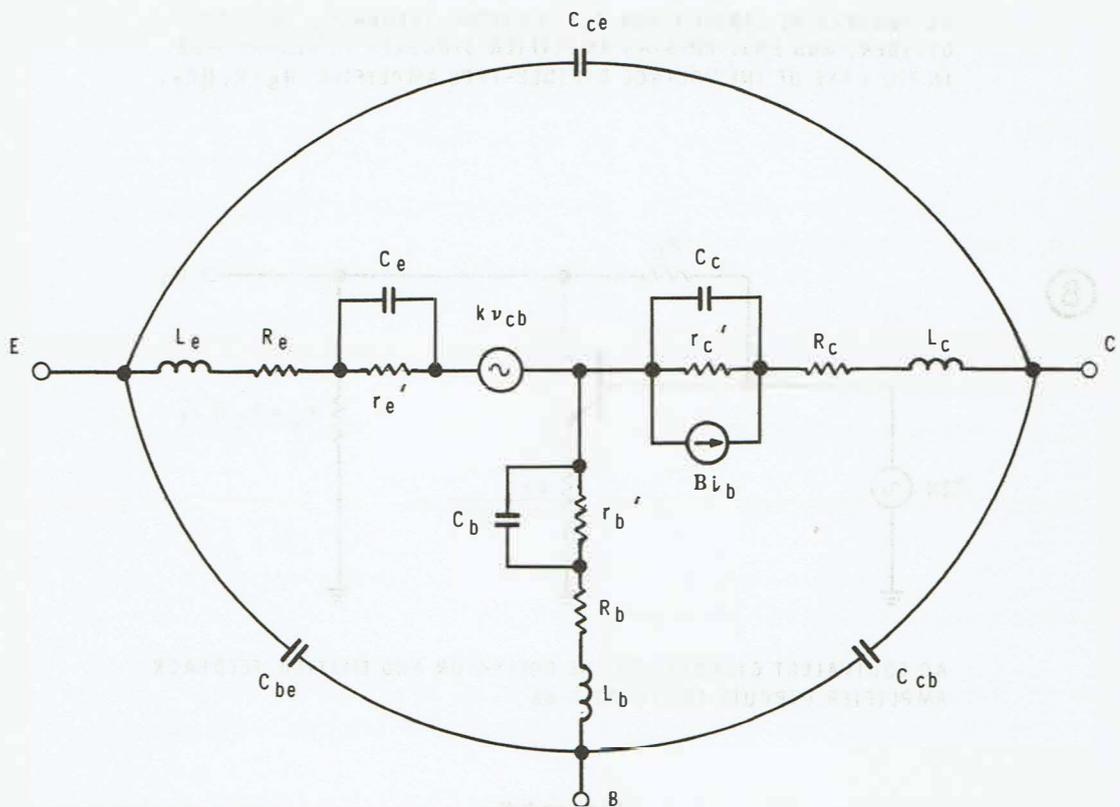


Figure 3-9

A reasonably complete AC transistor model.

The use of lower case subscripts generally indicates an AC quantity. To avoid confusing DC and AC quantities, we will use capital letters for DC quantities, and lower case letters for AC quantities. For example, V_{CE} denotes the DC collector-to-emitter voltage and v_{ce} denotes the AC collector-to-emitter voltage.

r_e' — Essentially, this represents the junction resistance of the forward biased emitter-base diode. Ideally, $r_e' = r_j = 26\text{mV}/I_E$. Since there are wide unit-to-unit variations in the value of r_e' , we will use the following compromise formula for purposes of calculation:

$$r_e' = r_j = \frac{37\text{mV}}{I_E} \quad (\text{Eq. 3-9})$$

r_b' — This component of the resistance in the base leg is called the base-spreading resistance. The value of r_b' depends upon the construction details of the transistor, doping levels, etc. For general purpose transistors, r_b' is usually less than 200Ω .

r_c' — This is the AC resistance of the reverse biased collector-base diode. Typically, r_c' has a value in excess of $1\text{M}\Omega$.

R_e, R_b, R_c — These represent the ohmic, contact, and lead resistances of the internal emitter, base, and collector portions of the BJT.

L_e, L_b, L_c — These represent the emitter, base, and collector lead inductances.

C_e, C_b, C_c — These represent internal shunt capacitance.

C_{ce}, C_{be}, C_{cb} — These are the terminal-to-terminal capacitances. Such capacitances vary with lead length, case types, etc.

κv_{cb} — The output voltage of a BJT has a small effect on the base current. To account for this the dependent voltage source, κv_{cb} , is included in the model.

βi_b — This dependent current source is used to account for the current amplifying properties of the BJT.

Fortunately, for most applications, a BJT model as complex as the model in Figure 3-9 is not necessary. In fact, for low and mid-frequency applications, the greatly simplified BJT model in Figure 3-10 is usually adequate. Naturally, at high enough frequencies the various reactive elements in Figure 3-9 cannot be neglected. We will have more to say about this in Unit 9 when high frequency effects are discussed in detail.

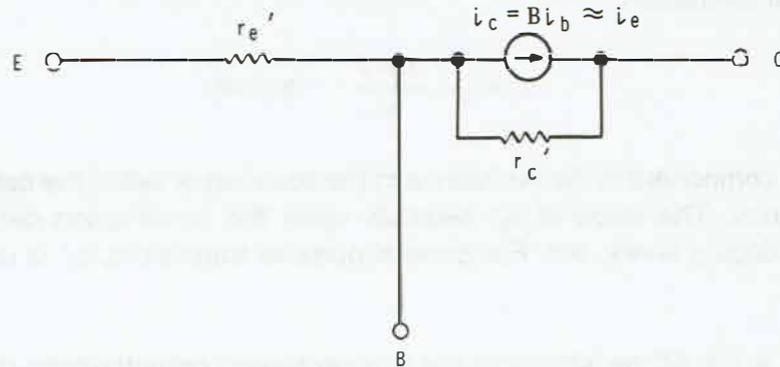


Figure 3-10

Simplified AC transistor model.

AC Parameters

The most useful AC or small signal BJT parameters include B , α , and r_e' . In Unit 1 B and α were defined as:

$$B = \frac{I_C}{I_B} \text{ and } \alpha = \frac{I_C}{I_E}$$

where I_B , I_E , and I_C represented DC quantities. Also, recall that:

$$h_{FE} = B, B = \frac{\alpha}{1 - \alpha} \text{ and } \alpha = \frac{B}{B + 1}$$

The AC values of B and α are defined in terms of **ratios of current changes** rather than DC values. Specifically:

$$B_{AC} = \frac{\Delta I_C}{\Delta I_B} \text{ and } \alpha_{AC} = \frac{\Delta I_C}{\Delta I_E}$$

Here, the symbol Δ means "a small change in."

Although the DC and AC values of B are usually close in value they are not equal. Consequently, to distinguish between a BJT's DC and AC B values, BJT data sheets normally use the following notation:

$$\text{DC } B = h_{FE} \text{ and AC } B = h_{fe}$$

Remember, to avoid confusing DC and AC quantities, we will use capital letters for DC quantities and lower-case letters for AC quantities.

Self-Test Review

1. An amplifier whose voltage gain is 100 has a dB voltage gain of _____ dB.
2. A dB voltage gain of 30 corresponds to a regular voltage gain of _____.
3. To avoid loading the signal source, an amplifier's input resistance should be _____ compared to the output resistance of the signal source.
large or small
4. To avoid loading the output of an amplifier, the load resistance should be _____ compared to the amplifier's output resistance.
large or small
5. The most frequently used coupling technique in BJT circuits is _____ coupling.
6. In the AC equivalent circuit, coupling and bypass capacitors are replaced by _____ circuits.
open or short
7. In the DC equivalent circuit, coupling and bypass capacitors are replaced by _____ circuits.
open or short
8. Assuming $I_{CQ} = 1\text{mA}$ and $V_{CEQ} = 6\text{V}$ the value of r_e' is approximately _____ Ω .

9. In Figure 3-11 the AC load resistance is _____ $k\Omega$.
10. In Figure 3-11 the AC emitter resistance is _____ Ω .

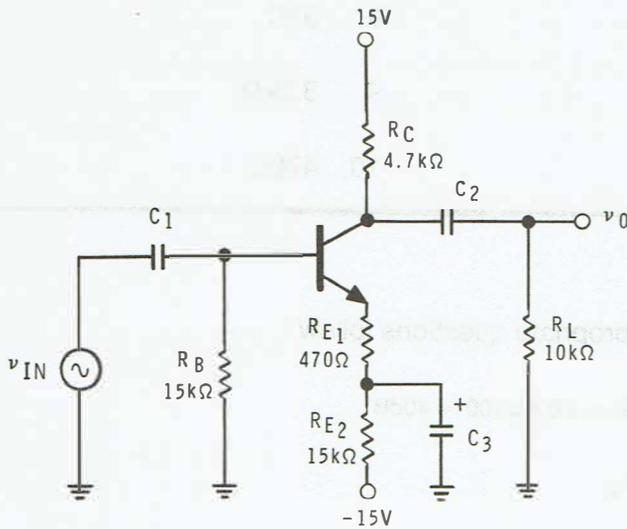


Figure 3-11

Circuit for Self-Test Review questions 9 and 10.

Answers

- | | |
|----------|-----------------|
| 1. 40 | 6. short |
| 2. 31.6 | 7. open |
| 3. large | 8. 37Ω |
| 4. large | 9. $3.2k\Omega$ |
| 5. RC | 10. 470Ω |

The solutions to appropriate questions follow:

$$1. \quad A_{v_{dB}} = 20 \log A_v = 20 \log 100 = 40\text{dB}$$

$$2. \quad \begin{aligned} A_{v_{dB}} &= 20 \log A_v \\ 30 &= 20 \log A_v \\ \log A_v &= \frac{30}{20} = 1.5 \end{aligned}$$

Thus:

$$A_v = 10^{1.5} \text{ or } 31.6$$

8. Since $I_{CQ} = 1\text{mA}$, I_E is essentially 1mA . Using the compromise formula for r_e' you have:

$$r_e' = \frac{37\text{mV}}{I_E} = \frac{37\text{mV}}{1\text{mA}} = 37\Omega$$

9. In the AC equivalent circuit, Figure 3-8A, $r_L = R_C \parallel R_L$. Therefore:

$$r_L = 4.7k\Omega \parallel 10k\Omega = \frac{4.7k\Omega(10k\Omega)}{4.7k\Omega + 10k\Omega} = 3.2k\Omega$$

10. In the AC equivalent circuit, Figure 3-8A, the AC emitter resistance equals R_{E_1} . Thus:

$$R_{E_{AC}} = R_{E_1} = 470\Omega$$

ANALYSIS OF COMMON EMITTER AMPLIFIERS

In this section, we will use the AC equivalent circuits and simplified AC BJT model to derive a number of formulas useful for the analysis and design of common-emitter voltage amplifiers.

In addition, we will discuss Miller's theorem. As you will see, Miller's theorem is especially useful for analyzing amplifiers that use collector feedback in their biasing schemes. Finally, formulas will be provided to simplify the analysis process.

Emitter Feedback, Voltage Divider, and Emitter Bias-Type Amplifiers.

Look at the AC equivalent circuit in Figure 3-12A. By replacing the transistor with the simplified AC BJT model of Figure 3-12B, you obtain the circuit shown in Figure 3-12C. Since r_c' is usually large enough to neglect, we have not included it in the AC equivalent circuit of Figure 3-12B.

By starting at the base terminal and following the path indicated by the dotted lines in Figure 3-12C, the following loop equation can be written:

$$v_{IN} - i_e R_{E_1} - i_e r_{e'} = 0$$

Solving for the AC emitter current, i_e , yields:

$$i_e = \frac{v_{IN}}{R_{E_1} + r_{e'}} \approx i_c \quad (\text{Eq. 3-10})$$

In Figure 3-12C, note that the AC collector current, i_c , flows through the AC load resistance, r_L . Here, the direction of i_c is such that when v_{IN} is positive v_O is negative. Therefore, via Ohm's law:

$$v_O = v_c = \frac{-v_{IN}}{R_{E_1} + r_{e'}} r_L \quad (\text{Eq. 3-11})$$

The negative sign in Equation 3-11 simply indicates that v_{IN} and v_O are 180° out of phase with each other.

Recall that the voltage gain, A_V , is the ratio of v_O to v_{IN} . Solving Equation 3-11 for this ratio, you obtain:

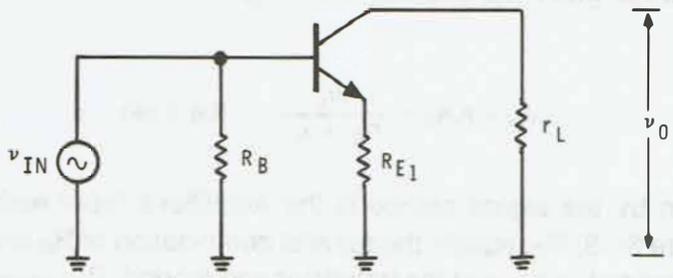
$$A_V = \frac{-r_L}{R_{E_1} + r_{e'}} \quad (\text{Eq. 3-12})$$

Once again, the negative sign indicates that v_O and v_{IN} are 180° out of phase with each other.

Since the output current is i_c and the input current is i_b the current gain, A_i , is:

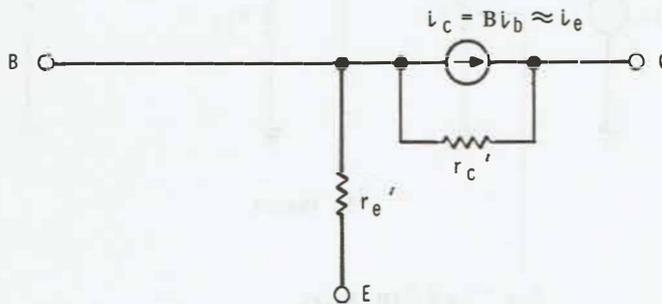
$$A_i = \frac{i_c}{i_b} = \beta = h_{fe} \quad (\text{Eq. 3-13})$$

(A)



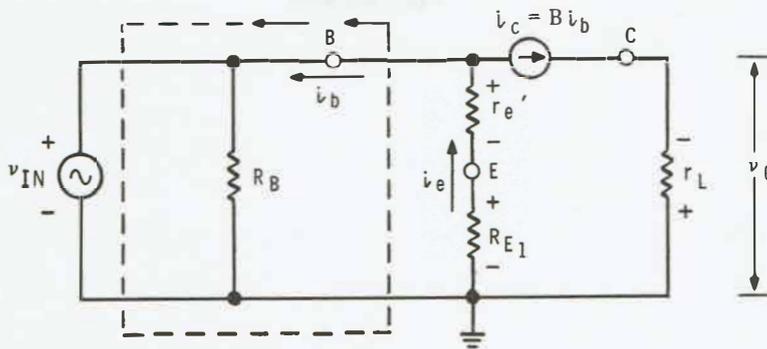
AC EQUIVALENT CIRCUIT

(B)



SIMPLIFIED AC TRANSISTOR MODEL

(C)



AC EQUIVALENT CIRCUIT WITH SIMPLIFIED BJT MODEL.

Figure 3-12

AC models for the emitter feedback, voltage divider, and emitter-bias common emitter amplifiers.

- A. AC equivalent circuit.
- B. Simplified AC transistor model.
- C. AC equivalent circuit with simplified BJT model.

To find the power gain, A_p , multiply the magnitude of the current and voltage gains. Thus:

$$A_p = A_i A_v = \frac{\beta r_L}{R_{E_1} + r_{e'}} \quad (\text{Eq. 3-14})$$

The load seen by the signal source is the amplifier's input resistance, R_{IN} . As shown in Figure 3-13, R_{IN} equals the parallel combination of R_B and the equivalent resistance between the base of the transistor and ground, $R_{IN(\text{BASE})}$.

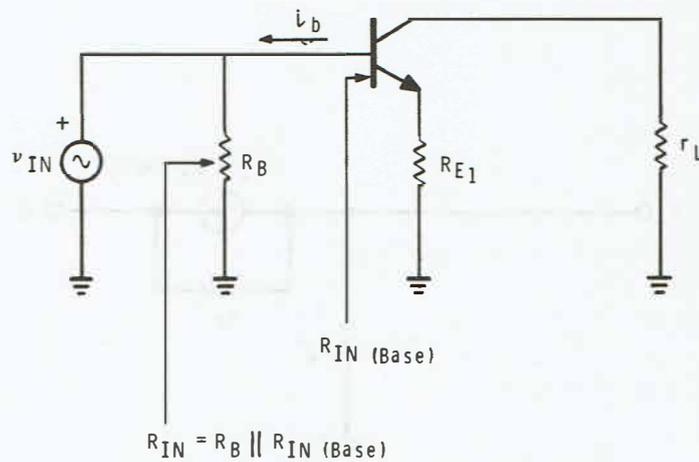


Figure 3-13

Input resistance.

In Figure 3-13 note that the voltage between the base of the transistor and ground, v_b , equals v_{IN} . Also, since the base current is i_b Ohm's law can be used to calculate the value of $R_{IN(BASE)}$ as follows:

$$R_{IN(BASE)} = \frac{v_b}{i_b} = \frac{v_{IN}}{i_b} \quad (\text{Eq. 3-15})$$

From Equation 3-10 on Page 3-30, you know that:

$$i_c = \frac{v_{IN}}{R_{E_1} + r_{e'}}$$

Since $i_b = \frac{i_c}{B}$:

$$i_b = \frac{v_{IN}}{B(R_{E_1} + r_{e'})} \quad (\text{Eq. 3-16})$$

Substituting Equation 3-16 into Equation 3-15 yields:

$$R_{IN(BASE)} = B(R_{E_1} + r_{e'})$$

Consequently, the input resistance of the amplifier is:

$$R_{IN} = R_B \parallel R_{IN(BASE)} = R_B \parallel B(R_{E_1} + r_{e'}) \quad (\text{Eq. 3-17})$$

Dependent sources, like $B i_b$, complicate the process of calculating the output resistance of an amplifier. For this reason, we will not derive a formula for R_O .

In any event, the output resistance of common-emitter amplifiers is large. For most common-emitter amplifiers, you can assume $R_O \approx R_C$. Thus, loading of the amplifier's output will be minimum if $R_L \gg R_C$.

The following examples illustrate the analysis of typical common-emitter circuits.

Example 3-6

The BJT in Figure 3-14A has an h_{fe} of 150. Calculate the DC emitter current and DC terminal-to-ground voltages. Also estimate the input resistance, voltage gain, and the peak AC output voltage. (If necessary, refer to the common-emitter biasing and amplifier circuits in Figure 3-6.)

First you calculate the DC responses. By mentally opening the capacitors and reducing the AC source to zero, you obtain the DC equivalent circuit shown in Figure 3-14B. Here:

$$V_B = \frac{15V(10k\Omega)}{10k\Omega + 10k\Omega} = 7.5V$$

$$V_E = V_B - V_{BE} = 7.5V - 0.7V = 6.8V$$

$$I_E = \frac{V_E}{R_E} = \frac{6.8V}{6.8k\Omega} = 1mA$$

$$V_C = V_{CC} - I_C R_C$$

$$V_C = 15V - 1mA(3k\Omega) = 12V$$

Next you calculate the AC responses. If you replace the capacitors with short circuits, and reduce the DC source to zero, you have the AC equivalent circuit shown in Figure 3-14C. Here, note that:

$$r_L = R_C || R_L = 3k\Omega || 1M\Omega \approx 3k\Omega$$

Since the $10\mu F$ bypass capacitor shorts out the entire $6.8k\Omega$ emitter resistor $R_E = 0$.

In addition, since $I_E = 1mA$, r_e' is:

$$r_e' = \frac{37mV}{I_E} = 37\Omega$$

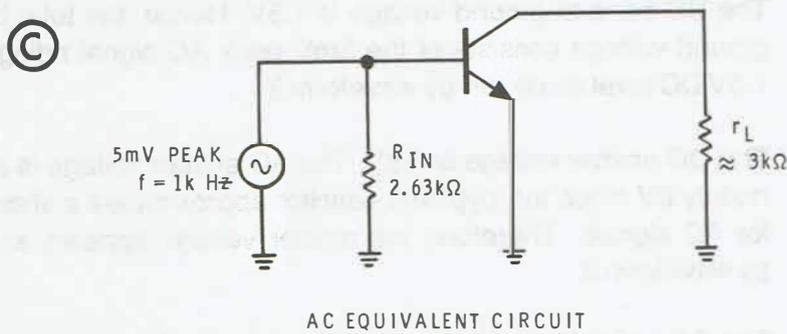
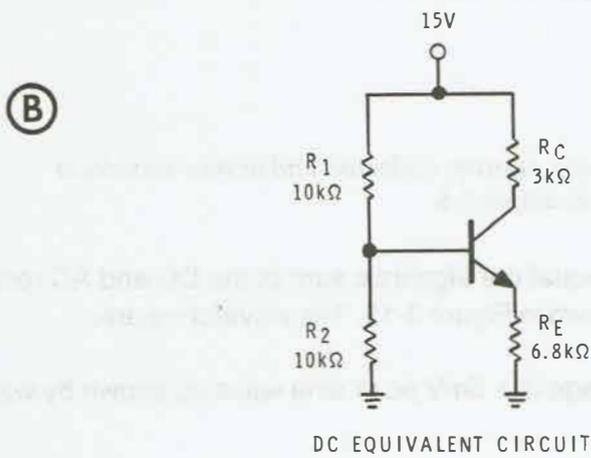
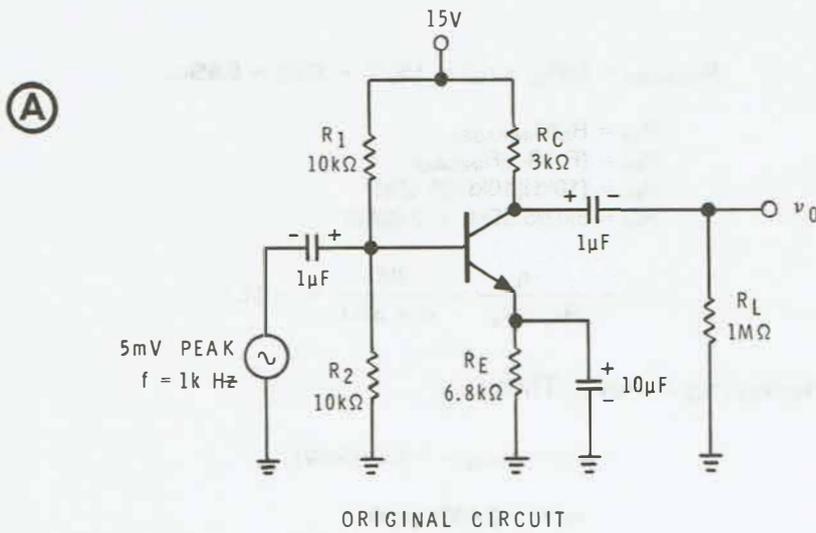


Figure 3-14

- Circuits for Example 3-6.
- A. Original circuit.
 - B. DC equivalent circuit.
 - C. AC equivalent circuit.

Therefore:

$$R_{IN(BASE)} = B(R_{E_1} + r_{e'}) = 150(0 + 37\Omega) = 5.55k\Omega$$

$$R_{IN} = R_B \parallel R_{IN(BASE)}$$

$$R_{IN} = (R_1 \parallel R_2) \parallel R_{IN(BASE)}$$

$$R_{IN} = (10k\Omega \parallel 10k\Omega) \parallel 5.55k\Omega$$

$$R_{IN} = 5k\Omega \parallel 5.55k\Omega = 2.63k\Omega$$

$$A_V = \frac{-r_L}{R_{E_1} + r_{e'}} = \frac{3k\Omega}{0 + 37\Omega} = -81.1$$

Since $A_V = v_O/v_{IN}$, $v_O = A_V v_{IN}$. Thus:

$$v_O = A_V v_{IN} = -81.1(5mV)$$

$$v_O = -0.405V \text{ peak}$$

The minus sign indicates that v_O and v_{IN} are 180° out of phase with each other.

Example 3-7

Sketch the input, base, emitter, collector, and output waveform for the amplifier in Example 3-6.

Since the actual responses equal the algebraic sum of the DC and AC responses the waveforms appear as shown in Figure 3-15. The waveforms are:

1. The input voltage is a 5mV peak sine wave as shown by waveform 1.
2. Since the input coupling capacitor approximates a short circuit for AC signals, the AC base-to-ground voltage equals v_{IN} or 5mV peak. The DC base-to-ground voltage is 7.5V. Hence, the total base-to-ground voltage consists of the 5mV peak AC signal riding on the 7.5V DC level as shown by waveform 2.
3. The DC emitter voltage is 6.8V. The AC emitter voltage is approximately 0V since the bypass capacitor approximates a short circuit for AC signals. Therefore, the emitter voltage appears as shown by waveform 3.
4. The AC collector voltage equals $A_V v_{IN}$ or 0.405V peak. Since the DC collector voltage is 12V, the total collector voltage appears as shown by waveform 4.

- The output coupling capacitor passes the AC component of the collector voltage, and blocks the DC component. Therefore, the output voltage appears as shown by waveform 5.

In Figure 3-15, you should also note the following:

- The input voltage is 10mV AC peak-to-peak.
- The input coupling capacitor charges to the DC base voltage.
- The bypass capacitor charges to the DC emitter voltage.
- The output coupling capacitor charges to the DC collector voltage.
- The input and output voltages are 180° out of phase with each other.

In many amplifiers, the coupling and bypass capacitors are electrolytic-type capacitors. Since electrolytic capacitors are usually polarized, you must make sure that they are connected into the circuit with the polarities as indicated in Figure 3-15.

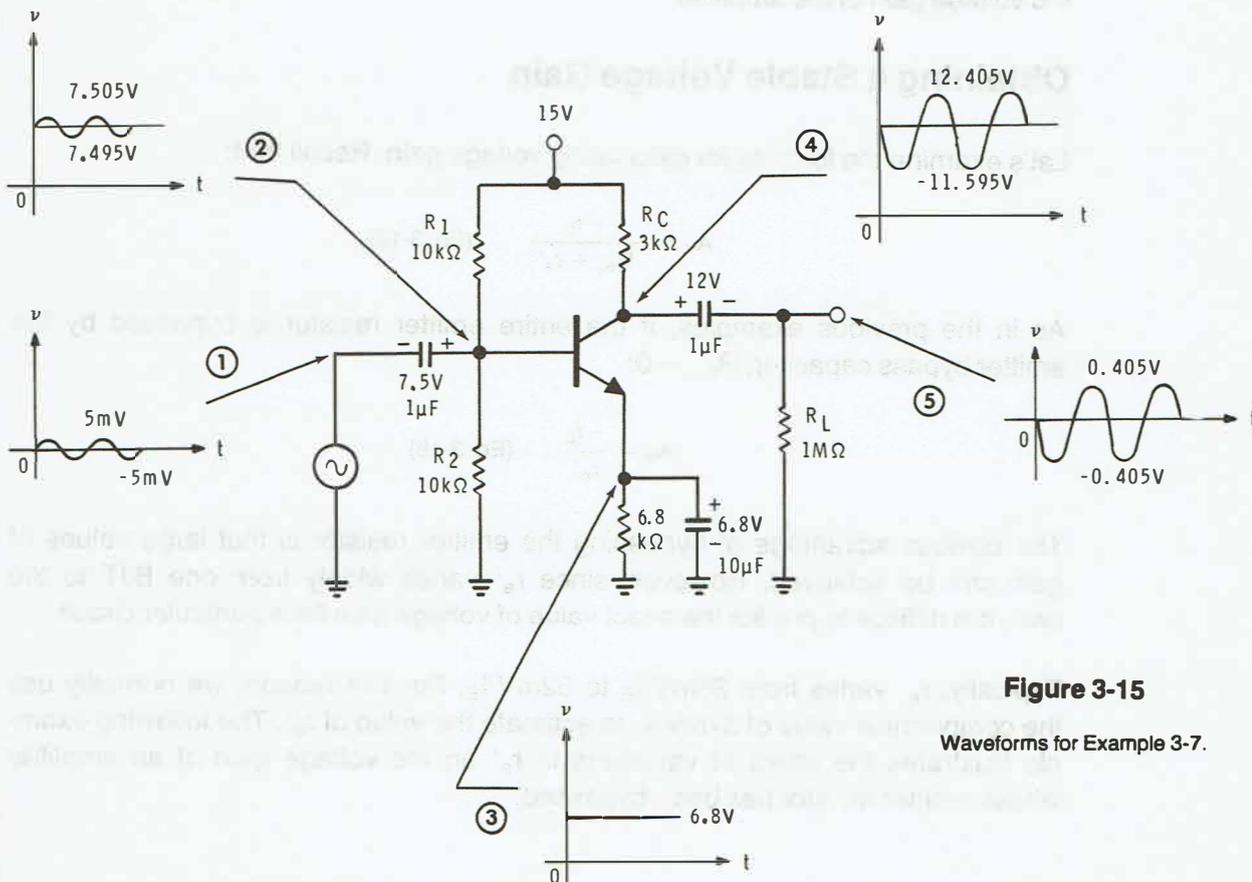


Figure 3-15

Waveforms for Example 3-7.

Example 3-8

What is the AC output voltage in Figure 3-14A if R_L is changed from $1M\Omega$ to $6k\Omega$?

The DC currents and voltages will be the same as in Example 3-6. Also, since I_E is $1mA$, r_e' is still approximately 37Ω . In this case, however the AC load resistance is:

$$r_L = R_C \parallel R_L = 3k\Omega \parallel 6k\Omega = 2k\Omega$$

Thus, the voltage gain is:

$$A_V = -\frac{r_L}{R_{E_1} + r_e'} = -\frac{2k\Omega}{0 + 37\Omega} = -54$$

Therefore, the peak AC output voltage is:

$$v_O = A_V v_{IN} = -54(5mV) = -0.27V$$

In this example, the load resistance, R_L , is small compared to the collector resistance, R_C . As a result, the AC load resistance, r_L , decreased. This, in turn, reduced the voltage gain of the amplifier.

Obtaining a Stable Voltage Gain

Let's examine the formula for calculating voltage gain. Recall that:

$$A_V = \frac{-r_L}{R_{E_1} + r_e'} \quad (\text{Eq. 3-12})$$

As in the previous examples, if the entire emitter resistor is bypassed by the emitter bypass capacitor, $R_{E_1} = 0$:

$$A_V = \frac{-r_L}{r_e'} \quad (\text{Eq. 3-18})$$

The obvious advantage of bypassing the emitter resistor is that large values of gain can be achieved. However, since r_e' varies widely from one BJT to the next, it is difficult to predict the exact value of voltage gain for a particular circuit.

Typically, r_e' varies from $26mV/I_E$ to $52mV/I_E$. For this reason, we normally use the compromise value of $37mV/I_E$ to estimate the value of r_e' . The following example illustrates the effect of variations in r_e' on the voltage gain of an amplifier whose emitter resistor has been bypassed.

Example 3-9

In Figure 3-15, the voltage gain was calculated to be -81.1 , based on the assumption that $r_e' = 37\text{mV}/I_E$. Estimate the voltage gain if $r_e' = 26\text{mV}/I_E$, and if $r_e' = 52\text{mV}/I_E$.

In Figure 3-15, $I_E = 1\text{mA}$ and $r_L = 3\text{k}\Omega$.

Assuming $r_e' = \frac{26\text{mV}}{I_E}$:

$$r_e' = \frac{26\text{mV}}{1\text{mA}} = 26\Omega$$

$$A_v = \frac{-r_L}{r_e'} = \frac{-3\text{k}\Omega}{26\Omega} = -115.4$$

Assuming $r_e' = \frac{52\text{mV}}{I_E}$:

$$r_e' = \frac{52\text{mV}}{1\text{mA}} = 52\Omega$$

$$A_v = \frac{-r_L}{r_e'} = \frac{-3\text{k}\Omega}{52\Omega} = -57.7$$

Clearly, if many amplifiers like the one in Figure 3-15 were constructed, you would expect to find wide variation in the unit-to-unit gains.

The standard techniques for stabilizing the voltage gain, with respect to variations in r_e' , is to bypass only a portion of the emitter resistor. In this case,

$$A_v = \frac{-r_L}{R_{E_1} + r_e'}$$

Obviously, if $R_{E_1} \gg r_e'$, variations in r_e' will only produce slight changes in A_v . In this way, the voltage gain effectively becomes independent of the value of r_e' . In addition, since $R_{IN(\text{BASE})} = \beta(R_{E_1} + r_e')$, the input resistance of the amplifier is increased. This, of course, is desirable.

Example 3-10

Figure 3-16 illustrates the amplifier we have been analyzing. In this case, however, the $6.8\text{k}\Omega$ emitter resistor has been split into two series components. If R_{E_2} is bypassed, calculate the voltage gain assuming $r_e' = 26\text{mV}/I_E$, $r_e' = 37\text{mV}/I_E$, and $r_e' = 52\text{mV}/I_E$ with $r_L = 3\text{k}\Omega$.

Since $I_E = 1\text{mA}$, the values of r_e' to be considered are 26Ω , 37Ω , and 52Ω respectively. In Figure 3-16, $R_{E_1} = 563\Omega$, and $r_L = 3\text{k}\Omega$. Thus:

When $r_e' = 26\Omega$:

$$A_v = \frac{-r_L}{R_{E_1} + r_e'} = \frac{-3\text{k}\Omega}{563\Omega + 26\Omega} = -5.09$$

When $r_e' = 37\Omega$:

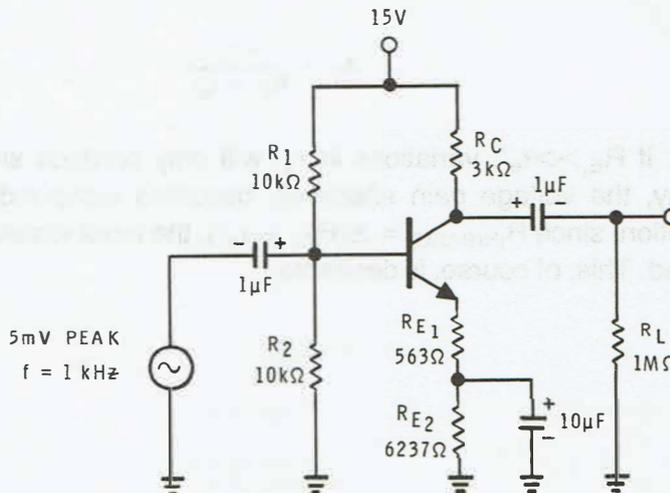
$$A_v = \frac{-r_L}{R_{E_1} + r_e'} = \frac{-3\text{k}\Omega}{563\Omega + 37\Omega} = -5$$

When $r_e' = 52\Omega$:

$$A_v = \frac{-r_L}{R_{E_1} + r_e'} = \frac{-3\text{k}\Omega}{563\Omega + 52\Omega} = -4.88$$

Comparing the results of Example 3-10 with those obtained in Example 3-9, you can see that the partially bypassed emitter resistor provides a very stable voltage gain. Obviously, to achieve this stability, you sacrifice a significant decrease in the value of the voltage gain.

Figure 3-16
Circuit for Example 3-10.



Collector and Emitter Feedback Amplifiers

The presence of collector feedback complicates the AC equivalent circuit. In order to simplify the analysis and design process we will first discuss Miller's theorem.

Figure 3-17A illustrates an inverting amplifier where a resistor, R , is connected between the input and output terminals. As far as the AC equivalent circuit is concerned, Miller's theorem lets you visualize the equivalent circuit shown in Figure 3-17B. Here, note that:

1. The input Miller resistance equals $\frac{R}{A_V + 1}$
2. The output Miller resistance equals $\frac{R A_V}{A_V + 1}$

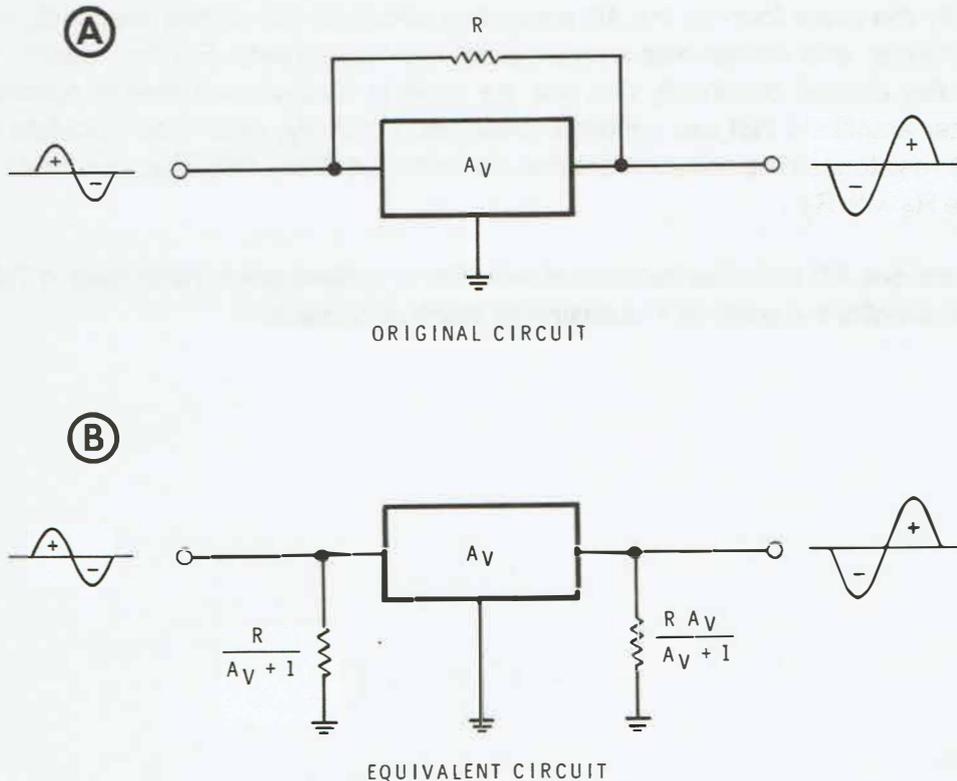


Figure 3-17

Miller's theorem.
 A. Original circuit.
 B. Equivalent circuit.

The magnitude of A_V is used to calculate the input and output Miller resistances. For example, if $A_V = -9$, and $R = 100\text{k}\Omega$, the input and output Miller resistances are:

$$R_{IN} = \frac{100\text{k}\Omega}{9 + 1} = 10\text{k}\Omega$$

$$R_O = \frac{100\text{k}\Omega(9)}{10} = 90\text{k}\Omega$$

Miller's theorem greatly simplifies the AC analysis of circuits with collector feedback. Figure 3-18 illustrates this concept. By applying Miller's theorem to the circuit in Figure 3-18A, you obtain the equivalent circuit shown in Figure 3-18B. Since the output Miller resistance is in parallel with r_L , the circuit can be simplified as shown in Figure 3-18C. Also, since R_B is usually a large resistance value, the parallel combination of r_L and the output Miller resistance is essentially equal to the value of r_L .

Especially important is the fact that the equivalent circuit in Figure 3-18C has exactly the same form as the AC equivalent circuit for the emitter feedback, voltage divider, and emitter-bias amplifiers analyzed previously. For this reason, the formulas derived previously can also be used to analyze and design common-emitter amplifiers that use collector feedback. Naturally, when you calculate the input resistance of a common-emitter, collector feedback amplifier, you must replace R_B with R_B' .

The various AC formulas for common-emitter amplifiers are summarized in Table 3-1 to simplify the analysis and design as much as possible.

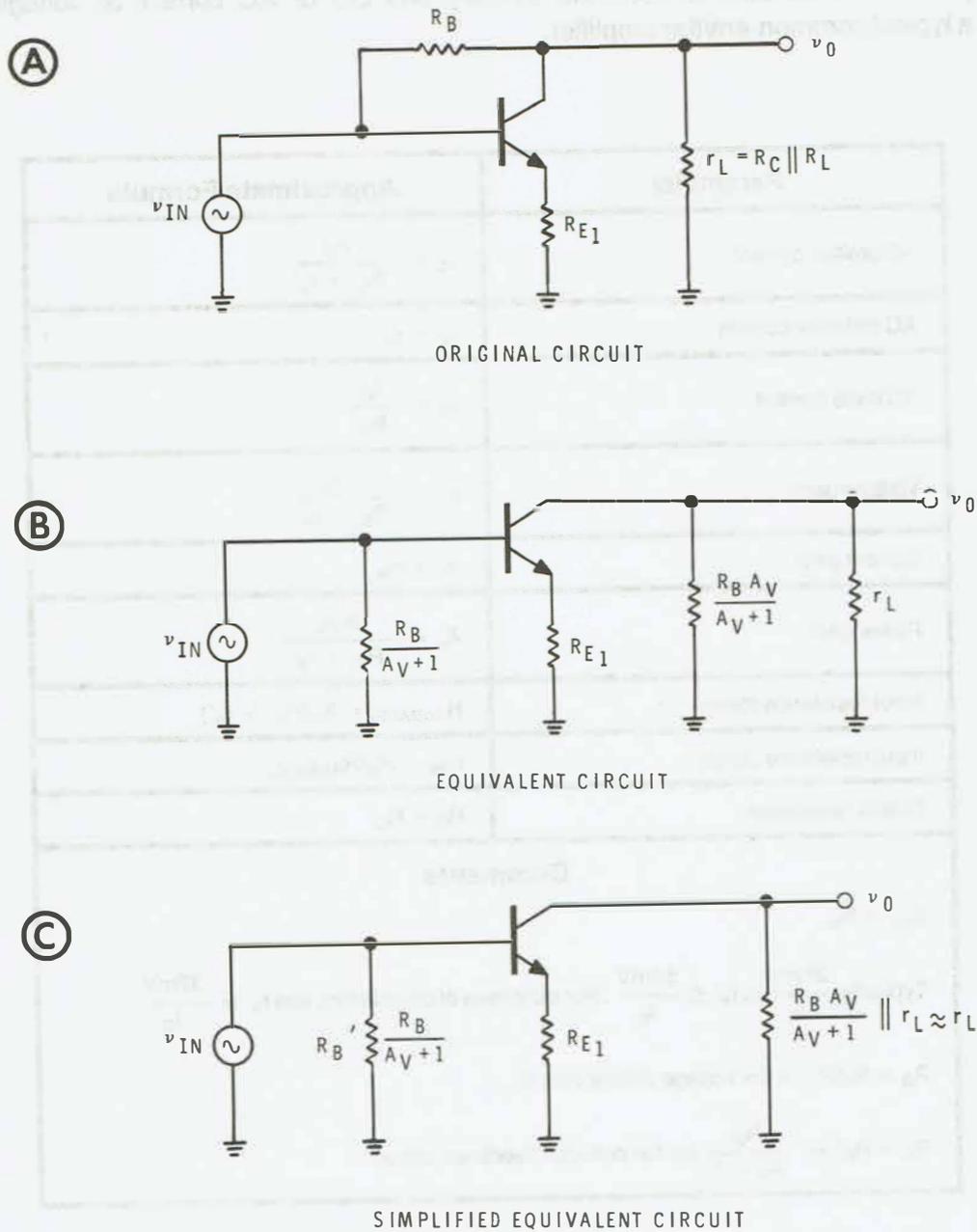


Figure 3-18

Applying Miller's theorem to a collector and emitter feedback-type common emitter amplifier.

- A. Original circuit.
- B. Equivalent circuit.
- C. Simplified equivalent circuit.

By using Table 3-1 in conjunction with the biasing summary guides in Unit 2, you should be able to calculate virtually any DC or AC current or voltage in a typical common-emitter amplifier.

Parameter	Approximate Formula
AC emitter current	$i_C = \frac{v_{IN}}{R_{E_1} + r_{e'}}$
AC collector current	$i_C = i_e$
AC base current	$i_C = \frac{i_C}{h_{fe}}$
Voltage gain	$A_V = \frac{-r_L}{R_{E_1} + r_{e'}}$
Current gain	$A_i = h_{fe}$
Power gain	$A_p = \frac{h_{fe} r_L}{R_{E_1} + r_{e'}}$
Input resistance (base)	$R_{IN(BASE)} = h_{fe}(R_{E_1} + r_{e'})$
Input resistance (total)	$R_{IN} = R_B R_{IN(BASE)}$
Output resistance	$R_O \approx R_C$
Comments	
$B_{AC} = h_{fe}$ Typically $\frac{26mV}{I_E} \leq r_{e'} \leq \frac{52mV}{I_E}$. For purposes of calculation, use $r_{e'} = \frac{37mV}{I_E}$ $R_B = R_1 R_2$ for the voltage divider circuit. $R_B = R_B' = \frac{R_B}{A_V + 1}$ for the collector feedback circuit.	

TABLE 3-1

Common-Emitter AC Formula Summary Guide

Example 3-11

Calculate the voltage gain and input resistance for the circuit shown in Figure 3-19. Assume that $h_{FE} \approx h_{fe} = 150$.

First calculate the DC emitter current, I_E .

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta}} = \frac{10V - 0.7V}{5k\Omega + \frac{645k\Omega}{150}} = 1mA \approx I_E$$

Now:

$$r_e' = \frac{37mV}{I_E} = \frac{37mV}{1mA} = 37\Omega$$

$$r_L = R_C || R_L = 5k\Omega || 20k\Omega = 4k\Omega$$

Since $R_{E_i} = 0$:

$$A_V = \frac{-r_L}{r_e'} = \frac{-4k\Omega}{37\Omega} = -108.1$$

$$R_{IN(BASE)} = h_{ie}(R_{E_i} + r_e') = 150(0 + 37\Omega) = 5.55k\Omega$$

From Miller's Theorem:

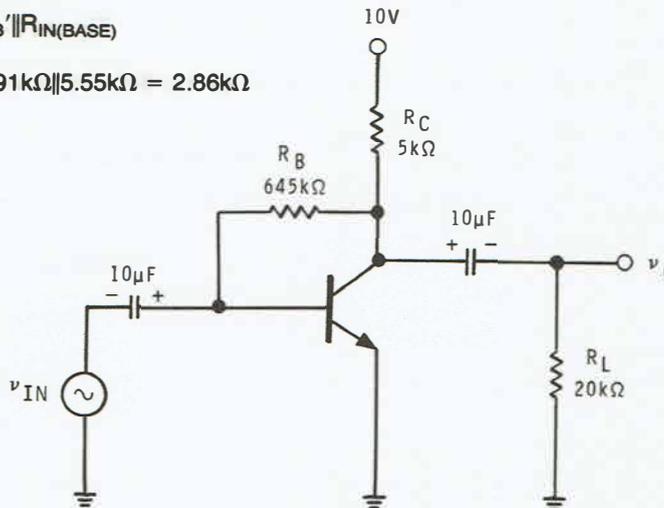
$$R_{B'} = \frac{R_B}{A_V + 1} = \frac{645k\Omega}{109.1} = 5.91k\Omega$$

Therefore:

$$R_{IN} = R_{B'} || R_{IN(BASE)}$$

$$R_{IN} = 5.91k\Omega || 5.55k\Omega = 2.86k\Omega$$

Figure 3-19
Circuit for Example 3-11.



Self-Test Review

Refer to Figure 3-20 for questions 11 through 15.

11. The circuit's voltage gain equals _____.
12. The input resistance looking into the base is _____ $k\Omega$.
13. The input resistance of the circuit is _____ $k\Omega$.
14. The circuit's output resistance equals _____ $k\Omega$.
15. The peak output voltage equals _____ V.

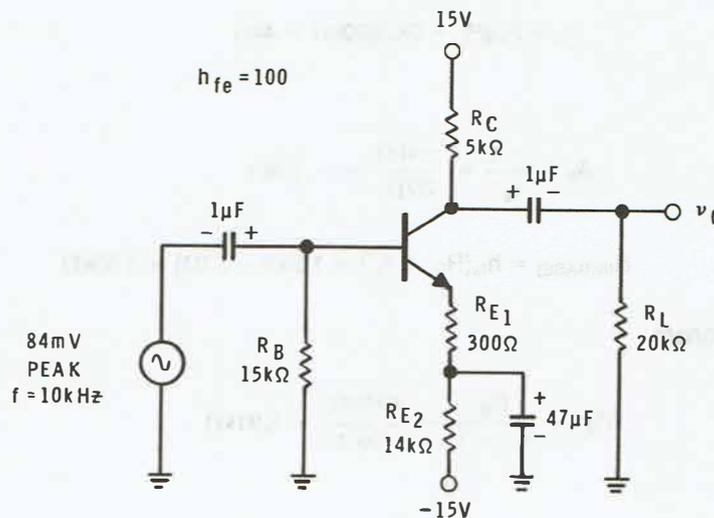


Figure 3-20

Circuit for Self-Test Review questions 11-15.

Refer to Figure 3-21 for questions 16 through 20.

16. The circuit's voltage gain equals _____.
17. The input resistance of the circuit is _____ $k\Omega$.
18. If the $100\mu\text{F}$ capacitor is open, the voltage gain will be _____.
19. To obtain a peak output voltage of 1V , v_{IN} must equal _____ mV peak.
20. The circuit's output resistance equals _____ $k\Omega$.

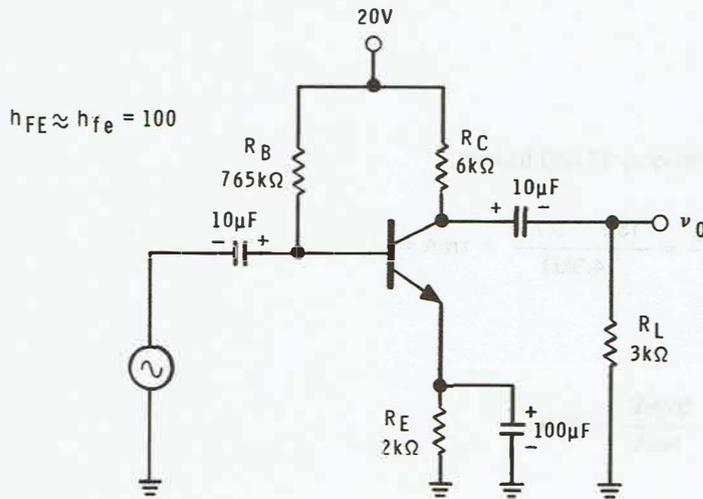


Figure 3-21

Circuit for Self-Test Review questions 16-20.

Answers

- | | |
|---------------------|--------------------|
| 11. -11.9 | 16. -108 |
| 12. 33.7k Ω | 17. 1.85k Ω |
| 13. 10.38k Ω | 18. -0.99 |
| 14. 5k Ω | 19. 9.26mV |
| 15. 1V | 20. 6k Ω |

The solutions to questions 11-20 follow:

$$11. \quad I_C = \frac{V_{EE} - V_{BE}}{R_E} = \frac{15V - 0.7V}{14.3k\Omega} = 1mA \approx I_E$$

Therefore:

$$r_{e'} = \frac{37mV}{I_E} = \frac{37mV}{1mA} = 37\Omega$$

And:

$$r_L = R_C \parallel R_L = 5k\Omega \parallel 20k\Omega = 4k\Omega$$

Since $R_{E_1} = 300\Omega$ we have:

$$A_v = \frac{-r_L}{R_{E_1} + r_{e'}} = \frac{-4k\Omega}{300\Omega + 37\Omega} = -11.9$$

$$12. \quad R_{IN(BASE)} = h_{fe}(R_{E_1} + r_{e'})$$

$$R_{IN(BASE)} = 100(300\Omega + 37\Omega) = 33.7k\Omega$$

$$13. \quad R_{IN} = R_B \parallel R_{IN(BASE)} = 15k\Omega \parallel 33.7k\Omega = 10.38k\Omega$$

$$14. \quad R_O \approx R_C = 5k\Omega$$

15. Since $v_{IN} = 84\text{mV}$ and $A_V = -11.9$, the peak output voltage, v_O is:

$$v_O = A_V v_{IN} = 11.9(84\text{mV}) = 999.6\text{mV} \approx 1\text{V peak}$$

16. For the emitter feedback circuit:

$$I_C = \frac{V_{CC} - V_{BE}}{R_E + \frac{R_B}{\beta}} = \frac{20\text{V} - 0.7\text{V}}{2\text{k}\Omega + \frac{765\text{k}\Omega}{100}} = \frac{19.3\text{V}}{9.65\text{k}\Omega}$$

$$I_C = 2\text{mA} \approx I_E$$

Thus:

$$r_e' = \frac{37\text{mV}}{I_E} = \frac{37\text{mV}}{2\text{mA}} = 18.5\Omega$$

Therefore:

$$A_V = \frac{-r_L}{R_{E_1} + r_e'} = \frac{6\text{k}\Omega \parallel 3\text{k}\Omega}{0 + 18.5\Omega} = \frac{-2\text{k}\Omega}{18.5\Omega} = -108$$

17. $R_B = 765\text{k}\Omega$ and $R_{IN(\text{BASE})} = h_{fe}(r_e')$ because $R_{E_1} = 0$. Therefore:

$$R_{IN} = R_B \parallel R_{IN(\text{BASE})}$$

$$R_{IN} = 765\text{k}\Omega \parallel 100(18.5\Omega)$$

$$R_{IN} = 765\text{k}\Omega \parallel 1.85\text{k}\Omega \approx 1.85\text{k}\Omega$$

18. Assuming the $100\mu\text{F}$ capacitor is open, $R_{E_1} = R_E = 2\text{k}\Omega$. Thus:

$$A_V = \frac{-r_L}{R_{E_1} + r_e'} = \frac{2\text{k}\Omega}{2\text{k}\Omega + 18.5\Omega} = -0.99$$

Incidentally, when you troubleshoot an amplifier whose gain is very low, one of the things to check for is an open emitter-bypass capacitor.

19. Since $A_V = -108$ and $v_O = 1\text{V peak}$

$$v_{IN} = \frac{v_O}{A_V} = \frac{1\text{V}}{108} = 9.26\text{mV peak}$$

20. $R_O \approx R_C = 6\text{k}\Omega$

AC LOAD LINES AND THE DESIGN OF COMMON EMITTER VOLTAGE AMPLIFIERS

At this point, you should be able to calculate AC emitter, collector and base current, voltage, current and power gains, and the input and output resistances of typical common-emitter voltage amplifiers.

In this section, you will learn how to estimate the maximum possible, undistorted, AC output voltage that can be obtained from a given amplifier. As you will see, the amplifier's AC load line is used for this purpose. In addition, several rules of thumb, and design examples will be provided that simplify the task of designing useful voltage amplifiers.

The AC Load Line

The DC load lines of the various common-emitter circuits are illustrated in Figure 3-22A. Recall that the intercepts indicate the maximum possible DC collector current, $I_{C(sat)}$, and DC collector-to-emitter voltage, $V_{CE(cut)}$.

In a common-emitter circuit, the slope of the DC load line depends upon the total resistance between the collector and emitter terminals in the **DC equivalent circuit**. For the circuits discussed so far, this total DC resistance equals $R_C + R_E$.

For this reason, the slope of the DC load lines in Figure 3-22A is $\frac{-1}{R_C + R_E}$.

From the introduction to AC load lines in Unit 1, recall that the AC load line crosses the DC load line at the Q point. The slope of the AC load line is determined by the total resistance between the collector and emitter terminals in the **AC equivalent circuit**. For the circuits discussed so far, this total AC resistance

equals $R_{E_1} + r_L$. Consequently, the slope of the AC load line is $\frac{-1}{R_{E_1} + r_L}$ as shown in Figure 3-22B.

To calculate the intercepts of the AC load line you need the AC load line equation. In geometry, the equation of a straight line in point slope form is given as:

$$y - y_1 = m(x - x_1)$$

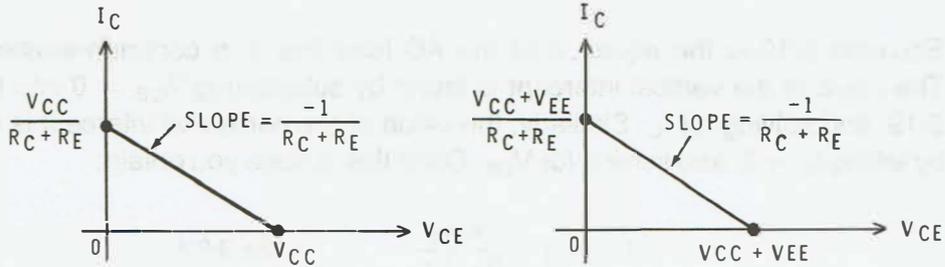
Where: m = slope of the line.

x and y are the variables.

x_1 and y_1 are the coordinates of a point on the line.

(A)

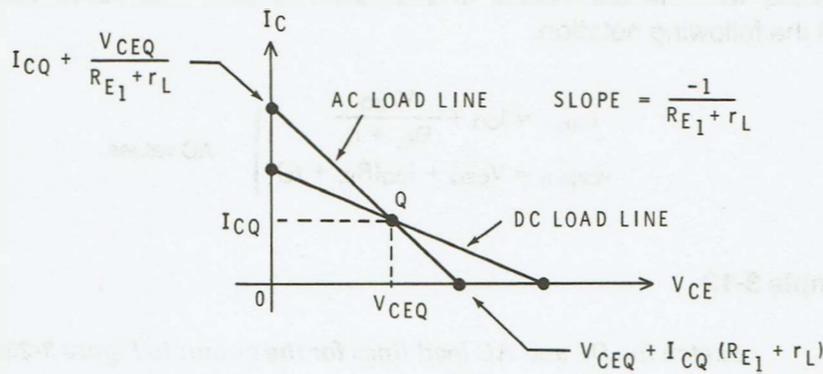
DC LOAD LINES



EMITTER FEEDBACK, COLLECTOR FEEDBACK, AND VOLTAGE DIVIDER CIRCUITS

EMITTER BIAS CIRCUIT

(B)



THE AC LOAD LINE

Figure 3-22

Common emitter DC and AC load lines.

- A. DC load lines.
- B. The AC load line.

Applying this formula to the AC load line in Figure 3-22B yields:

$$I_C - I_{CQ} = \frac{1}{R_{E_1} + r_L} (V_{CE} - V_{CEQ}) \quad (\text{Eq. 3-19})$$

Equation 3-19 is the equation of the AC load line in a common-emitter circuit. The value of the vertical intercept is found by substituting $V_{CE} = 0$ into Equation 3-19, and solving for I_C . Similarly, the value of the horizontal intercept is obtained by letting $I_C = 0$, and solving for V_{CE} . Once this is done you obtain:

$$I_C = I_{CQ} + \frac{V_{CEQ}}{R_{E_1} + r_L} \quad (\text{Eq. 3-20})$$

$$V_{CE} = V_{CEQ} + I_{CQ}(R_{E_1} + r_L) \quad (\text{Eq. 3-21})$$

Equation 3-20 indicates that the value of the **AC saturation current**, and Equation 3-21 indicates the value of the **AC cutoff voltage**. To avoid confusing these quantities with the DC values of saturation current and cutoff voltage, we will adopt the following notation.

$$\left. \begin{aligned} i_{C(\text{sat})} &= I_{CQ} + \frac{V_{CEQ}}{R_{E_1} + r_L} \\ v_{CE(\text{cut})} &= V_{CEQ} + I_{CQ}(R_{E_1} + r_L) \end{aligned} \right\} \text{AC values.}$$

Example 3-12

Sketch the DC and AC load lines for the circuit in Figure 3-23A. Assume $h_{FE} \approx h_{fe} = 100$.

The intercepts of the DC load line are:

$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C + R_E} = \frac{16\text{V}}{2.8\text{k}\Omega + 3.2\text{k}\Omega} = \frac{16\text{V}}{6\text{k}\Omega} = 2.67\text{mA}$$

$$V_{CE(\text{cut})} = V_{CC} = 16\text{V}$$

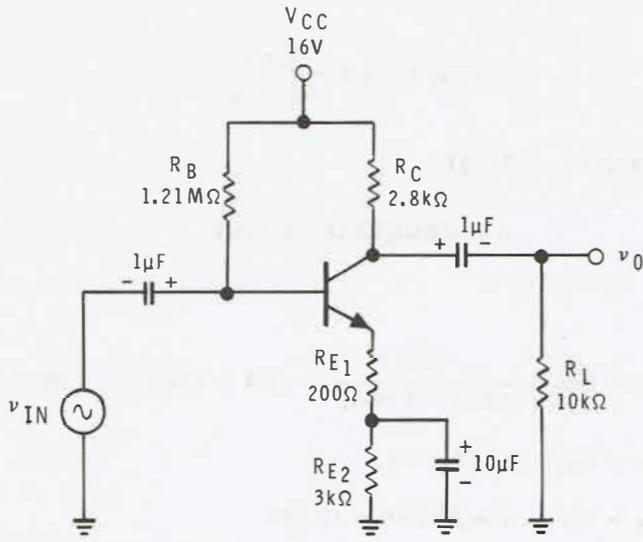
Before you can calculate the intercepts of the AC load line, you must calculate I_{CQ} and V_{CEQ} . Thus:

$$I_C = \frac{V_{CC} - V_{BE}}{R_E + \frac{R_B}{B}} = \frac{16\text{V} - 0.7\text{V}}{3.2\text{k}\Omega + \frac{1.21\text{M}}{100}} = \frac{15.3\text{V}}{15.3\text{k}\Omega} = 1\text{mA} = I_{CQ}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

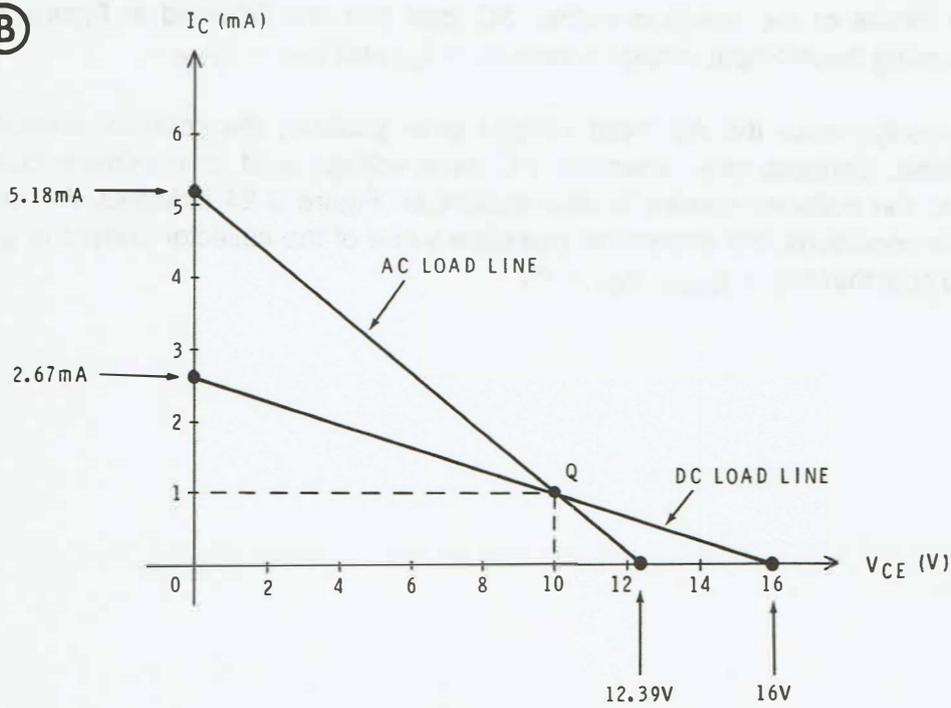
$$V_{CE} = 16\text{V} - 1\text{mA}(2.8\text{k}\Omega + 3.2\text{k}\Omega) = 10\text{V} = V_{CEQ}$$

(A)



CIRCUIT

(B)



LOAD LINES

Figure 3-23

Circuit and load lines for Example 3-12.

- A. Circuit.
- B. Load lines.

Now:

$$i_{C(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{R_{E1} + r_L}$$

Since $R_C = 2.8\text{k}\Omega$ and $R_L = 10\text{k}\Omega$:

$$r_L = 2.8\text{k}\Omega \parallel 10\text{k}\Omega = 2.19\text{k}\Omega$$

Therefore:

$$i_{C(\text{sat})} = 1\text{mA} + \frac{10\text{V}}{200\Omega + 2.19\text{k}\Omega} = 1\text{mA} + 4.18\text{mA} = 5.18\text{mA}$$

$$v_{CE(\text{cut})} = V_{CEQ} + I_{CQ}(R_{E1} + r_L)$$

$$v_{CE(\text{cut})} = 10\text{V} + 1\text{mA}(2.39\text{k}\Omega) = 12.39\text{V}$$

The load lines are sketched in Figure 3-23B.

Clipping Levels

The details of the common-emitter AC load line are provided in Figure 3-24. Assuming the AC input voltage is zero, $I_C = I_{CQ}$ and $V_{CE} = V_{CEQ}$.

Obviously, when the AC input voltage goes positive, the collector current increases. Consequently, when the AC input voltage is at its maximum positive peak, the collector current is also maximum. Figure 3-24 indicates that under these conditions, the **maximum possible** value of the collector current is $i_{C(\text{sat})}$. Also note that if $I_C = i_{C(\text{sat})}$, $V_{CE} = 0\text{V}$.

Similarly, when the AC input voltage is at its maximum negative peak, the collector current is minimum. In this case, Figure 3-24 indicates that the **maximum possible** value of the collector-to-emitter voltage is $V_{CE(cut)}$. Note that if $V_{CE} = v_{CE(cut)}$, $I_C = 0A$. Based on these observations, you can draw the following conclusions:

1. The maximum possible positive swing in the AC output voltage equals $I_{CQ}(R_{E1} + r_L)$.
2. The maximum possible negative swing in the output voltage equals V_{CEQ} .
3. The maximum useful, undistorted, peak output voltage equals V_{CEQ} or $I_{CQ}(R_{E1} + r_L)$, whichever is smaller.

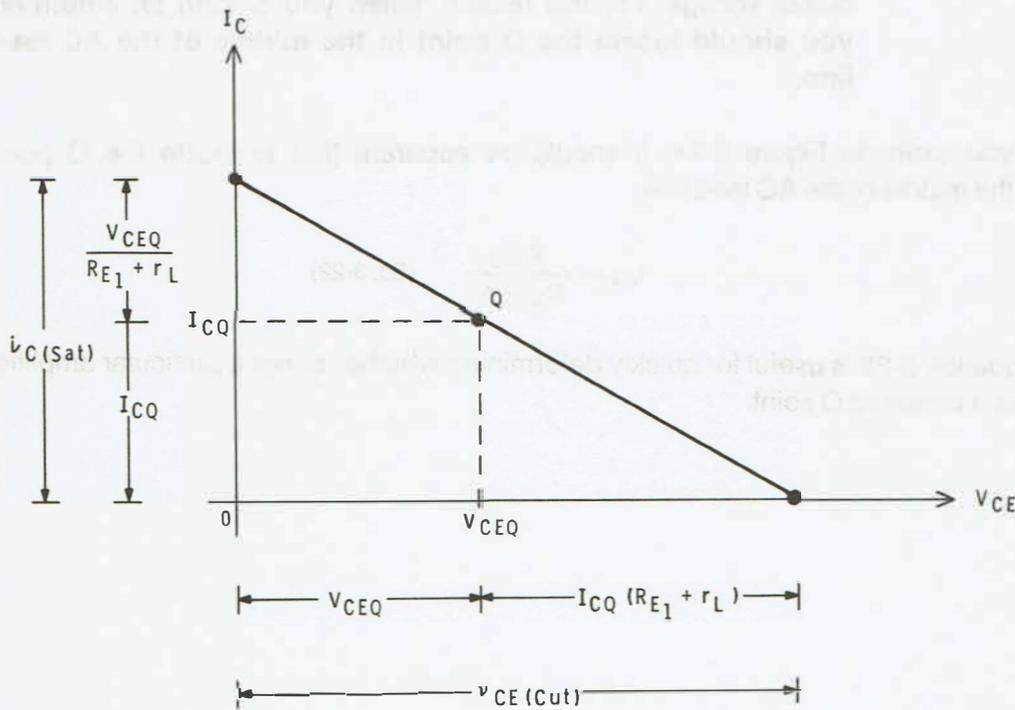


Figure 3-24

Details of the common emitter AC load line.

These concepts are summarized graphically in Figure 3-25 as follows:

1. In Figure 3-25A, the Q point is located near the upper end of the AC load line. When the input voltage goes positive I_C increases. However, since I_C cannot exceed $i_{C(sat)}$, a sufficiently large input signal causes the positive peak of the collector current to clip at $i_{C(sat)}$. Consequently, the output voltage is clipped on the negative half cycle as indicated in Figure 3-25A.
2. Figure 3-25B illustrates what happens if the Q point is located near the lower end of the AC load line. In this case, the positive peak of the output voltage is clipped.
3. In Figure 3-25C, the Q point is located in the middle of the AC load line. In this case, you obtain the maximum possible unclipped output voltage. For this reason, **when you design an amplifier, you should locate the Q point in the middle of the AC load line.**

If you examine Figure 3-24, it should be apparent that to locate the Q point in the middle of the AC load line:

$$I_{CQ} = \frac{V_{CEQ}}{R_{E1} + r_L} \quad (\text{Eq. 3-22})$$

Equation 3-22 is useful for quickly determining whether or not a particular amplifier has a centered Q point.

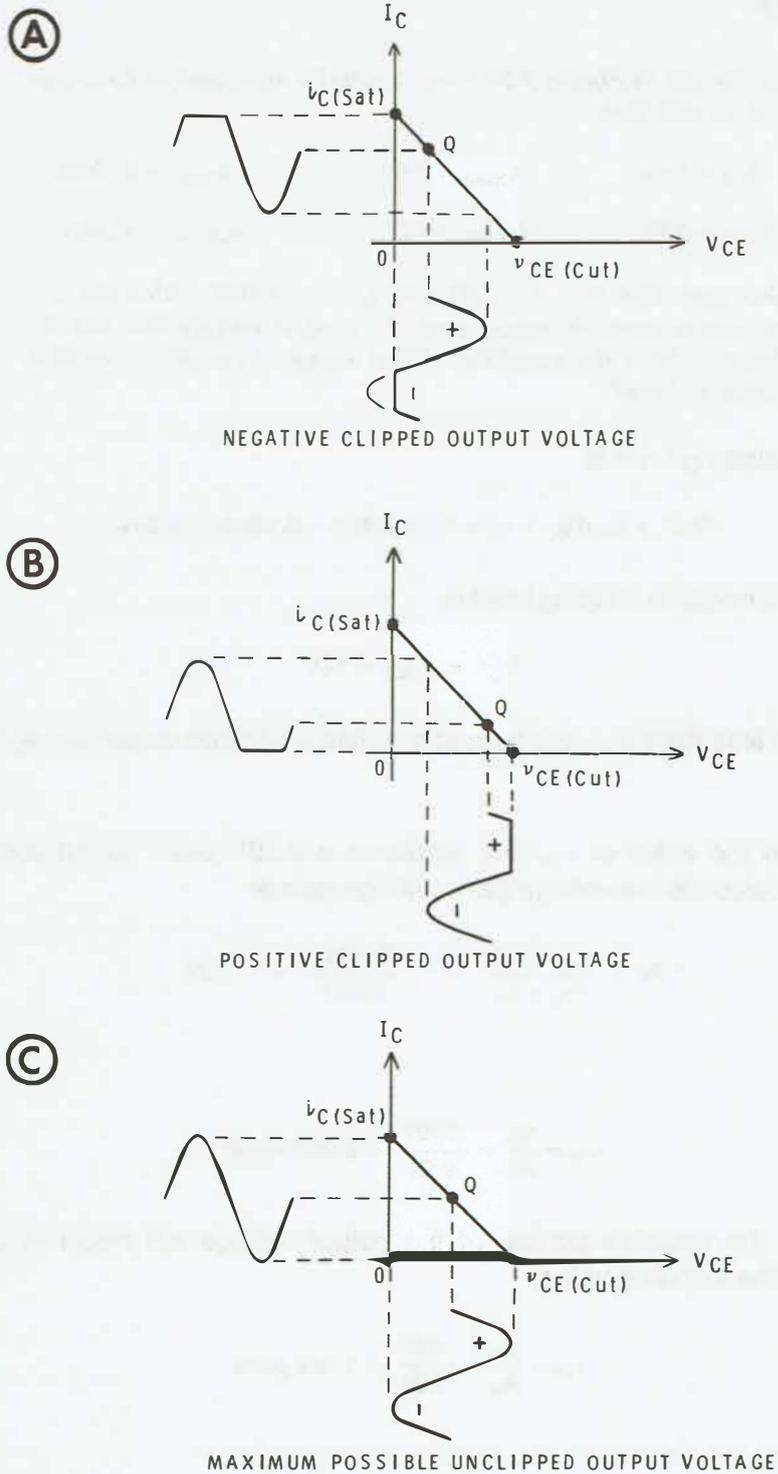


Figure 3-25

- Using the AC load line to predict clipping levels.
- Negative clipped output voltage.
 - Positive clipped output voltage.
 - Maximum possible unclipped output voltage.

Example 3-13

The circuit in Figure 3-23A was partially analyzed in Example 3-12. Recall that:

$$\begin{array}{lll} I_{CQ} = 1\text{mA} & I_{C(\text{sat})} = 2.67\text{mA} & i_{C(\text{sat})} = 5.18\text{mA} \\ V_{CEQ} = 10\text{V} & V_{CE(\text{cut})} = 16\text{V} & v_{CE(\text{cut})} = 12.39\text{V} \end{array}$$

Also note that $R_{E_1} = 200\Omega$ and $r_L = 2.19\text{k}\Omega$. Calculate the maximum possible, unclipped, AC output voltage that can be obtained from the amplifier. What value of v_{IN} produces this output voltage?

The positive clipping level is:

$$V_{O^+} = I_{CQ}(R_{E_1} + r_L) = 1\text{mA}(200\Omega + 2.19\text{k}\Omega) = 2.39\text{V}$$

Moreover, the negative clipping level is:

$$V_{O^-} = V_{CEQ} = 10\text{V}$$

Since V_{O^+} is less than V_{O^-} the largest possible unclipped output voltage is 2.39V peak.

To determine the value of v_{IN} that produces a 2.39V peak output voltage, you need to first calculate the voltage gain. Voltage gain is:

$$A_V = \frac{-r_L}{R_{E_1} + r_{e'}} = - \frac{2.19\text{k}\Omega}{237\Omega} = -9.24$$

Therefore:

$$v_{IN} = \frac{V_O}{A_V} = \frac{2.39\text{V}}{9.24} = 0.259\text{V peak}$$

Incidentally, the negative portion of the output voltage will begin to clip when v_{IN} exceeds the following value:

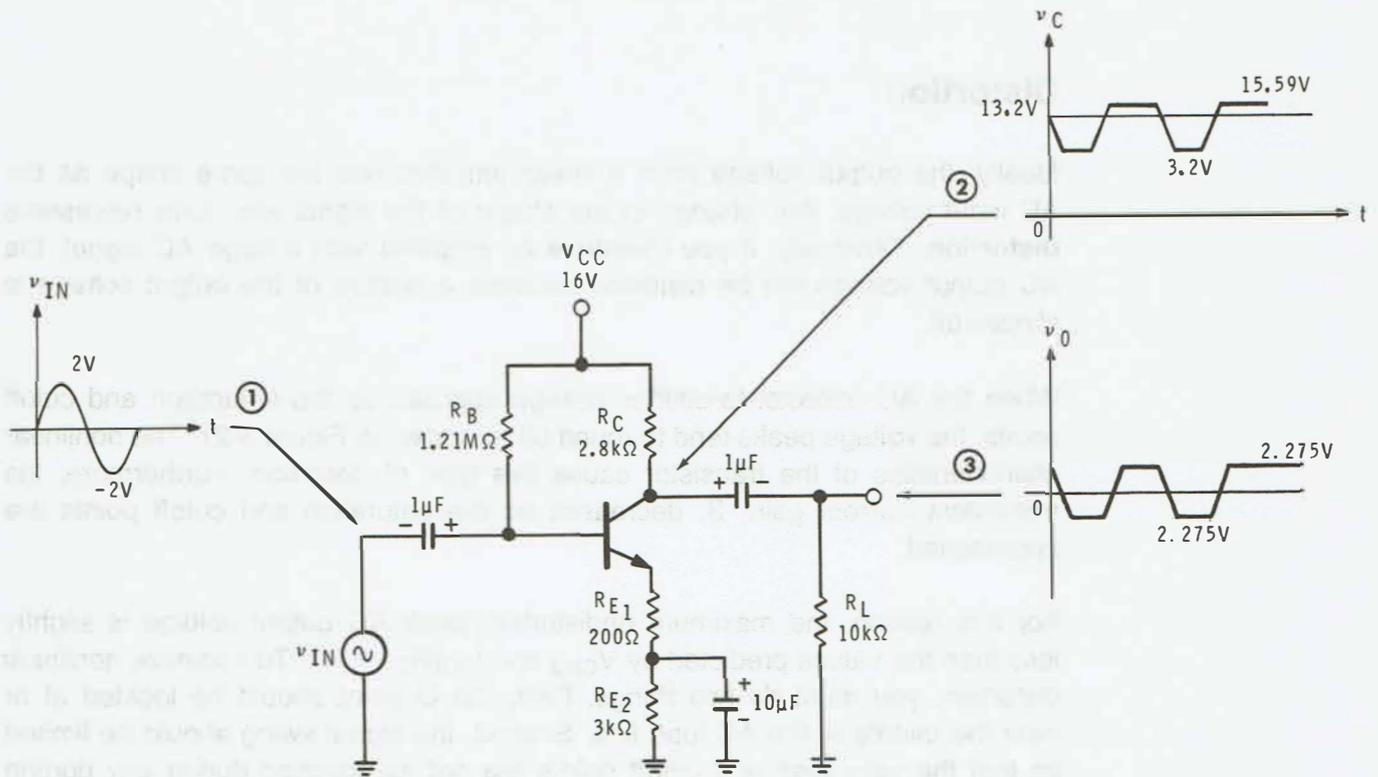
$$v_{IN} = \frac{V_O}{A_V} = \frac{10\text{V}}{9.24} = 1.08\text{V peak}$$

Example 3-14

Sketch the collector and output voltages for the amplifier in Figure 3-23A assuming v_{IN} is a 2V peak sine wave.

In this case, v_{IN} is large enough to produce clipping on both the positive and negative portions of the output voltage.

As discussed in Example 3-13, the positive and negative clipping levels are 2.39V and 10V respectively. Therefore, the output voltage appears as shown by waveform 3 in Figure 3-26.

**Figure 3-26**

Waveforms for Example 3-14.

The collector voltage is the algebraic sum of the AC output voltage, and the DC collector voltage. The DC collector voltage is calculated as follows:

$$V_C = V_{CC} - I_C R_C$$

$$V_C = 16V - 1mA(2.8k\Omega) = 13.2V$$

Since the AC output voltage has a positive peak of 2.39V, the collector voltage has a positive peak of $13.2V + 2.39V$ or 15.59V. Similarly, since the negative peak of the AC output voltage is 10V, the negative peak of the collector voltage is $13.2V - 10V$ or 3.2V.

Hence, the collector voltage appears as shown by waveform 2 in Figure 3-26.

Distortion

Ideally, the output voltage from a linear amplifier has the same shape as the AC input voltage. Any change in the shape of the signal waveform represents **distortion**. Obviously, if you overdrive an amplifier with a large AC signal, the AC output voltage will be distorted because a portion of the output voltage is clipped off.

When the AC collector-to-emitter voltage approaches the saturation and cutoff points, the voltage peaks tend to round off as shown in Figure 3-27. The nonlinear characteristics of the transistor cause this type of distortion. Furthermore, the transistors current gain, B , decreases as the saturation and cutoff points are approached.

For this reason, the maximum undistorted, peak AC output voltage is slightly less than the values predicted by V_{CEQ} and $I_{CQ}(R_{E_1} + r_L)$. To minimize nonlinear distortion, you must do two things. First, the Q point should be located at or near the middle of the AC load line. Second, the signal swing should be limited so that the saturation and cutoff points are not approached during any portion of the AC cycle.

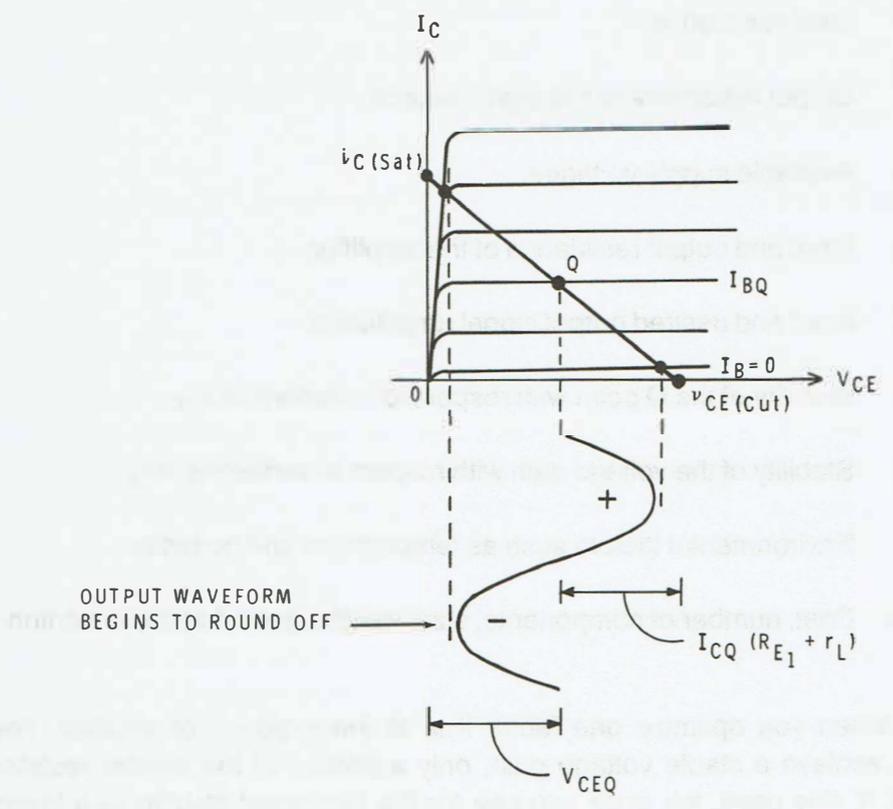


Figure 3-27

An example of nonlinear distortion.

Designing Common-Emitter Voltage Amplifiers

Some of the factors you should consider when you design an amplifier include:

1. Desired gain — voltage, current, and/or power.
2. Load resistance.
3. Output resistance of the signal source.
4. Available supply voltages.
5. Input and output resistance of the amplifier.
6. Input and desired output signal amplitudes.
7. Stability of the Q point with respect to variations in h_{FE} .
8. Stability of the voltage gain with respect to variations in r_e' .
9. Environmental factors such as temperature and humidity.
10. Cost, number of components, size, weight, and tolerable distortion.

Frequently, when you optimize one factor it is at the expense of another. For example, to achieve a stable voltage gain, only a portion of the emitter resistor is bypassed. In this case, the price you pay for the increased stability is a lower value of voltage gain.

The design of an amplifier requires numerous compromises or trade-off's before you can select the final component values. Let's examine some of the more obvious compromises you need to consider.

CHOICE OF BIASING SCHEME

The emitter feedback, collector feedback, and collector and emitter feedback circuits provide quasi-stable Q points, and require a minimum number of components. Therefore, you should consider these circuits for those applications that require few components or where the input signal is relatively small.

The voltage divider and emitter bias circuits provide very stable Q points, and require only a few additional components.

Generally speaking, these are the preferred biasing schemes for discrete linear applications. These circuits can accept somewhat larger input signals than the other biasing schemes because the Q point is not likely to shift towards the saturation and cutoff regions due to temperature or unit-to-unit variations.

FULLY OR PARTIALLY BYPASSED EMITTER RESISTOR

To achieve large gains, the emitter resistor must be fully bypassed. If stability is essential, only a portion of the emitter resistor should be bypassed. Applications that require large stable voltage gains may need several stages of amplification.

Applications that require a large input resistance for the amplifier should have a partially bypassed emitter resistor.

SUPPLY VOLTAGE(S)

The maximum peak AC output voltage is limited by V_{CEQ} and $I_{CQ}(R_{E_1} + r_L)$. In turn, these quantities are limited by the available supply voltage(s). In any event, the supply voltage(s) must be large enough to provide the desired signal swing. We will have more to say about this concept later.

CAPACITOR SELECTION

The coupling and bypass capacitors must be chosen so that they approximate short circuits at the **lowest** frequency to be amplified, f_1 . For this reason, the following inequalities need to be satisfied when selecting capacitors:

$$|X_{C_1}| \ll R_{IN} \text{ at } f_1$$

$$|X_{C_2}| \ll R_L \text{ at } f_1$$

$$|X_{C_3}| \ll R_{E_2} \text{ at } f_1$$

By defining “much less,” \ll , to be $1/20$, you can find the value required for C_1 as follows:

$$|X_{C_1}| = \frac{1}{2\pi f C_1} = \frac{0.159}{f_1 C_1} \leq \frac{R_{IN}}{20}$$

Solving for C_1 yields:

$$C_1 \geq \frac{3.18}{f_1 R_{IN}} \quad (\text{Eq. 3-23})$$

Similarly, for C_2 and C_3 :

$$C_2 \geq \frac{3.18}{f_1 R_L} \quad (\text{Eq. 3-24})$$

$$C_3 \geq \frac{3.18}{f_1 R_{E_2}} \quad (\text{Eq. 3-25})$$

In practice, standard value capacitors close to the calculated values would be selected for the design. Naturally, the voltage ratings for C_1 , C_2 , and C_3 should exceed the DC base, collector, and emitter voltages respectively.

Depending upon the given amplifier specifications, additional compromises may have to be considered.

Design Procedure

In designing a voltage amplifier, the basic problem is to select component values that provide the required voltage gain and also locate the Q point near the center of the AC load line.

Frequently, the value of a single component affects several parameters. For example, if the value of R_C changes, the voltage gain, DC collector-to-emitter voltage, clipping levels, and output resistance will also change. Consequently, in a well designed amplifier, the value chosen for R_C must simultaneously satisfy several parameters.

By rearranging the formulas derived previously, you can develop a systematic design procedure for single supply circuits. For example, to design a partially bypassed emitter feedback amplifier, you can proceed as follows:

1. **Select I_{CQ} .** The value chosen for I_{CQ} is somewhat arbitrary. For small signal amplifiers, 1 to 2mA is a popular choice.
2. **Calculate r_e' .** The value of r_e' is determined by your choice of I_{CQ} , since $r_e' = 37\text{mV}/I_{CQ}$.
3. **Select R_{E_1} .** The purpose of R_{E_1} is to stabilize the voltage gain by masking out variations in r_e' . If R_{E_1} is excessively large, the voltage gain will be very small. Thus, the value chosen for R_{E_1} represents a stability/gain trade-off. As a guide, R_{E_1} is usually 5 to 10 times larger than r_e' .
4. **Calculate r_L .** The magnitude of the voltage gain equals $\frac{r_L}{R_{E_1} + r_e'}$.
Since the values of R_{E_1} and r_e' were determined in steps 2 and 3, the value of r_L required to provide the desired gain is $A_V(R_{E_1} + r_e')$.
5. **Calculate V_{CEQ} .** Since $r_L = R_L \parallel R_C$, and the values of r_L and R_L are known, you can determine the value of R_C required to provide the desired gain.

6. **Calculate V_{CEQ} .** At this point, the values chosen for R_C and R_{E_1} satisfy the gain requirement. In order to provide a Q point near the middle of the AC load line V_{CEQ} must equal $I_{CQ}(R_{E_1} + r_L)$.

7. **Calculate V_{EQ} .** For the emitter feedback circuit:

$$V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CEQ}]$$

8. **Calculate R_E .** From Ohm's law:

$$R_E = V_{EQ}/I_{CQ}$$

9. **Calculate R_{E_2} :**

$$R_{E_2} = R_E - R_{E_1}$$

10. **Calculate R_B .** For the emitter feedback circuit:

$$R_B = \frac{V_{CC} - [V_{BE} + V_{EQ}]}{I_{BQ}}$$

11. **Calculate the minimum acceptable capacitor values.**

Similar procedures can be used to design the other single-supply common-emitter circuits.

Design Guide

The following design guide lists the steps and formulas for designing elementary common-emitter voltage amplifiers. To design circuits with fully bypassed emitter resistors, simply set $R_{E_1} = 0$ in the appropriate formulas.

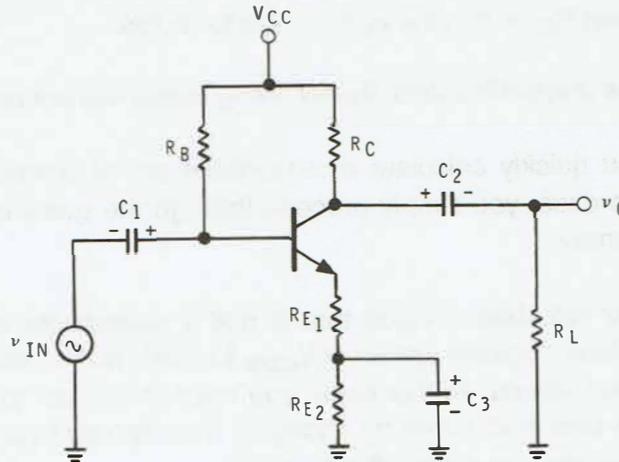
For a particular set of specifications, the following outcomes are possible:

1. You quickly calculate a reasonable set of component values. In this case, you simply proceed through the guide in a step-by-step manner.
2. You calculate a value that is **not** a reasonable value. Examples include negative values of V_{CEQ} , for NPN BJT's, and negative resistance values. In this case, you must "back up" to determine why this occurred. Often by changing a component value in a previous step, you can correct the problem.
3. Component values cannot be calculated that satisfy all the original specifications. Here, you should consider changing the original specifications. If this is not possible, then a simple single-stage amplifier cannot be used for the design.

By referring to the design guide and the material presented earlier, you should be able to design useful voltage amplifiers. The design of more complex amplifiers will be covered later.

COMMON-EMITTER VOLTAGE AMPLIFIER DESIGN GUIDE EMITTER FEEDBACK PARTIALLY BYPASSED

1

1. Select I_{CQ} 2. Calculate $r_{e'}$

$$r_{e'} = \frac{37\text{mV}}{I_{CQ}}$$

3. Select R_{E1}

$$R_{E1} = 5 \text{ to } 10 \text{ times } r_{e'}$$

4. Calculate r_L

$$r_L = A_v(r_{e'} + R_{E1})$$

5. Calculate R_C

$$R_C = \frac{R_L r_L}{R_L - r_L}$$

6. Calculate V_{CEQ}

$$V_{CEQ} = I_{CQ}(R_{E1} + r_L)$$

7. Calculate V_{EQ}

$$V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CEQ}]$$

8. Calculate R_E

$$R_E = \frac{V_{EQ}}{I_{CQ}}$$

9. Calculate R_{E2}

$$R_{E2} = R_E - R_{E1}$$

10. Calculate R_B

$$R_B = \frac{V_{CC} - [V_{BE} + V_{EQ}]}{I_{BQ}}$$

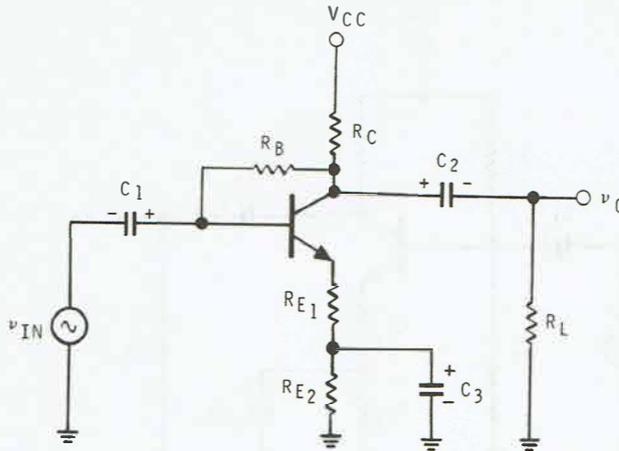
11. Select capacitors

$$C_1 \geq \frac{3.18}{f_1 R_{IN}}, \quad C_2 \geq \frac{3.18}{f_1 R_L}$$

$$C_3 \geq \frac{3.18}{f_1 R_{E2}}$$

COLLECTOR AND EMITTER FEEDBACK PARTIALLY BYPASSED

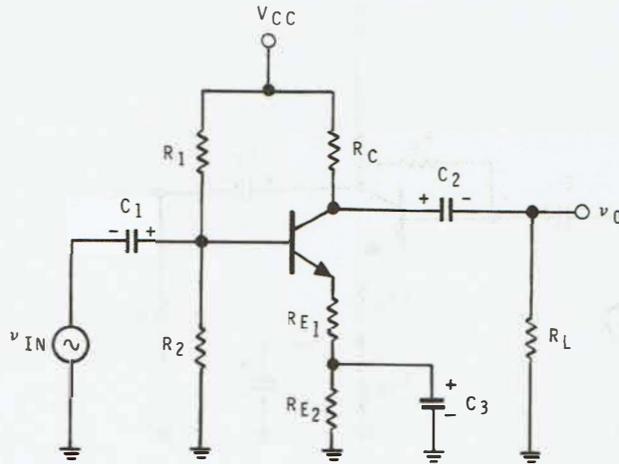
2



1. Select I_{CQ}
2. Calculate r_e' $r_e' = \frac{37\text{mV}}{I_{CQ}}$
3. Select R_{E1} $R_{E1} = 5 \text{ to } 10 \text{ times } r_e'$
4. Calculate r_L $r_L = A_V(r_e' + R_{E1})$
5. Calculate R_C $R_C = \frac{R_L r_L}{R_L - r_L}$
6. Calculate V_{CEQ} $V_{CEQ} = I_{CQ}(R_{E1} + r_L)$
7. Calculate V_{EQ} $V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CEQ}]$
8. Calculate R_E $R_E = \frac{V_{CEQ}}{I_{CQ}}$
9. Calculate R_{E2} $R_{E2} = R_E - R_{E1}$
10. Calculate R_B $R_B = \frac{V_{CEQ} - V_{BE}}{I_{BQ}}$
11. Select capacitors $C_1 \geq \frac{3.18}{f_1 R_{IN}}, C_2 \geq \frac{3.18}{f_1 R_L}$
 $C_3 \geq \frac{3.18}{f_1 R_{E2}}$

VOLTAGE DIVIDER PARTIALLY BYPASSED

3



1. Select I_{CQ}
2. Calculate r_e'
$$r_e' = \frac{37\text{mV}}{I_{CQ}}$$
3. Select R_{E1}
$$R_{E1} = 5 \text{ to } 10 \text{ times } r_e'$$
4. Calculate r_L
$$r_L = A_V(r_e' + R_{E1})$$
5. Calculate R_C
$$R_C = \frac{R_L r_L}{R_L - r_L}$$
6. Calculate V_{CEQ}
$$V_{CEQ} = I_{CQ}(R_{E1} + r_L)$$
7. Calculate V_{EQ}
$$V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CEQ}]$$
8. Calculate R_E
$$R_E = \frac{V_{EQ}}{I_{CQ}}$$
9. Calculate R_{E2}
$$R_{E2} = R_E - R_{E1}$$
10. Select R_2
$$R_2 \leq 10 R_E$$
11. Calculate R_1
$$R_1 = \frac{R_2(V_{CC} - V_{BQ})}{V_{BQ}}$$
12. Select capacitors
$$C_1 \geq \frac{3.18}{f_1 R_{IN}}, C_2 \geq \frac{3.18}{f_1 R_L}$$

$$C_3 \geq \frac{3.18}{f_1 R_{E2}}$$

Example 3-15

Design a small signal voltage amplifier that provides a typical voltage gain of 108. A general purpose BJT is available for the design whose $h_{FE} \approx h_{fe} = 100$. Before you design the circuits, assume that:

$$V_{CC} = 20V$$

$$R_L = 3k\Omega$$

$$f_1 = 100\text{Hz}$$

The large voltage gain requires a **fully bypassed** emitter resistor. In this case, an emitter feedback circuit is suitable for the design. Referring to circuit 1 in the design guide, proceed as follows:

1. Select $I_{CQ} = 2\text{mA}$
2. $r_e' = \frac{37\text{mV}}{I_{CQ}} = \frac{37\text{mV}}{2\text{mA}} = 18.5\Omega$
3. $R_{E_1} = 0$ since the emitter resistor is fully bypassed.
4. $r_L = A_v(R_{E_1} + r_e') = 108(0 + 18.5\Omega) = 2k\Omega$
5. $R_C = \frac{R_L r_L}{R_L - r_L} = \frac{3k\Omega(2k\Omega)}{3k\Omega - 2k\Omega} = 6k\Omega$
6. $V_{CEQ} = I_{CQ}(R_{E_1} + r_L) = 2\text{mA}(0 + 2k\Omega) = 4V$
7. $V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CEQ}]$
 $V_{EQ} = 20V - [2\text{mA}(6k\Omega) + 4V] = 4V$
8. $R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{4V}{2\text{mA}} = 2k\Omega$
9. $R_{E_2} = R_E = 2k\Omega$ ($R_{E_1} = 0$)
10. Since $I_{CQ} = 2\text{mA}$ and $h_{FE} = 100$, I_{BQ} equals $2\text{mA}/100$ or $20\mu\text{A}$.
Then:

$$R_B = \frac{V_{CC} - [V_{BE} + V_{EQ}]}{I_{BQ}} = \frac{20V - [0.7V + 4V]}{20\mu\text{A}} = 765k\Omega$$

11. To calculate C_1 you must first calculate R_{IN} .

$$R_{IN(BASE)} = h_{ie}(R_{E_1} + r_{e'}) = 100(0 + 18.5\Omega) = 1.85k\Omega$$

$$R_{IN} = R_B || R_{IN(BASE)} = 765k\Omega || 1.85k\Omega \approx 1.85k\Omega$$

Then:

$$C_1 \geq \frac{3.18}{f_1 R_{IN}} = \frac{3.18}{(100)(1.85k\Omega)} = 1.72 \times 10^{-5}F$$

$$C_1 \geq 17.2\mu F$$

For the other capacitors:

$$C_2 \geq \frac{3.18}{f_1 R_L} = \frac{3.18}{100(3k\Omega)} = 1.06 \times 10^{-5}F$$

$$C_2 \geq 10.6\mu F$$

$$C_3 \geq \frac{3.18}{f_1 R_{E_2}} = \frac{3.18}{100(2k\Omega)} = 1.59 \times 10^{-5}F$$

$$C_3 \geq 15.9\mu F$$

Example 3-16

Design a small signal voltage amplifier to provide a stable voltage gain of approximately 15. Assume:

$$V_{CC} = 15V$$

$$R_L = 6k\Omega$$

$$h_{FE} \approx h_{fe} = 100$$

$$f_1 = 500Hz$$

The stable gain and single supply suggest a voltage divider circuit with a partially bypassed emitter resistor. Referring to circuit 3 in the design guide:

1. Select $I_{CQ} = 1mA$.
2. $r_e' = \frac{37mV}{I_{CQ}} = \frac{37mV}{1mA} = 37\Omega$
3. Select $R_{E1} = 10r_e' = 370\Omega$
4. $r_L = A_V(R_{E1} + r_e') = 15(370\Omega + 37\Omega) = 6.1k\Omega$
5. $R_C = \frac{R_L r_L}{R_L - r_L} = \frac{6k\Omega(6.1k\Omega)}{6k\Omega - 6.1k\Omega} = -366k\Omega?$

Obviously, a negative value for R_C is not reasonable. To obtain a positive value of R_C , $R_L > r_L$. With $R_{E1} = 370\Omega$ and $r_e' = 37\Omega$, the value of r_L calculated in step 4 was $6.1k\Omega$. Since $R_L = 6k\Omega$, you must change something so that R_L will be larger than r_L .

What can you do? There are two options:

1. Increase I_{CQ} . This results in a smaller r_e' . Consequently, you can use a smaller value of R_{E1} to stabilize the gain. Since $r_L = A_V(R_{E1} + r_e')$, smaller values of R_{E1} and/or r_e' will decrease the value required for r_L .
2. Leave I_{CQ} at $1mA$ but decrease the value of R_{E1} . For example, try $R_{E1} = 5r_e'$ or 185Ω .

Let's examine each option in more detail.

For Option 1:

1. Select $I_{CQ} = 2\text{mA}$
2. $r_e' = \frac{37\text{mV}}{I_{CQ}} = \frac{37\text{mV}}{2\text{mA}} = 18.5\Omega$
3. Select $R_{E1} = 10r_e' = 10(18.5\Omega) = 185\Omega$
4. $r_L = A_V(R_{E1} + r_e') = 15(185\Omega + 18.5\Omega) = 3.05\text{k}\Omega$

Note that $R_L > r_L$ which corrected the initial problem.

5. $R_C = \frac{R_L r_L}{R_L - r_L} = \frac{6\text{k}\Omega(3.05\text{k}\Omega)}{6\text{k}\Omega - 3.05\text{k}\Omega} = 6.2\text{k}\Omega$
6. $V_{CEQ} = I_{CQ}(R_{E1} + r_L) = 2\text{mA}(185\Omega + 3.05\text{k}\Omega)$
 $V_{CEQ} = 6.47\text{V}$
7. $V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CEQ}]$
 $= 15\text{V} - [2\text{mA}(6.2\text{k}\Omega) + 6.47\text{V}]$
 $= 15\text{V} - 18.87\text{V}$
 $= -3.87\text{V}?$

Unfortunately, increasing I_{CQ} to 2mA solved one problem but created another. Clearly a negative value for V_{EQ} is not reasonable with an NPN BJT. To solve this problem, you could specify a larger supply voltage. For example if V_{CC} was increased to 25V, V_{EQ} would not be negative, and the design would proceed smoothly.

Since the original specifications called for $V_{CC} = 15\text{V}$, let's explore option 2 before changing specifications.

For Option 2:

1. Select $I_{CQ} = 1\text{mA}$
2. $r_e' = 37\Omega$
3. Select $R_{E1} = 5r_e' = 5(37\Omega) = 185\Omega$
4. $r_L = A_v(R_{E1} + r_e') = 15(185\Omega + 37\Omega) = 3.33\text{k}\Omega$
5. $R_C = \frac{R_L r_L}{R_L - r_L} = \frac{6\text{k}\Omega(3.33\text{k}\Omega)}{6\text{k}\Omega - 3.33\text{k}\Omega} = 7.48\text{k}\Omega$
6. $V_{CEQ} = I_{CQ}(R_{E1} + r_L) = 1\text{mA}(185\Omega + 3.33\text{k}\Omega)$
 $V_{CEQ} = 3.52\text{V}$
7. $V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CEQ}]$
 $V_{EQ} = 15\text{V} - [1\text{mA}(7.48\text{k}\Omega) + 3.52\text{V}]$
 $V_{EQ} = 15\text{V} - 11\text{V} = 4\text{V}$
8. $R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{4\text{V}}{1\text{mA}} = 4\text{k}\Omega$
9. $R_{E2} = R_E - R_{E1} = 4\text{k}\Omega - 185\Omega = 3.815\text{k}\Omega \approx 3.82\text{k}\Omega$
10. Select $R_2 = 3.9\text{k}\Omega$
11. $R_1 = \frac{R_2(V_{CC} - V_{BQ})}{V_{BQ}}$

Since $V_{EQ} = 4\text{V}$, $V_{BQ} = 0.7\text{V} + 4\text{V} = 4.7\text{V}$. Thus:

$$R_1 = \frac{3.9\text{k}\Omega(15\text{V} - 4.7\text{V})}{4.7\text{V}} = 8.55\text{k}\Omega$$

$$12. \quad R_{IN(BASE)} = h_{fe}(R_{E_1} + r_{e'})$$

$$R_{IN(BASE)} = 100(185\Omega + 37\Omega) = 22.2k\Omega$$

$$R_{IN} = R_1 \parallel R_2 \parallel R_{IN(BASE)}$$

$$R_{IN} = 8.55k\Omega \parallel 3.9k\Omega \parallel 22.2k\Omega$$

$$R_{IN} = 2.68k\Omega \parallel 22.2k\Omega = 2.4k\Omega$$

$$C_1 \geq \frac{3.18}{f_1 R_{IN}} = \frac{3.18}{500(2.4k\Omega)} = \frac{3.18}{1.2 \times 10^6 \Omega} = 2.65\mu F$$

$$C_2 \geq \frac{3.18}{f_1 R_L} = \frac{3.18}{500(6k\Omega)} = \frac{3.18}{3 \times 10^6 \Omega} = 1.06\mu F$$

$$C_3 \geq \frac{3.18}{f_1 R_{E_2}} = \frac{3.18}{500(3.82k\Omega)} = \frac{3.18}{1.91 \times 10^6 \Omega} = 1.66\mu F$$

The calculated capacitor values are minimum values.

Emitter Bias Designs

To design single-supply amplifiers, our method essentially consisted of the following steps:

1. R_C was chosen to provide the desired value of voltage gain.
2. The value of V_{CEQ} required to center the Q point was calculated.
3. R_E was then chosen to establish the value for V_{CEQ} calculated in step 2.

In this way, **both** the gain and Q point requirements were satisfied. Symbolically, you can summarize the design steps as follows:

$$V_{CEQ} = V_{CQ} - V_{EQ}$$

And:

$$V_{CQ} = V_{CC} - I_{CQ}R_C \quad V_{EQ} = I_{CQ}R_E$$

Therefore:

$$V_{CEQ} = (V_{CC} - I_{CQ}R_C) - I_{CQ}R_E$$

Value of R_C sets gain and V_{CQ} value.

Chosen so that V_{CEQ} equals the value required for a centered Q point.

Let's consider what happens if you apply these steps to an emitter bias circuit.

$$V_{CEQ} = V_{CQ} - V_{EQ}$$

And:

$$V_{CQ} = V_{CC} - I_{CQ}R_C \quad V_{EQ} = I_{CQ}R_E - V_{EE} \approx -0.7V$$

Therefore:

$$V_{CEQ} = (V_{CC} - I_{CQ}R_C) - (-0.7V)$$

As before, the value of R_C establishes the gain and V_{CQ} value. Note however that the value of R_E has very little effect on the value of V_{CEQ} since, in an emitter bias circuit, $V_{EQ} \approx -0.7V$.

The value selected for R_C , to obtain the desired voltage gain, essentially fixes the value of V_{CQ} . **It is unlikely that this value of V_{CQ} will also provide a centered Q point.**

If a specific gain and centered Q point are both desired, you can do the following:

1. Select "reasonable values" for the supply voltages.
2. Design the circuit to obtain the desired voltage gain.
3. Draw the circuit's AC load line. From the load line, determine the values of I_{CQ} and V_{CQ} necessary to center the Q point.
4. Calculate the values of V_{CC} and V_{EE} that provide the desired Q point.

The following examples illustrate this process.

Example 3-17

Design a $\times 10$ emitter bias voltage amplifier to drive a $10\text{k}\Omega$ load. Predict the clipping levels of the amplifier, and sketch its AC load line.

Our initial choice for supply voltages is $\pm 15\text{V}$. To select component values for a voltage gain of 10, you can proceed as follows:

1. Select $I_{CQ} = 1\text{mA}$
2. $r_e' = \frac{37\text{mV}}{I_{CQ}} = \frac{37\text{mV}}{1\text{mA}} = 37\Omega$
3. $R_{E_1} = 10r_e' = 10(37\Omega) = 370\Omega$
4. $r_L = A_v R_{E_1} + r_e'$
 $r_L = 10(370\Omega + 37\Omega) = 4.07\text{k}\Omega$
5. $R_C = \frac{R_L r_L}{R_L - r_L} = \frac{10\text{k}\Omega(4.07\text{k}\Omega)}{10\text{k}\Omega - 4.07\text{k}\Omega} = 6.86\text{k}\Omega$
6. $R_E = \frac{V_{EE} - 0.7\text{V}}{I_{CQ}} = \frac{15\text{V} - 0.7\text{V}}{1\text{mA}} = 14.3\text{k}\Omega$
7. $R_{E_2} = R_E - R_{E_1} = 14.3\text{k}\Omega - 370\Omega = 13.93\text{k}\Omega$
8. $R_B \approx 10R_E$ Select $R_B = 150\text{k}\Omega$

Figure 3-28A illustrates the circuit. Naturally, capacitor values depend upon the lowest frequency, f_1 , to be amplified.

To sketch the AC load line, you need the Q point and intercept values. Thus:

$$\begin{aligned} I_{CQ} &= 1\text{mA} \\ V_{CQ} &= V_{CC} - I_{CQ}R_C = 15\text{V} - 1\text{mA}(6.86\text{k}\Omega) = 8.14\text{V} \\ V_{EQ} &\approx -0.7\text{V} \\ V_{CEQ} &= V_{CQ} - V_{EQ} = 8.14\text{V} - (-0.7\text{V}) = 8.84\text{V} \end{aligned}$$

$$i_{C(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{R_{E1} + r_L}$$

$$i_{C(\text{sat})} = 1\text{mA} + \frac{8.84\text{V}}{370\Omega + 4.07\text{k}\Omega} = 2.99\text{mA} \approx 3\text{mA}$$

$$V_{CE(\text{cut})} = V_{CEQ} + I_{CQ}(R_{E1} + r_L)$$

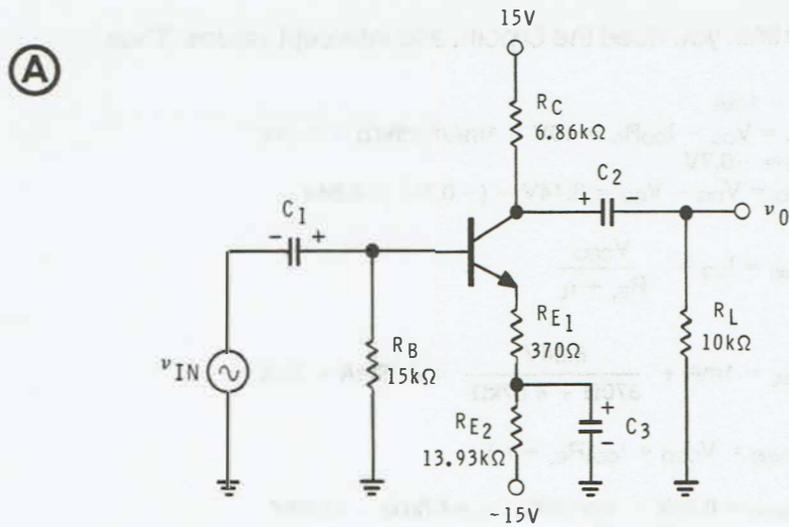
$$V_{CE(\text{cut})} = 8.84\text{V} + 1\text{mA}(370\Omega + 4.07\text{k}\Omega) = 13.28\text{V}$$

The circuit's AC load line is illustrated in Figure 3-28B. Here, note that:

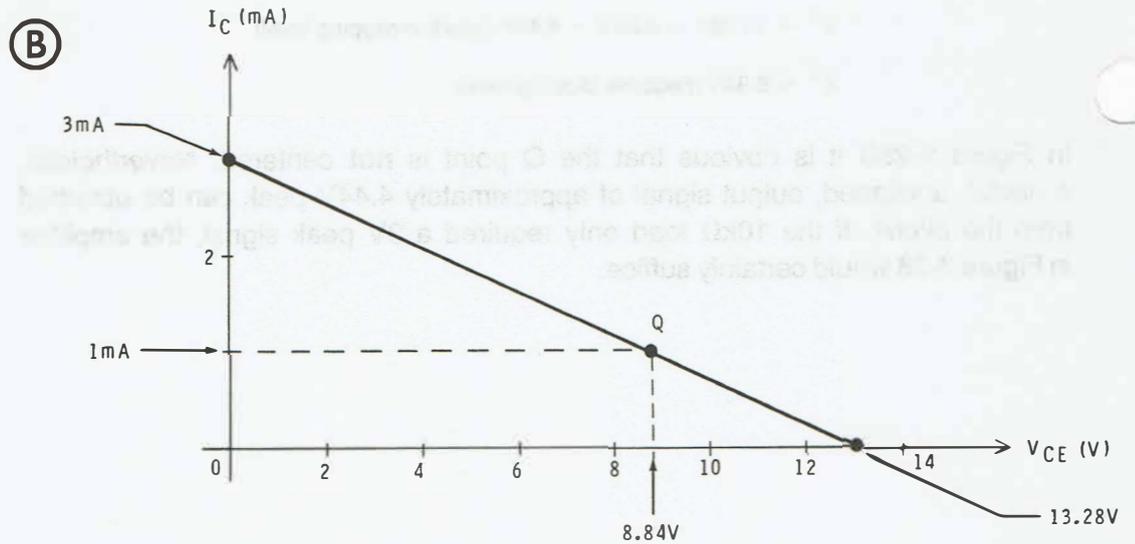
$$V^+ = 13.28\text{V} - 8.84\text{V} = 4.44\text{V} \text{ (positive clipping level)}$$

$$V^- = 8.84\text{V} \text{ (negative clipping level)}$$

In Figure 3-28B it is obvious that the Q point is **not** centered. Nevertheless, a useful, unclipped, output signal of approximately 4.44V peak can be obtained from the circuit. If the 10k Ω load only required a 3V peak signal, the amplifier in Figure 3-28 would certainly suffice.



AN EMITTER BIAS $\times 10$ VOLTAGE AMPLIFIER



AC LOAD LINE

Figure 3-28

Circuit and load line for Example 3-17.

- A. An emitter bias $\times 10$ voltage amplifier.
- B. AC load line.

Example 3-18

Calculate the values of V_{CC} and V_{EE} in Figure 3-28A to provide a centered Q point. Sketch the modified circuit, and its AC load line.

Our starting point is the AC load line in Figure 3-28B. Here, the values of I_{CQ} and V_{CEQ} corresponding to a centered Q point are:

$$I_{CQ} = \frac{i_{C(\text{sat})}}{2} = \frac{3\text{mA}}{2} = 1.5\text{mA}$$

$$V_{CEQ} = \frac{V_{CE(\text{cut})}}{2} = \frac{13.28\text{V}}{2} = 6.64\text{V}$$

In an emitter bias circuit:

$$V_{CC} = V_{R_C} + V_{CEQ} + V_{EQ}$$

$$V_{CC} = I_{CQ}R_C + V_{CEQ} - 0.7\text{V}$$

$$V_{EE} = I_{CQ}R_E + 0.7\text{V}$$

Therefore, the required supply voltages are:

$$V_{CC} = 1.5\text{mA}(6.86\text{k}\Omega) + 6.64\text{V} - 0.7\text{V} = 16.23\text{V}$$

$$V_{EE} = 1.5\text{mA}(14.3\text{k}\Omega) + 0.7\text{V} = 22.15\text{V}$$

Before we sketch the load line, let's verify the Q point and intercept values for the modified circuit in Figure 3-29A. Here:

$$I_{CQ} = \frac{V_{EE} - V_{BE}}{R_E} = \frac{22.15V - 0.7V}{14.3k\Omega} = 1.5mA$$

$$V_{CQ} = V_{CC} - I_{CQ}R_C$$

$$V_{CQ} = 16.23V - 1.5mA(6.86k\Omega) = 5.94V$$

$$V_{EQ} = -0.7V$$

$$V_{CEQ} = V_{CQ} - V_{EQ} = 5.94V - (-0.7V) = 6.64V$$

$$i_{C(sat)} = I_{CQ} + \frac{V_{CEQ}}{R_{E_1} + r_L}$$

$$i_{C(sat)} = 1.5mA + \frac{6.64V}{370\Omega + 4.07k\Omega} = 3mA$$

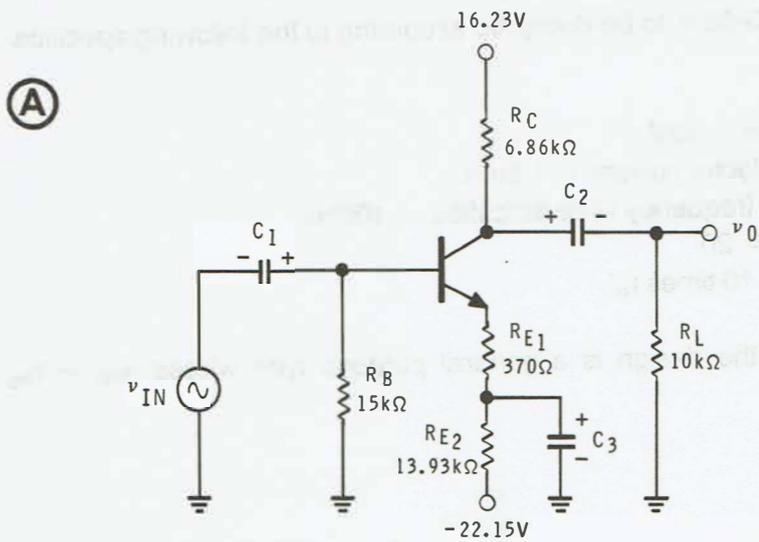
$$V_{CE(cut)} = V_{CEQ} + I_{CQ}(R_{E_1} + r_L)$$

$$V_{CE(cut)} = 6.64V + 1mA(370\Omega + 4.07k\Omega) = 13.28V$$

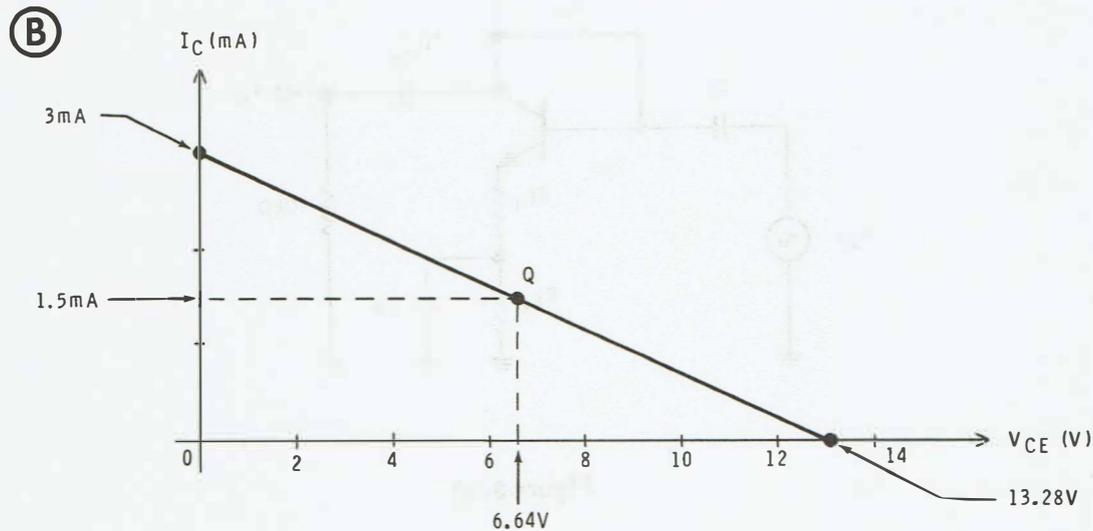
The load line is illustrated in Figure 3-29B. Here, note that the positive and negative clipping levels are:

$$V^+ = V^- = 6.64V$$

In this case, an unclipped, peak output voltage can be obtained that is approximately 2V larger than the amplifier in Figure 3-28A.



x 10 VOLTAGE AMPLIFIER WITH CENTERED Q POINT



AC LOAD LINE

Figure 3-29

Circuit and load line for Example 3-18.

- A. x 10 voltage amplifier with centered Q point.
- B. AC load line.

Self-Test Review

The amplifier in Figure 3-30 is to be designed according to the following specifications:

Supply voltage = 30V.

Quiescent collector current = 1.5mA.

Lowest signal frequency to be amplified = 100Hz.

Voltage gain = 20.

R_{E1} should be 10 times r_e' .

The BJT available for the design is a general purpose type whose $h_{FE} \approx h_{fe} = 100$.

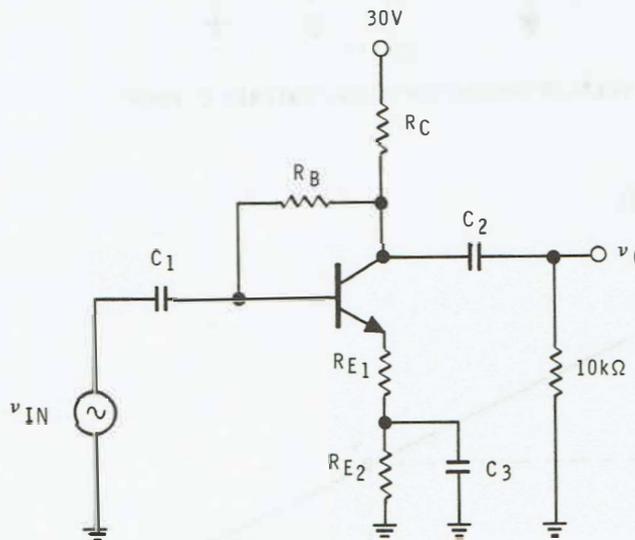


Figure 3-30

Circuit for Self-Test Review questions 21-30.

Based on the given information, and design methods provided in the unit, calculate the following:

21. The required value of $R_{E_1} = \underline{\hspace{2cm}} \Omega$.
22. The required value of $R_C = \underline{\hspace{2cm}} \text{k}\Omega$.
23. The required value of $R_{E_2} = \underline{\hspace{2cm}} \text{k}\Omega$.
24. The required value of $R_B = \underline{\hspace{2cm}} \text{M}\Omega$.
25. The required value of $C_1 = \underline{\hspace{2cm}} \mu\text{F}$.
26. The required value of $C_2 = \underline{\hspace{2cm}} \mu\text{F}$.
27. The required value of $C_3 = \underline{\hspace{2cm}} \mu\text{F}$.
28. The voltage ratings for C_1 , C_2 , and C_3 respectively should be larger than $\underline{\hspace{1cm}} \text{V}$, $\underline{\hspace{1cm}} \text{V}$, and $\underline{\hspace{1cm}} \text{V}$.
29. The maximum, unclipped, peak output voltage is approximately $\underline{\hspace{2cm}} \text{V}$.
30. The intercepts of the circuit's AC load line are $i_{C(\text{sat})} = \underline{\hspace{2cm}} \text{mA}$, and $v_{CE(\text{cut})} = \underline{\hspace{2cm}} \text{V}$.

Answers

- | | |
|---------------------|------------------------------|
| 21. 247 Ω | 26. 3.18 μ F |
| 22. 11.88k Ω | 27. 14.5 μ F |
| 23. 2.193k Ω | 28. 4.36V, 12.18V, and 3.29V |
| 24. 0.521M Ω | 29. 8.52V |
| 25. 2.45 μ F | 30. 3mA, 17.04V |

The solution to questions 21-30 follow:

$$21. \text{ Since } I_{CQ} = 1.5\text{mA}, r_e' = \frac{37\text{mV}}{1.5\text{mA}} = 24.7\Omega$$

$$R_{E_1} = 10r_e' = 10(24.7\Omega) = 247\Omega$$

22. First calculate the required value of r_L :

$$r_L = A_v(R_{E_1} + r_e')$$

$$r_L = 20(247\Omega + 24.7\Omega) = 5.43\text{k}\Omega$$

Since:

$$R_C = \frac{R_L r_L}{R_L - r_L}$$

We have:

$$R_C = \frac{10\text{k}\Omega(5.43\text{k}\Omega)}{10\text{k}\Omega - 5.43\text{k}\Omega} = 11.88\text{k}\Omega$$

23. Before R_{E_2} can be calculated, values for V_{CEQ} , V_{EQ} , and R_E are required. Thus:

$$V_{CEQ} = I_{CQ}(R_{E_1} + r_L)$$

$$V_{CEQ} = 1.5\text{mA}(247\Omega + 5.43\text{k}\Omega) = 8.52\text{V}$$

$$V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CEQ}]$$

$$V_{EQ} = 30\text{V} - [1.5\text{mA}(11.88\text{k}\Omega) + 8.52\text{V}]$$

$$V_{EQ} = 30\text{V} - 26.34\text{V} = 3.66\text{V}$$

$$R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{3.66\text{V}}{1.5\text{mA}} = 2.44\text{k}\Omega$$

Since $R_{E_2} = R_E - R_{E_1}$, we have:

$$R_{E_2} = 2.44\text{k}\Omega - 247\Omega = 2.193\text{k}\Omega$$

24. Since $I_{CQ} = 1.5\text{mA}$ and $h_{FE} = 100$, the value of I_{BQ} is $1.5\text{mA}/100$ or $15\mu\text{A}$. Thus:

$$R_B = \frac{V_{CEQ} - V_{BE}}{I_{BQ}} = \frac{8.52\text{V} - 0.7\text{V}}{15\mu\text{A}} = 0.521\text{M}\Omega$$

25. Before calculating the minimum acceptable value of C_1 , you must first calculate the amplifier's input resistance, R_{IN} .

$$R_{IN(\text{BASE})} = h_{FE}(R_{E_1} + r_e')$$

$$R_{IN(\text{BASE})} = 100[247\Omega + 24.7\Omega] = 27.17\text{k}\Omega$$

Since the circuit employs collector feedback the value of R_B' is, from Miller's theorem:

$$R_B' = \frac{R_B}{A_v + 1} = \frac{0.521\text{M}\Omega}{20 + 1} = 24.81\text{k}\Omega$$

Therefore, the effective input resistance is:

$$R_{IN} = R_B' \parallel R_{IN(\text{BASE})}$$

$$R_{IN} = 24.81\text{k}\Omega \parallel 27.17\text{k}\Omega = 12.97\text{k}\Omega$$

Finally, the minimum acceptable value of C_1 is:

$$C_1 = \frac{3.18}{f_1 R_{IN}} = \frac{3.18}{100\text{Hz}(12.97\text{k}\Omega)} = \frac{3.18}{12.97 \times 10^5}$$

$$C_1 = 0.245 \times 10^{-5}\text{F} = 2.45\mu\text{F}$$

26. The minimum acceptable value C_2 is:

$$C_2 = \frac{3.18}{f_1 R_L} = \frac{3.18}{100\text{Hz}(10\text{k}\Omega)} = \frac{3.18}{10 \times 10^5}$$

$$C_2 = 0.318 \times 10^{-5}\text{F} = 3.18\mu\text{F}$$

27. The minimum acceptable value of C_3 is:

$$C_3 = \frac{3.18}{f_1 R_{E_2}} = \frac{3.18}{100\text{Hz}(2.193\text{k}\Omega)} = \frac{3.18}{2.193 \times 10^5}$$

$$C_3 = 1.45 \times 10^{-5}\text{F} = 14.5\mu\text{F}$$

28. C_1 charges to the DC base voltage, V_{BQ} .
 C_2 charges to the DC collector voltage, V_{CQ} .
 C_3 charges to the DC voltage across, R_{E_2} .

Therefore:

$$V_{C_1} = V_{BQ} = 0.7\text{V} + V_{EQ} = 0.7\text{V} + 3.66\text{V} = 4.36\text{V}$$

$$V_{C_2} = V_{CQ} = V_{CC} - I_{CQ}R_C = 30\text{V} - 1.5\text{mA}(11.88\text{k}\Omega) = 12.18\text{V}$$

$$V_{C_3} = I_{CQ}R_{E_2} = 1.5\text{mA}(2.193\text{k}\Omega) = 3.29\text{V}$$

29. Since the circuit was designed for a centered Q point:

$$V^+ = V^- = V_{CEQ} = 8.52\text{V}$$

30. $i_{C(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{R_{E_1} + r_L}$

$$i_{C(\text{sat})} = 1.5\text{mA} + \frac{8.52\text{V}}{247\Omega + 5.43\text{k}\Omega} = 3\text{mA}$$

$$v_{CE(\text{cut})} = V_{CEQ} + I_{CQ}(R_{E_1} + r_L)$$

$$v_{CE(\text{cut})} = 8.52\text{V} + 1.5\text{mA}(247\Omega + 5.43\text{k}\Omega)$$

$$v_{CE(\text{cut})} = 17.04\text{V}$$

Note that since the Q point is centered:

$$i_{C(\text{sat})} = 2I_{CQ}$$

$$v_{CE(\text{cut})} = 2V_{CEQ}$$

SUMMARY

By adding coupling and bypass capacitors to the biasing circuits, you can construct useful voltage amplifiers. In these amplifiers, the DC currents and voltages can be calculated by using the formulas introduced in Unit 2. Similarly, by referring to Table 3-1, you can calculate the AC currents and voltages. Then you can obtain the actual, total responses by adding, algebraically, the DC and AC values.

Equivalent circuits help you visualize the operation of BJT circuits. To obtain the DC equivalent circuit, you must replace coupling and bypass capacitors by open circuits, and reduce the AC source to zero. To obtain the AC equivalent, you must replace coupling and bypass capacitors with short circuits, and reduce DC sources to zero.

The equivalent resistance between the collector and emitter terminals in the DC and AC equivalent circuits determines the slope of the DC and AC load lines. The point of intersection of the two lines determines the operating point, Q. Using this information, the intercept values of the AC load line were found to be:

$$i_{C(\text{sat})} = I_{CQ} = \frac{V_{CEQ}}{R_{E_1} + r_L}$$

$$v_{CE(\text{cut})} = V_{CEQ} + I_{CQ}(R_{E_1} + r_L)$$

The positive and negative clipping levels (V^+ and V^-) for a particular circuit, can be estimated from the AC load line. They are:

$$V^+ = I_{CQ}(R_{E_1} + r_L)$$

$$V^- = V_{CEQ}$$

When you design an amplifier, you should locate the Q point at or near the middle of the AC load line. The Design Guide in this unit gives a step-by-step procedure for doing this for single-supply circuits. Miller's theorem simplifies the design process for collector feedback amplifiers.

In an emitter bias circuit, the value of R_E has very little effect on the value of V_{CEQ} .

Therefore, to obtain a specific gain and a centered Q point, the design procedure must be modified as discussed in the text.

SUMMARY

By adding a load and a source resistor to the feedback circuit, you can control the output voltage regulation. In other words, the DC source and voltage divider can be controlled by using the same feedback circuit. Figure 3-1 shows the feedback circuit. You can calculate the AC output voltage by using the AC equivalent circuit. The AC equivalent circuit is shown in Figure 3-2. The AC equivalent circuit is shown in Figure 3-3. The AC equivalent circuit is shown in Figure 3-4. The AC equivalent circuit is shown in Figure 3-5.

The AC equivalent circuit is shown in Figure 3-6. The AC equivalent circuit is shown in Figure 3-7. The AC equivalent circuit is shown in Figure 3-8. The AC equivalent circuit is shown in Figure 3-9. The AC equivalent circuit is shown in Figure 3-10. The AC equivalent circuit is shown in Figure 3-11. The AC equivalent circuit is shown in Figure 3-12. The AC equivalent circuit is shown in Figure 3-13. The AC equivalent circuit is shown in Figure 3-14. The AC equivalent circuit is shown in Figure 3-15.

The AC equivalent circuit is shown in Figure 3-16. The AC equivalent circuit is shown in Figure 3-17. The AC equivalent circuit is shown in Figure 3-18. The AC equivalent circuit is shown in Figure 3-19. The AC equivalent circuit is shown in Figure 3-20. The AC equivalent circuit is shown in Figure 3-21. The AC equivalent circuit is shown in Figure 3-22. The AC equivalent circuit is shown in Figure 3-23. The AC equivalent circuit is shown in Figure 3-24. The AC equivalent circuit is shown in Figure 3-25.

$$V_{out} = \frac{V_{in} R_f}{R_f + R_{in}}$$

$$V_{out} = V_{in} \frac{R_f}{R_f + R_{in}}$$

The positive and negative feedback circuit is shown in Figure 3-26. The positive and negative feedback circuit is shown in Figure 3-27. The positive and negative feedback circuit is shown in Figure 3-28. The positive and negative feedback circuit is shown in Figure 3-29. The positive and negative feedback circuit is shown in Figure 3-30. The positive and negative feedback circuit is shown in Figure 3-31. The positive and negative feedback circuit is shown in Figure 3-32. The positive and negative feedback circuit is shown in Figure 3-33. The positive and negative feedback circuit is shown in Figure 3-34. The positive and negative feedback circuit is shown in Figure 3-35.

$$V_{out} = \frac{V_{in} R_f}{R_f + R_{in}}$$

When you design an amplifier, you should consider the AC equivalent circuit. The AC equivalent circuit is shown in Figure 3-36. The AC equivalent circuit is shown in Figure 3-37. The AC equivalent circuit is shown in Figure 3-38. The AC equivalent circuit is shown in Figure 3-39. The AC equivalent circuit is shown in Figure 3-40. The AC equivalent circuit is shown in Figure 3-41. The AC equivalent circuit is shown in Figure 3-42. The AC equivalent circuit is shown in Figure 3-43. The AC equivalent circuit is shown in Figure 3-44. The AC equivalent circuit is shown in Figure 3-45.

The AC equivalent circuit is shown in Figure 3-46. The AC equivalent circuit is shown in Figure 3-47. The AC equivalent circuit is shown in Figure 3-48. The AC equivalent circuit is shown in Figure 3-49. The AC equivalent circuit is shown in Figure 3-50. The AC equivalent circuit is shown in Figure 3-51. The AC equivalent circuit is shown in Figure 3-52. The AC equivalent circuit is shown in Figure 3-53. The AC equivalent circuit is shown in Figure 3-54. The AC equivalent circuit is shown in Figure 3-55.

The AC equivalent circuit is shown in Figure 3-56. The AC equivalent circuit is shown in Figure 3-57. The AC equivalent circuit is shown in Figure 3-58. The AC equivalent circuit is shown in Figure 3-59. The AC equivalent circuit is shown in Figure 3-60. The AC equivalent circuit is shown in Figure 3-61. The AC equivalent circuit is shown in Figure 3-62. The AC equivalent circuit is shown in Figure 3-63. The AC equivalent circuit is shown in Figure 3-64. The AC equivalent circuit is shown in Figure 3-65.

UNIT EXAMINATION

The following multiple choice examination is designed to test your understanding of the material presented in this unit. Place a check beside the multiple choice answer (A, B, C, or D) that you feel is most correct. When you have completed the examination, compare your answers with the correct ones that appear after the exam.

- An amplifier whose voltage gain is 50 has a db voltage gain of:
 - 50.
 - 1.7.
 - 67.8.
 - 33.9.
- An amplifier whose db voltage gain is 80 has a regular voltage gain of:
 - 80.
 - 1000.
 - 10000.
 - 100000.
- A common-emitter amplifier that uses collector feedback has $R_B = 520\text{k}\Omega$, $A_V = 25$, and $R_{IN(BASE)} = 10\text{k}\Omega$. The amplifier's input resistance, R_{IN} , is therefore:
 - r_e' .
 - $6.67\text{k}\Omega$.
 - $10\text{k}\Omega$.
 - $520\text{k}\Omega \parallel 10\text{k}\Omega$.

Refer to Figure 3-31 for questions 4 through 8.

- The voltage gain is approximately:
 - 18.3.
 - 25.
 - 216.
 - 400.
- Assuming $h_{fe} = 150$ the input resistance is:
 - $7.66\text{k}\Omega$.
 - $10\text{k}\Omega$.
 - $32.8\text{k}\Omega$.
 - r_e' .

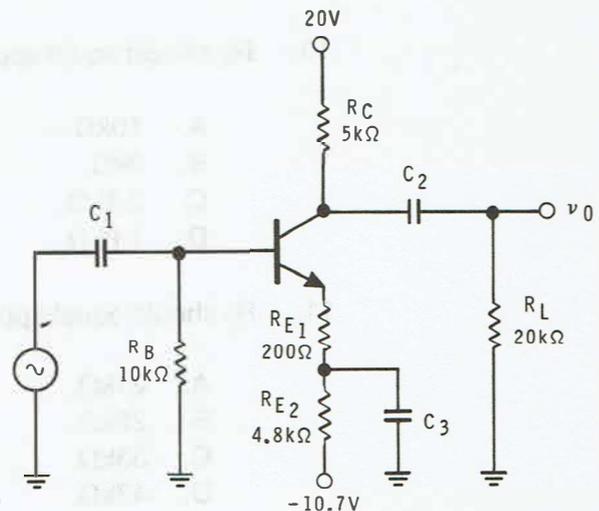


Figure 3-31

Circuit for Unit Examination questions 4-8.

6. The circuit's output resistance is approximately:
- A. $4\text{k}\Omega$.
 - B. $5\text{k}\Omega$.
 - C. $10\text{k}\Omega$.
 - D. $20\text{k}\Omega$.
7. The clipping levels of v_O are approximately:
- A. $\pm 10.7\text{V}$.
 - B. $+10.7\text{V}$, -8.4V .
 - C. $+8.4\text{V}$, -10V .
 - D. $\pm 20\text{V}$.
8. The largest value of v_{IN} that results in an unclipped output voltage is approximately:
- A. 0.58V peak.
 - B. 0.46V peak.
 - C. 1V peak.
 - D. 1.2V peak.

Refer to Figure 3-32 for questions 9 through 15.

9. R_C should equal approximately:
- A. $14.2\text{k}\Omega$.
 - B. $13\text{k}\Omega$.
 - C. $10\text{k}\Omega$.
 - D. $8.76\text{k}\Omega$.
10. R_E should equal approximately:
- A. $10\text{k}\Omega$.
 - B. $3\text{k}\Omega$.
 - C. $2.1\text{k}\Omega$.
 - D. $1.8\text{k}\Omega$.
11. R_2 should equal approximately:
- A. $21\text{k}\Omega$.
 - B. $22\text{k}\Omega$.
 - C. $33\text{k}\Omega$.
 - D. $47\text{k}\Omega$.

12. R_1 should equal approximately:
- 142k Ω .
 - 10k Ω .
 - 86.7k Ω .
 - 129k Ω .
13. The smallest acceptable value for C_1 is:
- 4.48 μ F.
 - 30.3 μ F.
 - 56.8 μ F.
 - 65 μ F.
14. The smallest acceptable value for C_2 is:
- 12.72 μ F.
 - 30.3 μ F.
 - 56.8 μ F.
 - 65 μ F.
15. The smallest acceptable value for C_3 is:
- 4.48 μ F.
 - 30.3 μ F.
 - 56.8 μ F.
 - 05 μ F.

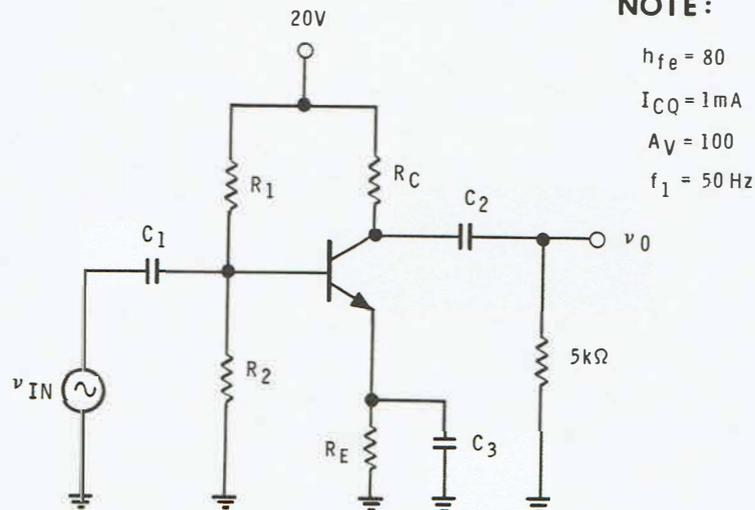


Figure 3-32

Circuit for Unit Examination questions 9-15.

15. The voltage across the resistor is 10 V.

- A. 10 Ω
- B. 20 Ω
- C. 30 Ω
- D. 40 Ω

16. The voltage across the resistor is 10 V.

- A. 4 Ω
- B. 8 Ω
- C. 16 Ω
- D. 32 Ω

17. The voltage across the resistor is 10 V.

- A. 10 Ω
- B. 20 Ω
- C. 30 Ω
- D. 40 Ω

18. The voltage across the resistor is 10 V.

- A. 4 Ω
- B. 8 Ω
- C. 16 Ω
- D. 32 Ω



FIGURE 3-10

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EXAMINATION ANSWERS

1. D — $A_{Vdb} = 20 \log A_V$
 $A_{Vdb} = 20 \log 50 = 33.9\text{db.}$

2. C — Since $A_{Vdb} = 80$, we have:

$$80 = 20 \log A_V$$

$$\log A_V = \frac{80}{20} = 4$$

Thus:

$$A_V = 10^4 = 10\,000$$

3. B — Since collector feedback is used, you must calculate the value of R_B' via Miller's theorem.

$$R_B' = \frac{R_B}{A_V + 1} = \frac{520\text{k}\Omega}{26} = 20\text{k}\Omega$$

The amplifier's input resistance equals $R_B' \parallel R_{IN(\text{BASE})}$. Thus:

$$R_{IN} = 20\text{k}\Omega \parallel 10\text{k}\Omega = 6.67\text{k}\Omega$$

4. A — First calculate the values of r_e' and r_L .

$$I_{CQ} = \frac{V_{EE} - V_{BE}}{R_E} = \frac{10.7\text{V} - 0.7\text{V}}{5\text{k}\Omega} = 2\text{mA}$$

$$r_e' = \frac{37\text{mV}}{I_{CQ}} = \frac{37\text{mV}}{2\text{mA}} = 18.5\Omega$$

$$r_L = R_C \parallel R_L = 5\text{k}\Omega \parallel 20\text{k}\Omega = 4\text{k}\Omega$$

Using the formula for voltage gain:

$$A_V = \frac{-r_L}{R_E + r_e'} = \frac{-4\text{k}\Omega}{200\Omega + 18.5\Omega} = -18.3$$

5. A — First calculate $R_{IN(BASE)}$:

$$R_{IN(BASE)} = h_{fe}(R_{E_1} + r_{e'}) = 150(218.5\Omega) = 32.8k\Omega$$

Since $R_B = 10k\Omega$, R_{IN} is:

$$R_{IN} = R_B || R_{IN(BASE)} = 10k\Omega || 32.8k\Omega = 7.66k\Omega$$

6. B — In a common-emitter amplifier $R_O \approx R_C$. Thus:

$$R_O \approx 5k\Omega$$

7. C — First calculate V_{CEQ} :

$$V_{CQ} = V_{CC} - I_{CQ}R_C = 20V - 2mA(5k\Omega) = 10V$$

$$V_{EQ} \approx -0.7V$$

$$V_{CEQ} = V_{CQ} - V_{EQ} = 10V - (-0.7V) = 10.7V$$

The negative clipping level, V^- , $\approx V_{CEQ}$ or 10.7V.

The positive clipping level, V^+ , $\approx I_{CQ}(R_{E_1} + r_L)$ Thus:

$$V^+ = 2mA(200\Omega + 4k\Omega) = 8.4V$$

8. B — From question 7 the largest possible, unclipped, output voltage is 8.4V peak. Since $A_V = 18.3$, the value of v_{IN} that produces an 8.4V peak output voltage is:

$$v_{IN} = \frac{v_O}{A_V} = \frac{8.4V}{18.3} = 0.46V \text{ peak}$$

For questions 9-15, the indicated steps correspond to those in the Design Guide.

9. A — 1. $I_{CQ} = 1mA$
 2. $r_{e'} = \frac{37mV}{I_{CQ}} = \frac{37mV}{1mA} = 37\Omega$
 3. $R_{E_1} = 0$ since the emitter resistor is fully bypassed.
 4. $r_L = A_V(R_{E_1} + r_{e'})$
 $r_L = 100(0 + 37\Omega) = 3.7k\Omega$
 5. $R_C = \frac{R_L r_L}{R_L - r_L} = \frac{5k\Omega(3.7k\Omega)}{5k\Omega - 3.7k\Omega} = 14.2k\Omega$

10. C — 6. $V_{CEQ} = I_{CQ}(R_{E_1} + r_L)$
 $V_{CEQ} = 1\text{mA}(0 + 3.7\text{k}\Omega) = 3.7\text{V}$

7. $V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CEQ}]$
 $V_{EQ} = 20\text{V} - [1\text{mA}(14.2\text{k}\Omega) + 3.7\text{V}]$
 $V_{EQ} = 20\text{V} - 17.9\text{V} = 2.1\text{V}$

8. $R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{2.1\text{V}}{1\text{mA}} = 2.1\text{k}\Omega$

11. A — 9. $R_{E_2} = R_E = 2.1\text{k}\Omega$ ($R_{E_1} = 0$)

10. $R_2 \leq 10R_E$
 $R_2 \leq 10(2.1\text{k}\Omega)$
 $R_2 \leq 21\text{k}\Omega$

12. D — 11. For this example $R_2 = 21\text{k}\Omega$:

$$R_1 = \frac{R_2(V_{CC} - V_{BQ})}{V_{BQ}}$$

Since $V_{EQ} = 2.1\text{V}$, $V_{BQ} = 2.1\text{V} + 0.7\text{V} = 2.8\text{V}$ Thus:

$$R_1 = \frac{21\text{k}\Omega(20\text{V} - 2.8\text{V})}{2.8\text{V}} = 129\text{k}\Omega$$

13. C — 12. First calculate R_{IN} :

$$R_{IN(\text{BASE})} = h_{fe}(R_{E_1} + r_e')$$

$$R_{IN(\text{BASE})} = 80(0 + 37\Omega) = 2.96\text{k}\Omega$$

$$R_B = R_1 \parallel R_2 = 12.9\text{k}\Omega \parallel 21\text{k}\Omega = 7.5\text{k}\Omega$$

$$R_{IN} = R_B \parallel R_{IN(\text{BASE})} = 7.5\text{k}\Omega \parallel 2.96\text{k}\Omega = 2.1\text{k}\Omega$$

Finally, the minimum value for C_1 is:

$$C_1 = \frac{3.18}{f_1 R_{IN}} = \frac{3.18}{50(2.1\text{k}\Omega)} = 30.3\mu\text{F}$$

14. A — 12. $C_2 = \frac{3.18}{f_1 R_L} = \frac{3.18}{50(5\text{k}\Omega)} = 12.72\mu\text{F}$

15. B — 12. $C_3 = \frac{3.18}{f_1 R_{E_2}} = \frac{3.18}{50(2.1\text{k}\Omega)} = 30.3\mu\text{F}$

10 - C - 5
 $V_{10} = V_{10} - V_{10} = 0$
 $V_{10} = V_{10} - V_{10} = 0$

11 - A - 8
 $V_{11} = V_{11} - V_{11} = 0$
 $V_{11} = V_{11} - V_{11} = 0$
 $V_{11} = V_{11} - V_{11} = 0$
 $V_{11} = V_{11} - V_{11} = 0$

12 - C - 11
 $V_{12} = V_{12} - V_{12} = 0$
 $V_{12} = V_{12} - V_{12} = 0$
 $V_{12} = V_{12} - V_{12} = 0$

13 - C - 12
 $V_{13} = V_{13} - V_{13} = 0$
 $V_{13} = V_{13} - V_{13} = 0$
 $V_{13} = V_{13} - V_{13} = 0$

14 - A - 15
 $V_{14} = V_{14} - V_{14} = 0$
 $V_{14} = V_{14} - V_{14} = 0$
 $V_{14} = V_{14} - V_{14} = 0$

15 - B - 12
 $V_{15} = V_{15} - V_{15} = 0$
 $V_{15} = V_{15} - V_{15} = 0$
 $V_{15} = V_{15} - V_{15} = 0$
 $V_{15} = V_{15} - V_{15} = 0$

16 - A - 15
 $V_{16} = V_{16} - V_{16} = 0$
 $V_{16} = V_{16} - V_{16} = 0$
 $V_{16} = V_{16} - V_{16} = 0$

17 - B - 12
 $V_{17} = V_{17} - V_{17} = 0$
 $V_{17} = V_{17} - V_{17} = 0$
 $V_{17} = V_{17} - V_{17} = 0$

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UNIT 4

**COMMON-BASE AND
COMMON- COLLECTOR
VOLTAGE AMPLIFIERS**

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INTRODUCTION

Unit 3 discussed the analysis and design of common-emitter voltage amplifiers. In this unit, you will learn how to analyze and design, single-stage, common-base and common-collector voltage amplifiers.

As you will see, the methods used to analyze and design these amplifiers are similar to the methods used to analyze and design common-emitter circuits. In a later unit, you will learn how single-stage amplifiers can be combined to produce multistage amplifiers.

Finally, we will discuss how BJT circuits can be analyzed by using hybrid parameters. Since most data sheets provide "hybrid parameter values," you should understand what these values mean, and how they can be converted to the AC parameters you are already familiar with.

UNIT OBJECTIVES

When you have completed this unit, you should be able to:

1. Analyze and design common-base voltage amplifiers.
2. Analyze and design common-collector amplifiers.
3. Analyze and design Darlington-pair emitter-followers.
4. Given h parameters for one configuration, calculate the h parameters for the other two configurations.
5. Estimate values of α , B , r_e' , r_b' and r_c' from h parameter data sheet values.

UNIT ACTIVITY GUIDE

- Read section on “Common-Base Amplifiers.”
- Answer Self-Test Review questions 1-10.
- Perform Experiment 6 in Unit 9.
- Read section on “Common-Collector Amplifiers.”
- Answer Self-Test Review questions 11-22.
- Perform Experiment 7 in Unit 9.
- Read section on “Hybrid Parameters.”
- Answer Self-Test Review questions 23-32.
- Study Summary.
- Complete Unit Examination.
- Check Examination Answers.

COMMON-BASE AMPLIFIERS

In a common-base amplifier, the AC input signal is applied to the emitter terminal. As with common-emitter amplifiers, the AC output signal is taken from the collector terminal.

Compared to common-emitter amplifiers, common-base amplifiers have a very small input resistance. This is why common-emitter amplifiers are generally preferred for low and mid-frequency applications. High frequency effects will be discussed in Unit 9. Here, you will find that common-base circuits are, in some respects, superior to common-emitter circuits for high frequency applications.

DC Analysis

A typical common-base amplifier is illustrated in Figure 4-1A. Note that the polarity of the V_{EE} source is such that the emitter-base diode is forward biased. Similarly, the collector-base diode is reverse biased by V_{CC} .

By reducing the AC source to zero, and opening the capacitors, you obtain the DC equivalent circuit shown in Figure 4-1B. The analysis of this circuit is straightforward, and proceeds as follows:

Starting at the positive side of V_{EE} and going around the emitter-base loop in a clockwise direction, yields:

$$V_{EE} - I_E R_E - V_{BE} = 0$$

Thus, the DC emitter current, I_E , is:

$$I_E = \frac{V_{EE} - V_{BE}}{R_E} \approx I_C \quad (\text{Eq. 4-1})$$

Naturally:

$$I_B = \frac{I_C}{B} = \frac{I_C}{h_{FE}}$$

By starting at the positive side of V_{CC} and going around the collector-base loop in a clockwise direction, you obtain:

$$V_{CC} - V_{CB} - I_C R_C = 0$$

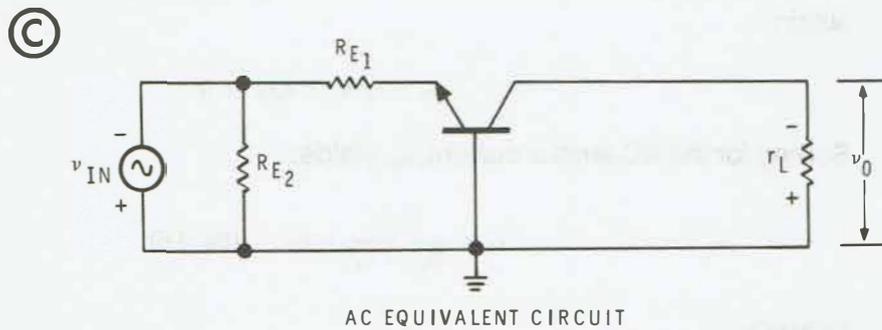
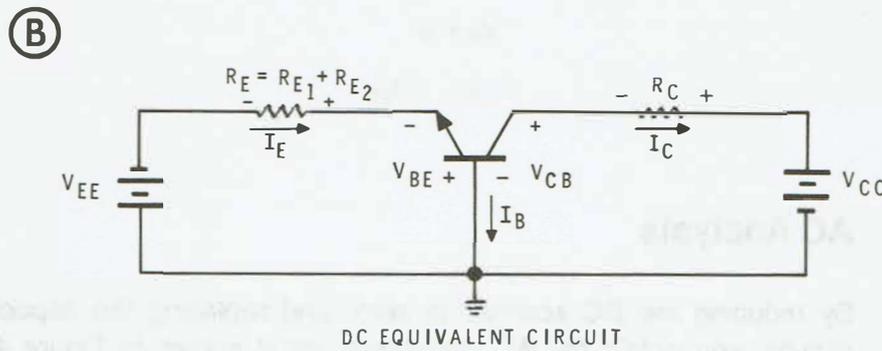
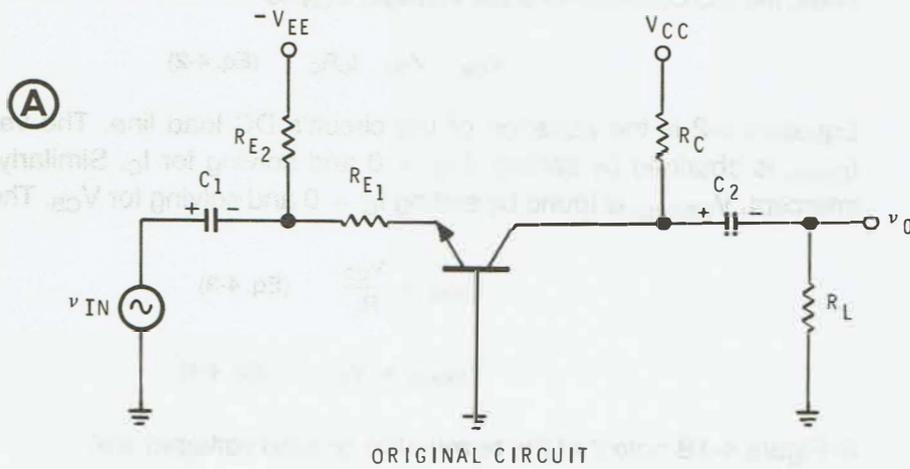


Figure 4-1

- A common base amplifier.
 A. Original circuit.
 B. DC equivalent circuit.
 C. AC equivalent circuit.

Thus, the DC collector-to-base voltage, V_{CB} , is:

$$V_{CB} = V_{CC} - I_C R_C \quad (\text{Eq. 4-2})$$

Equation 4-2 is the equation of the circuit's DC load line. The vertical intercept, $I_{C(\text{sat})}$, is obtained by setting $V_{CB} = 0$ and solving for I_C . Similarly, the horizontal intercept, $V_{CB(\text{cut})}$, is found by setting $I_C = 0$ and solving for V_{CB} . Therefore:

$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C} \quad (\text{Eq. 4-3})$$

$$V_{CB(\text{cut})} = V_{CC} \quad (\text{Eq. 4-4})$$

In Figure 4-1B note that the terminal-to-ground voltages are:

$$V_C = V_{CC} - I_C R_C \quad (\text{Eq. 4-5})$$

$$V_B = 0$$

$$V_E = -V_{BE}$$

AC Analysis

By reducing the DC sources to zero, and replacing the capacitors with short circuits, you obtain the AC equivalent circuit shown in Figure 4-1C. Since the transistor can be replaced with its AC model, the AC equivalent circuit can be redrawn as shown in Figure 4-2B. Here, by following the indicated path, you obtain:

$$v_{IN} - i_e R_{E_1} - i_e r_{e'} = 0$$

Solving for the AC emitter current, i_e , yields:

$$i_e = \frac{v_{IN}}{R_{E_1} + r_{e'}} \approx i_C \quad (\text{Eq. 4-6})$$

Naturally:

$$i_b = \frac{i_C}{\beta} = \frac{i_C}{h_{fe}}$$

In Figure 4-2B, note that the direction of i_C is such that when v_{IN} is negative, v_O is also negative. Consequently, in a common-base amplifier the input and output voltages are in phase with each other.

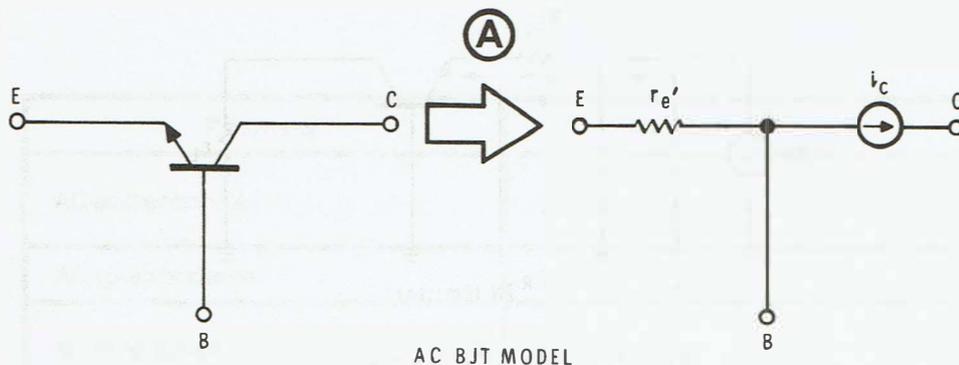
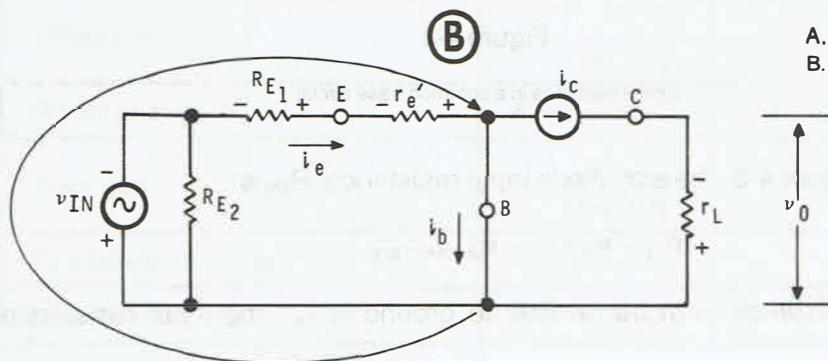


Figure 4-2

AC equivalent circuit for the amplifier in Figure 4-1A.

A. ACBJT model.

B. Replacing the BJT in Figure 4-1C with its AC model.



Since $v_O = v_C$ we have:

$$v_O = i_C r_L = \frac{v_{IN}}{R_{E1} + r_e'} r_L$$

Solving for the ratio of v_O to v_{IN} yields:

$$A_V = \frac{v_O}{v_{IN}} = \frac{r_L}{R_{E1} + r_e'} \quad (\text{Eq. 4-7})$$

Where:

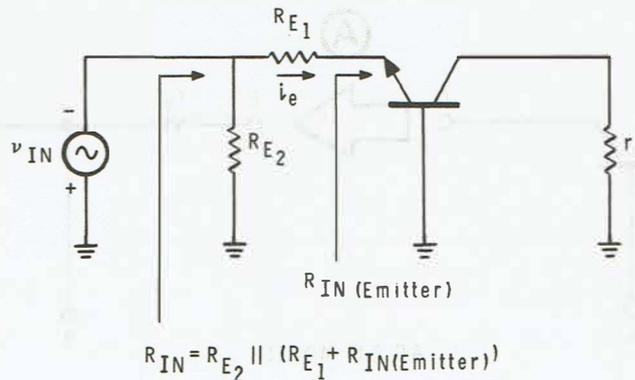
$$r_L = R_C \parallel R_L$$

Since the output current is i_C and the input current is i_e the current gain, A_i , is:

$$A_i = \frac{i_C}{i_e} = \alpha = h_{fb} \approx 1 \quad (\text{Eq. 4-8})$$

Also since the power gain is the product of the current and voltage gains:

$$A_p = A_i A_V = \frac{h_{fb} r_L}{R_{E1} + r_e'} \quad (\text{Eq. 4-9})$$

**Figure 4-3**

Input resistance in a common base circuit.

As indicated in Figure 4-3, the amplifier's input resistance, R_{IN} is:

$$R_{IN} = R_{E2} \parallel (R_{E1} + R_{IN(\text{EMITTER})})$$

Since the AC resistance from the emitter to ground is r_e' , the input resistance is:

$$R_{IN} = R_{E2} \parallel (R_{E1} + r_e') \quad (\text{Eq. 4-10})$$

Recall that the input resistance of a common-emitter amplifier is:

$$R_{IN} = R_B \parallel h_{ie}(R_E + r_e')$$

Comparing Equation 4-10 with the previous expression for a common-emitter amplifier indicates that the input resistance of a common-base amplifier is considerably smaller than the input resistance of a comparable common-emitter amplifier. This small input resistance is the principle disadvantage of a common-base amplifier.

A summary of the various AC formulas for the common-base amplifier is provided in Table 4-1. Note that the formulas for current gain, power gain, and input resistances are different from the common-emitter formulas discussed in Unit 3. As with the common-emitter amplifier, the output resistance of a common-base amplifier is approximately equal to the value of the collector resistor, R_C .

Parameter	Approximate Formula
AC emitter current	$i_e = \frac{v_{IN}}{R_{E_1} + r_e'}$
AC collector current	$i_c \approx i_e$
AC base current	$i_b = \frac{i_c}{h_{fe}}$
Voltage gain	$A_v = \frac{r_L}{R_{E_1} + r_e'}$
Current gain	$A_i = h_{fb} \approx 1$
Power gain	$A_p = \frac{h_{fb} r_L}{R_{E_1} + r_e'}$
Input resistance (emitter)	$R_{IN(EMITTER)} = r_e'$
Input resistance (total)	$R_{IN} = R_{E_2} \parallel (R_{E_1} + r_e')$
Output resistance	$R_O \approx R_C$
<u>Comments</u>	
$\alpha_{AC} = h_{fb} = \frac{B}{B + 1} \approx 1$ <p>Typically, $\frac{26mV}{I_E} \leq r_e' \leq \frac{52mV}{I_E}$. For purposes of calculation use $r_e' = \frac{37mV}{I_E}$</p> <p>R_{IN} is small compared to a common-emitter circuit.</p> <p>v_O and v_{IN} are in phase with each other.</p>	

TABLE 4-1

Common-base AC formula summary guide.

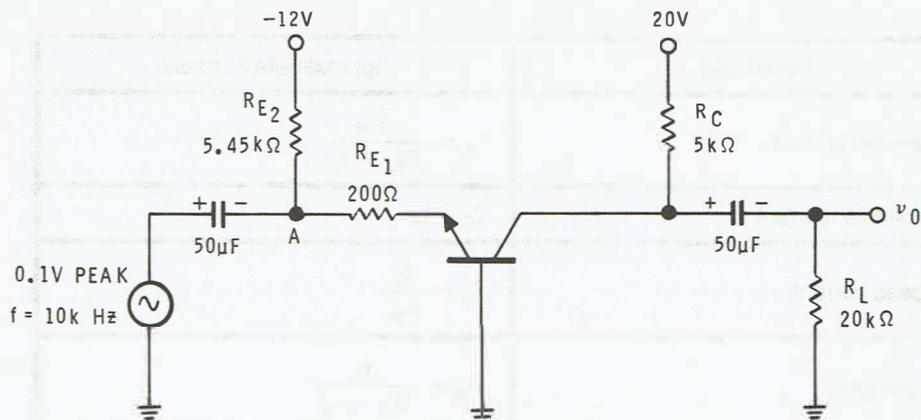


Figure 4-4

Circuit for Example 4-1.

Example 4-1

Calculate the voltage gain and input resistance for the circuit shown in Figure 4-4. Also sketch the voltage from point A to ground.

$$I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{12V - 0.7V}{5.45k\Omega + 200\Omega} = \frac{11.3V}{5.65k\Omega} = 2mA$$

$$r_{e'} = \frac{37mV}{I_E} = \frac{37mV}{2mA} = 18.5\Omega$$

$$A_V = \frac{r_L}{R_{E1} + r_{e'}} = \frac{5k\Omega || 20k\Omega}{200\Omega + 18.5\Omega} = \frac{4k\Omega}{218.5\Omega} = 18.3$$

$$R_{IN} = R_{E2} || (R_{E1} + r_{e'})$$

$$R_{IN} = 5.45k\Omega || (200\Omega + 18.5\Omega)$$

$$R_{IN} = 210\Omega$$

Since V_{EE} is negative with respect to ground, the DC voltage from point A to ground will also be negative. This is why the input coupling capacitor has its negative side connected to point A. The **magnitude** of the DC voltage from point A to ground is:

$$V_A = V_{EE} - I_E R_{E_2}$$

$$V_A = 12V - 2mA(5.45k\Omega) = 1.1V$$

Since the input coupling capacitor approximates a short circuit, the AC voltage from point A to ground equals v_{IN} , or 0.1V peak in this example.

The total voltage is the sum of the DC, and AC components. Therefore, the voltage from point A to ground appears as shown in Figure 4-5.

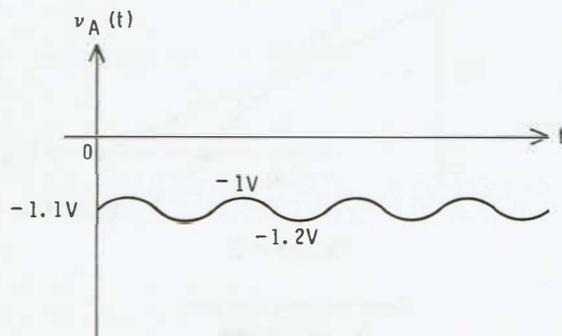


Figure 4-5

A sketch of $v_A(t)$ for Example 4-1.

Common-Base AC Load Line

An examination of the DC and AC equivalent circuits in Figure 4-1 indicates the following:

1. The DC resistance between the collector and base equals R_C .
2. The AC resistance between the collector and base equals r_L .

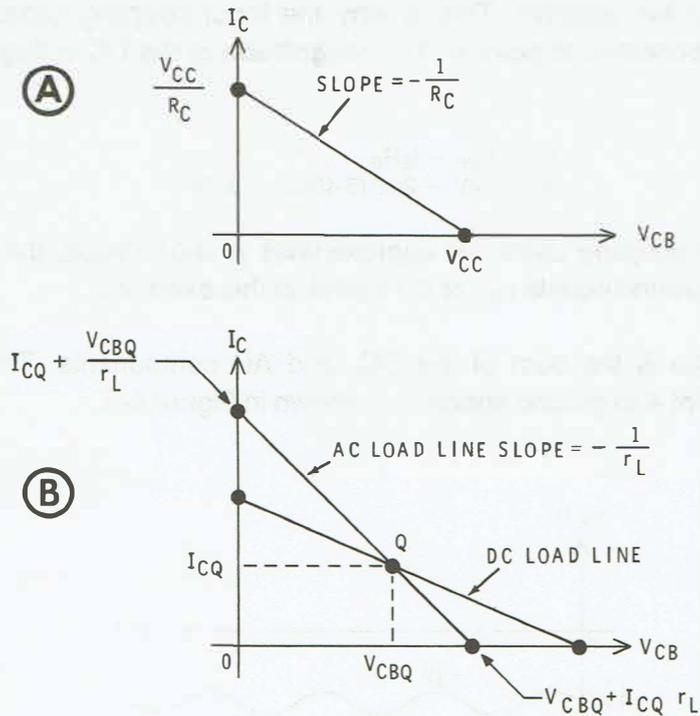


Figure 4-6

Common base load lines.

- A. DC load line.
- B. AC load line.

Based on these observations, it is apparent that the DC load line has a slope of $-1/R_C$, and the AC load line a slope of $-1/r_L$. A sketch of the DC and AC load lines for the collector-base circuit is provided in Figure 4-6. Since both the slope and the coordinates of a point on the AC load line are known, you can apply the point slope formula to determine the equation of the AC load line. Thus, by applying the general equation $y - y_1 = m(x - x_1)$ to Figure 4-6B you obtain:

$$I_C - I_{CQ} = \frac{-1}{r_L} (V_{CB} - V_{CBQ}) \quad (\text{Eq. 4-11})$$

Equation 4-11 is the equation of the AC load line in a common-base circuit. The intercept values are obtained in the usual manner. In this case:

$$i_{C(\text{sat})} = I_{CQ} + \frac{V_{CBQ}}{r_L} \quad (\text{Eq. 4-12})$$

$$v_{CB(\text{cut})} = V_{CBQ} + I_{CQ}r_L \quad (\text{Eq. 4-13})$$

Similarly, the clipping levels are approximated by:

$$V^+ = I_{CQ}r_L \quad (\text{Eq. 4-14})$$

$$V^- = V_{CBQ} \quad (\text{Eq. 4-15})$$

Example 4-2

Estimate the clipping levels for the common-base amplifier of Example 4-1.

Recall that $I_{CQ} = 2\text{mA}$, and $r_L = 4\text{k}\Omega$. In Figure 4-4, $V_C = V_{CBQ}$. Thus:

$$V_{CBQ} = V_{CC} - I_{CQ}R_C$$

$$V_{CBQ} = 20\text{V} - 2\text{mA}(5\text{k}\Omega) = 10\text{V}$$

Therefore:

$$V^+ = I_{CQ}r_L = 2\text{mA}(4\text{k}\Omega) = 8\text{V peak}$$

$$V^- = V_{CBQ} = 10\text{V peak}$$

Since the clipping levels are not equal, the Q point is not located in the center of the AC load line.

By examining the AC load line in Figure 4-6B, it is clear that in a **common-base** circuit, a centered Q point results if:

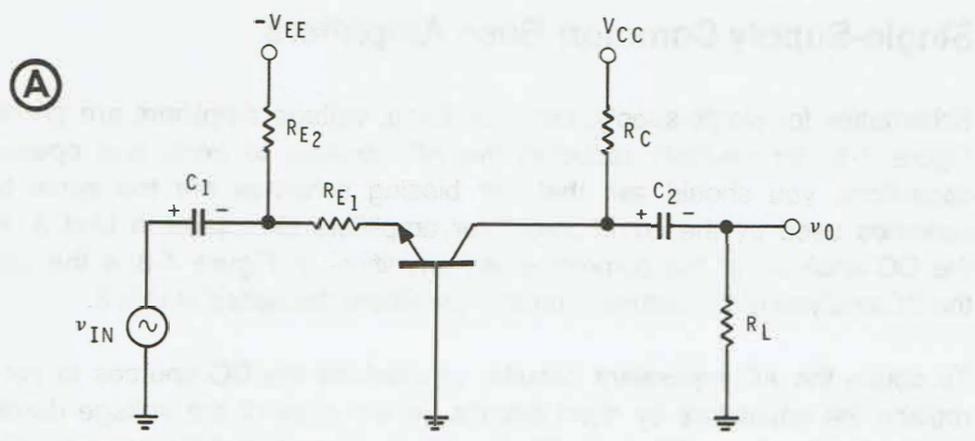
$$I_{CQ} = \frac{V_{CBQ}}{r_L} \quad (\text{Eq. 4-16})$$

The common-base amplifier of Figure 4-1A is reproduced in Figure 4-7A. By redrawing the circuit, you obtain the circuit shown in Figure 4-7B. Here, you should recognize the biasing scheme as the emitter-bias circuit introduced in Unit 2. In this case, however, $R_B = 0$ because the base of the transistor is connected **directly** to ground.

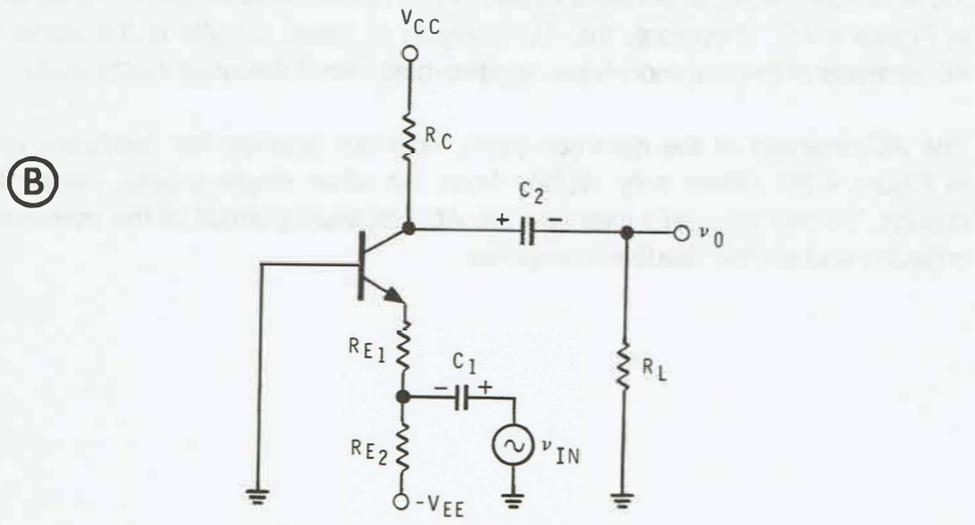
The AC equivalent circuit of the amplifier in Figure 4-7B is illustrated in Figure 4-7C. Naturally, this circuit is the same equivalent circuit as the one provided in Figure 4-1C. Only the manner in which the two circuits are drawn is different.

The point to be emphasized is this:

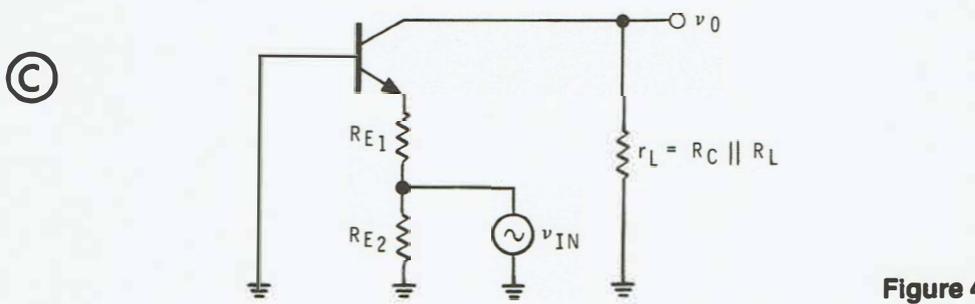
Some schematic diagrams draw a common-base amplifier, that uses emitter bias, as shown in Figure 4-7A, while others draw the circuit as shown in Figure 4-7B. You should recognize that each schematic represents the **same** physical circuit.



COMMON BASE AMPLIFIER OF FIGURE 4-1A



REDRAWING THE CIRCUIT



AC EQUIVALENT CIRCUIT

Figure 4-7

The common base amplifier in Figure 4-1A can be redrawn as shown above. When this is done it is obvious that the circuit utilizes emitter bias.

- A. Common base amplifier of Figure 4-1A.
- B. Redrawing the circuit.
- C. AC equivalent circuit.

Single-Supply Common-Base Amplifiers

Schematics for single-supply, common-base, voltage amplifiers are provided in Figure 4-8. By mentally reducing the AC sources to zero, and opening the capacitors, you should see that the biasing schemes are the same biasing schemes used by the common-emitter amplifiers discussed in Unit 3. Hence, the DC analysis of the common-base amplifiers in Figure 4-8 is the same as the DC analysis of the common-emitter amplifiers discussed in Unit 3.

To obtain the AC equivalent circuits, you reduce the DC sources to zero, and replace the capacitors by short circuits. In the case of the voltage divider and emitter feedback amplifiers, in Figure 4-8, the resulting AC equivalent circuit is the same as the AC equivalent circuit of the common-base, emitter-bias amplifier in Figure 4-7C. Therefore, the AC analysis of these circuits is the same as the AC analysis of the common-base, emitter-bias circuit discussed previously!

The AC analysis of the common-base, collector and emitter feedback amplifier in Figure 4-8C differs only slightly from the other single-supply, common-base circuits. To see why, let's examine the AC equivalent circuit of the common-base collector and emitter feedback amplifier.

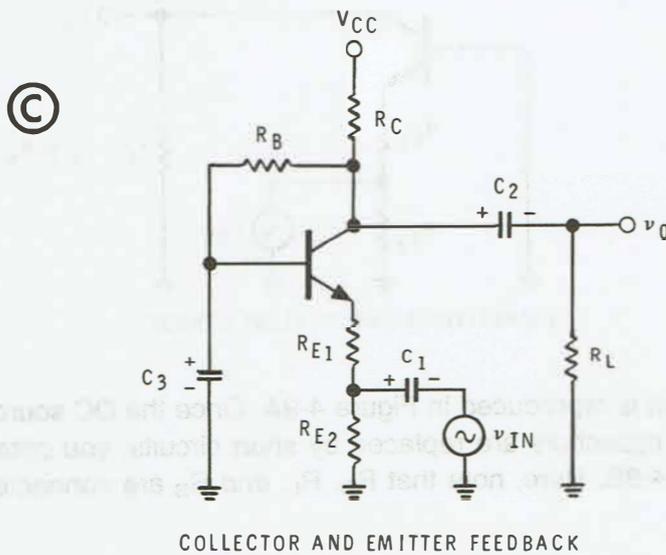
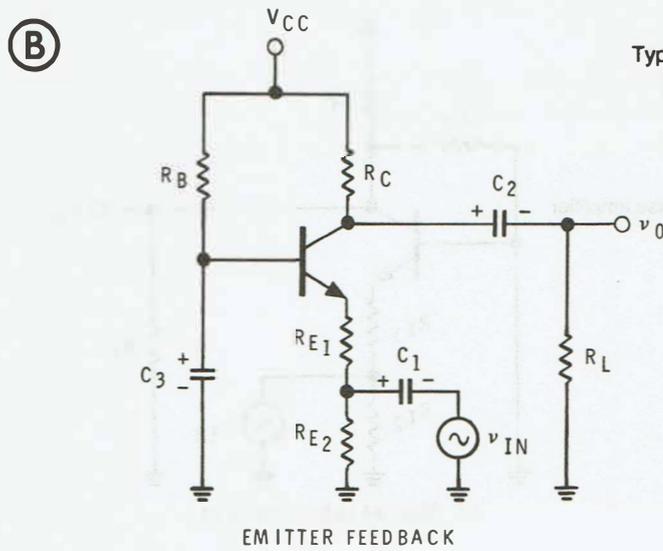
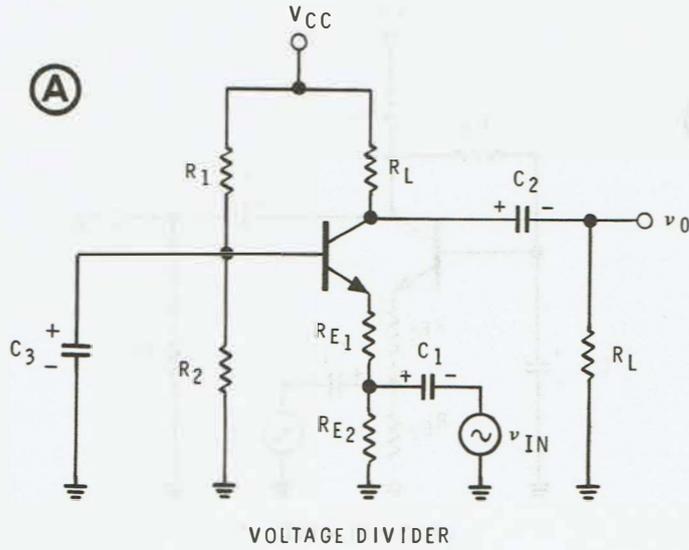


Figure 4-8

Typical single supply common base amplifiers.

- A. Voltage divider.
- B. Emitter feedback.
- C. Collector and emitter feedback.

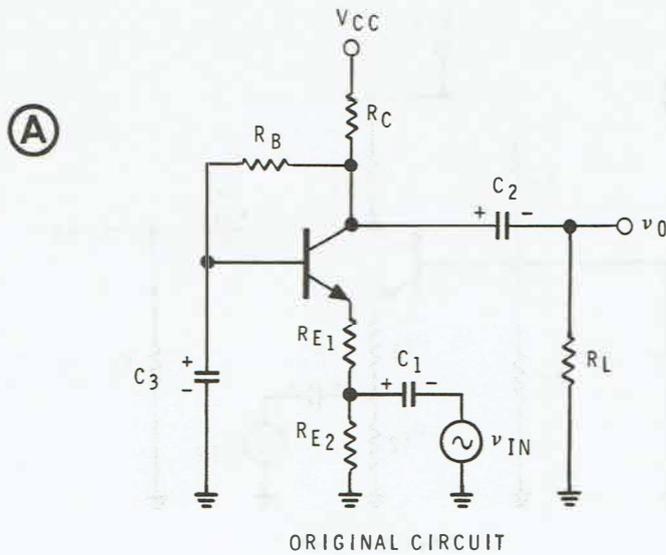
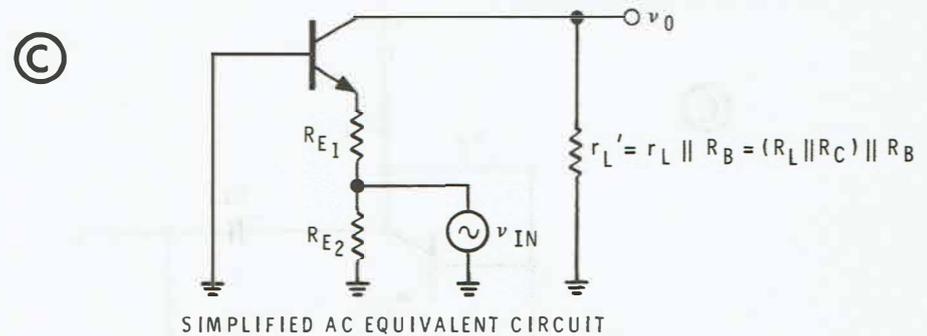
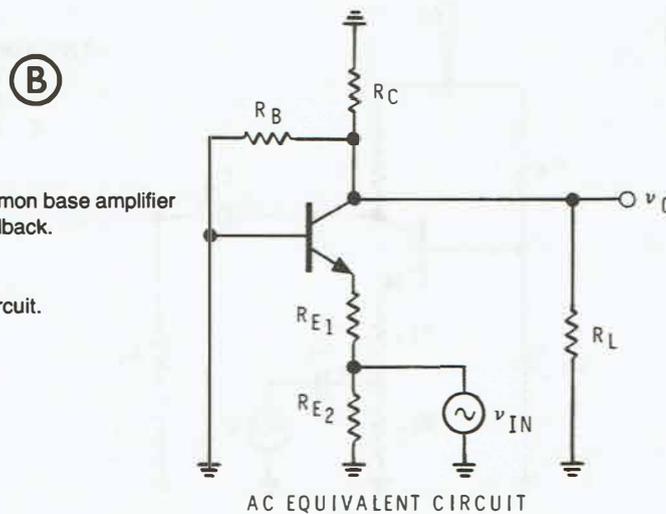


Figure 4-9

Developing the AC equivalent circuit for a common base amplifier utilizing collector and emitter feedback.

- A. Original circuit.
- B. AC equivalent circuit.
- C. Simplified AC equivalent circuit.



The original circuit is reproduced in Figure 4-9A. Once the DC source is reduced to zero, and the capacitors are replaced by short circuits, you obtain the circuit shown in Figure 4-9B. Here, note that R_C , R_L , and R_B are connected in parallel.

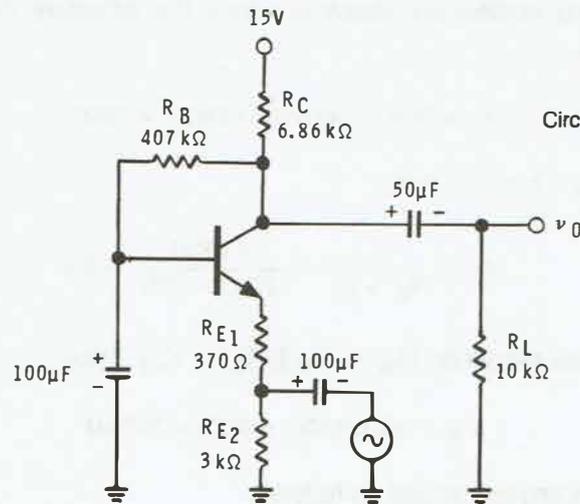


Figure 4-10

Circuit for Example 4-3.

For this reason, the circuit in Figure 4-9B reduces to the AC equivalent circuit of Figure 4-9C. The effective AC load resistance, r_L' , equals the parallel combination of r_L and R_B . Thus, when you analyze a common-base, collector and emitter feedback amplifier, r_L should be replaced by r_L' .

Incidentally, in most circuits $R_B \gg r_L$. For this reason, the parallel combination of r_L and R_B , r_L' , is approximately equal to the value of r_L .

Example 4-3

Calculate the voltage gain and input resistance for the amplifier in Figure 4-10. Also, estimate the positive and negative clipping levels. For calculation purposes, assume $h_{FE} = 100$.

In a collector and emitter feedback circuit:

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + R_E + \frac{R_B}{h_{FE}}}$$

Thus:

$$I_C = \frac{15V - 0.7V}{6.86k\Omega + 3.37k\Omega + \frac{407k\Omega}{100}} = \frac{14.3V}{14.3k\Omega} = 1mA = I_{CQ}$$

$$r_e' = \frac{37mV}{I_{CQ}} = \frac{37mV}{1mA} = 37\Omega$$

$$r_L = R_C || R_L = 6.86k\Omega || 10k\Omega = 4.07k\Omega$$

Since collector and emitter feedback is used, the effective AC load resistance, r_L' , is:

$$r_L' = R_B \parallel r_L = 407\text{k}\Omega \parallel 4.07\text{k}\Omega = 4.03\text{k}\Omega$$

Note that since $R_B \gg r_L$, $r_L' \approx r_L$

$$A_V = \frac{r_L'}{R_{E_1} + r_e'} = \frac{4.03\text{k}\Omega}{370\Omega + 37\Omega} = 9.9$$

For a common-base amplifier, $R_{IN} = R_{E_2} \parallel (R_{E_1} + r_e')$. Thus:

$$R_{IN} = 3\text{k}\Omega \parallel (370\Omega + 37\Omega) = 358.4\Omega$$

The clipping levels are estimated as follows:

$$V^+ = I_{CQ} r_L' = 1\text{mA}(4.03\text{k}\Omega) = 4.03\text{V}$$

$$V^- = V_{CBQ} = V_{CQ} - V_{BQ}$$

In this case:

$$V_{CQ} = V_{CC} - I_{CQ} R_C = 15\text{V} - 1\text{mA}(6.86\text{k}\Omega) = 8.14\text{V}$$

$$V_{BQ} = V_{BE} + V_{EQ} = 0.7\text{V} + 1\text{mA}(3.37\text{k}\Omega) = 4.07\text{V}$$

Thus:

$$V^- = 8.14\text{V} - 4.07\text{V} = 4.07\text{V}$$

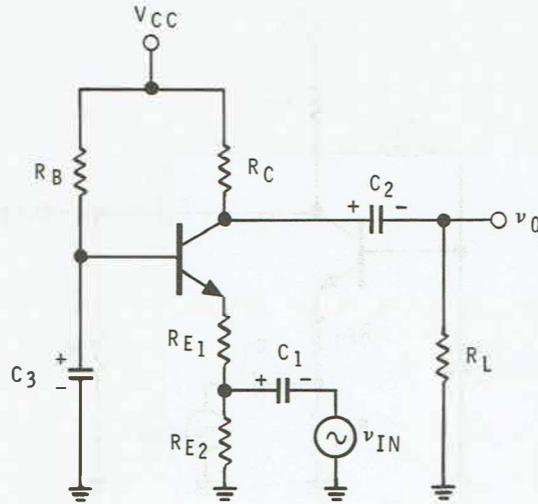
Since $V^+ \approx V^-$, it is clear that the Q point is located near the center of the AC load line. Incidentally, if you assume $r_L' = r_L = 4.07\text{k}\Omega$, the calculated values for the clipping levels are $\pm 4.07\text{V}$. As you can see, the error introduced by making this assumption is quite small.

Designing Common-Base Voltage Amplifiers

With relatively minor changes, the procedure used in Unit 3 to design common-emitter amplifiers can also be used to design common-base amplifiers. The following design guide for common-base amplifiers is very similar to the one provided in Unit 3 for common-emitter amplifiers.

In the case of the collector and emitter feedback amplifier, it is assumed that R_B is sufficiently large so that r_L' is closely approximated by the value of r_L . As before, high gain amplifiers are designed by setting $R_{E_1} = 0$ in the appropriate formulas.

COMMON-BASE VOLTAGE AMPLIFIER DESIGN GUIDE EMITTER FEEDBACK



1

1. Select I_{CQ} .
2. Calculate r_e' .

$$r_e' = \frac{37\text{mV}}{I_{CQ}}$$

3. Select R_{E1} .

$$R_{E1} = 5 \text{ to } 10 \text{ times } r_e'$$

4. Calculate r_L .

$$r_L = A_v(R_{E1} + r_e')$$

5. Calculate R_C .

$$R_C = \frac{R_L r_L}{R_L - r_L}$$

6. Calculate V_{CBQ} .

$$V_{CBQ} = I_{CQ} r_L$$

7. Calculate V_{EQ} .

$$V_{EQ} = V_{CC} - [I_{CQ} R_C + V_{CBQ} + V_{BE}]$$

8. Calculate R_E .

$$R_E = \frac{V_{EQ}}{I_{CQ}}$$

9. Calculate R_{E2} .

$$R_{E2} = R_E - R_{E1}$$

10. Calculate R_B .

$$R_B = \frac{V_{CC} - [V_{BE} + V_{EQ}]}{I_{BQ}}$$

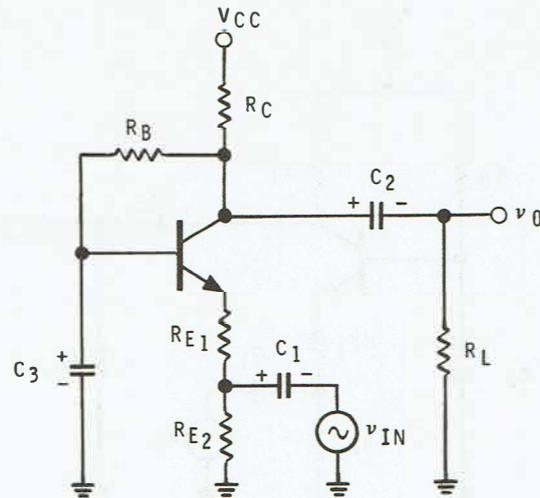
11. Select capacitors.

$$C_1 \geq \frac{3.18}{f_1 R_{IN}}, \quad C_2 \geq \frac{3.18}{f_1 R_L}$$

$$C_3 \geq \frac{3.18}{f_1 R_{IN}'} \quad R_{IN}' = R_B \parallel h_{fe}(R_{E1} + r_e')$$

COLLECTOR AND EMITTER FEEDBACK

2



1. Select I_{CQ} .
2. Calculate r_e' .

$$r_e' = \frac{37\text{mV}}{I_{CQ}}$$

3. Select R_{E1} .
4. Calculate r_L .
5. Calculate R_C .

$$R_{E1} = 5 \text{ to } 10 \text{ times } r_e'$$

$$r_L = A_V(R_{E1} + r_e')$$

$$R_C = \frac{R_L r_L}{R_L - r_L}$$

6. Calculate V_{CBQ} .
7. Calculate V_{EQ} .
8. Calculate R_E .

$$V_{CBQ} = I_{CQ} r_L$$

$$V_{EQ} = V_{CC} - [I_{CQ} R_C + V_{CBQ} + V_{BE}]$$

$$R_E = \frac{V_{EQ}}{I_{CQ}}$$

9. Calculate R_{E2} .
10. Calculate R_B .

$$R_{E2} = R_E - R_{E1}$$

$$R_B = \frac{V_{CBQ}}{I_{BQ}}$$

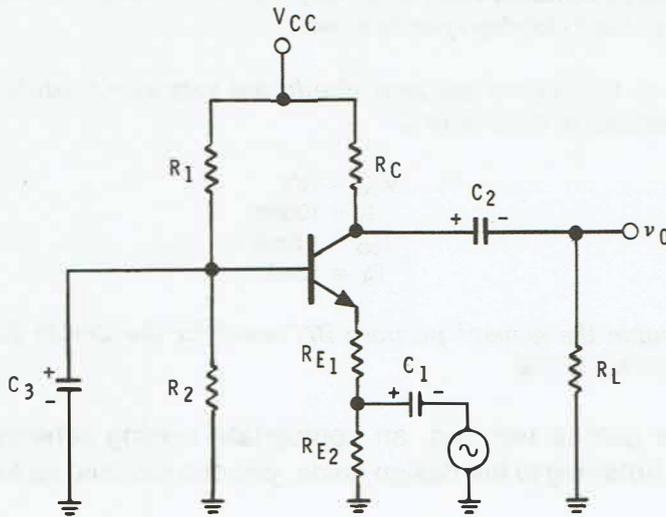
11. Select capacitors.

$$C_1 \geq \frac{3.18}{f_1 R_{IN}}, \quad C_2 \geq \frac{3.18}{f_1 R_L}$$

$$C_3 \geq \frac{3.18}{f_1 R_{IN}'} \quad R_{IN}' = h_{fe}(R_{E1} + r_e')$$

VOLTAGE DIVIDER

3



1. Select I_{CQ} .
2. Calculate r_e' .

$$r_e' = \frac{37\text{mV}}{I_{CQ}}$$

3. Calculate R_{E1} .
4. Calculate r_L .
5. Calculate R_C .

$$R_{E1} = 5 \text{ to } 10 \text{ times } r_e'$$

$$r_L = A_v(R_{E1} + r_e')$$

$$R_C = \frac{R_L r_L}{R_L - r_L}$$

6. Calculate V_{CBQ} .
7. Calculate V_{EQ} .
8. Calculate R_E .

$$V_{CBQ} = I_{CQ} r_L$$

$$V_{EQ} = V_{CC} - [I_{CQ} R_C + V_{CBQ} + V_{BE}]$$

$$R_E = \frac{V_{EQ}}{I_{CQ}}$$

9. Calculate R_{E2} .
10. Select R_2 .
11. Calculate R_1 .

$$R_{E2} = R_E - R_{E1}$$

$$R_2 \leq 10 R_E$$

$$R_1 = \frac{R_2(V_{CC} - V_{BQ})}{V_{BQ}}$$

12. Select capacitors.

$$C_1 \geq \frac{3.18}{f_1 R_{IN}}, \quad C_2 \geq \frac{3.18}{f_1 R_L}$$

$$C_3 \geq \frac{3.18}{f_1 R_{IN}'} \quad R_{IN}' = R_1 \parallel R_2 \parallel h_{ie}(R_{E1} + r_e')$$

Example 4-4

Design a common-base, single-supply voltage amplifier according to the following specifications:

$A_V = 12$. The voltage gain should not vary significantly with variations in h_{FE} and/or r_e' .

$$\begin{aligned} V_{CC} &= 15V \\ f_1 &= 100\text{Hz} \\ I_{CQ} &= 1.5\text{mA} \\ R_L &= 12\text{k}\Omega \end{aligned}$$

Assume the general purpose BJT used for the design has an $h_{FE} \approx h_{fe} = 150$.

Since a stable gain is required, an appropriate biasing scheme is the voltage divider circuit. Referring to the design guide, you can proceed as follows:

1. $I_{CQ} = 1.5\text{mA}$
2. $r_e' = \frac{37\text{mV}}{I_{CQ}} = \frac{37\text{mV}}{1.5\text{mA}} = 24.7\Omega$
3. $R_{E1} = 10r_e' = 10(24.7\Omega) = 247\Omega$
4. $r_L = A_V(R_{E1} + r_e') = 12(247\Omega + 24.7\Omega) = 3.26\text{k}\Omega$
5. $R_C = \frac{R_L r_L}{R_L - r_L} = \frac{12\text{k}\Omega(3.26\text{k}\Omega)}{12\text{k}\Omega - 3.26\text{k}\Omega} = 4.48\text{k}\Omega$
6. $V_{CBQ} = I_{CQ}r_L = 1.5\text{mA}(3.26\text{k}\Omega) = 4.89\text{V}$
7. $V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CBQ} + V_{BE}]$
 $= 15\text{V} - [1.5\text{mA}(4.48\text{k}\Omega) + 4.89\text{V} + 0.7\text{V}]$
 $= 15\text{V} - 12.31\text{V}$
 $= 2.69\text{V}$

$$8. R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{2.69V}{1.5mA} = 1.79k\Omega$$

$$9. R_{E_2} = R_E - R_{E_1} = 1.79k\Omega - 247\Omega = 1.54k\Omega$$

10. $R_2 \leq 10R_E$. Since $R_E = 1.79k\Omega$, a reasonable choice for R_2 is $3.3k\Omega$.

$$11. R_1 = \frac{R_2(V_{CC} - V_{BQ})}{V_{BQ}}$$

Since $V_{EQ} = 2.69V$, $V_{BQ} = 2.69V + 0.7V = 3.39V$. Thus:

$$R_1 = \frac{3.3k\Omega(15V - 3.39V)}{3.39V} = 11.3k\Omega$$

12. First calculate the equivalent resistance seen by C_1 , R_{IN} , and C_3 , R_{IN} .

$$R_{IN} = R_{E_2} \parallel (R_{E_1} + r_{e'})$$

$$R_{IN} = 1.54k\Omega \parallel (247\Omega + 24.7\Omega)$$

$$R_{IN} = 1.54k\Omega \parallel 271.7\Omega = 230\Omega$$

$$R_{IN}' = R_1 \parallel R_2 \parallel h_{ie}(R_{E_1} + r_{e'})$$

$$R_{IN}' = 11.3k\Omega \parallel 3.3k\Omega \parallel 150(271.7\Omega)$$

$$R_{IN}' = 2.55k\Omega \parallel 40.8k\Omega = 2.4k\Omega$$

Next, calculate the minimum capacitor values.

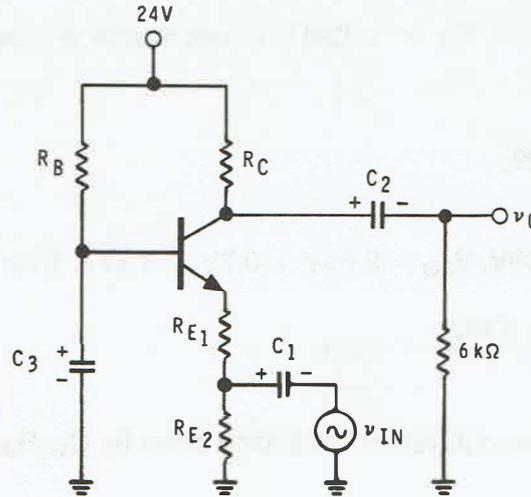
$$C_1 = \frac{3.18}{f_1 R_{IN}} = \frac{3.18}{100(230\Omega)} = 138.3\mu F$$

$$C_2 = \frac{3.18}{f_1 R_C} = \frac{3.18}{100(12k\Omega)} = 2.65\mu F$$

$$C_3 = \frac{3.18}{f_1 R_{IN}'} = \frac{3.18}{100(2.4k\Omega)} = 13.3\mu F$$

Self-Test Review

Refer to Figure 4-11 for questions 1 through 10.



$$R_{E1} = 10 r_{e'}$$

$$f_1 = 200 \text{ Hz}$$

$$h_{FE} = 100$$

$$h_{fe} = 90$$

$$I_{CQ} = 2 \text{ mA}$$

Figure 4-11

Circuit for Self-Test Review questions 1-10.

Assume the circuit is designed to provide a voltage gain of 15.

1. R_{E1} should equal approximately _____ Ω .
2. R_C should equal approximately _____ $k\Omega$.
3. R_{E2} should equal approximately _____ $k\Omega$.
4. R_B should equal approximately _____ $k\Omega$.
5. C_1 should have a DC voltage rating larger than _____ V.

6. C_1 should exceed approximately _____ μF .
7. C_2 should exceed approximately _____ μF .
8. C_3 should exceed approximately _____ μF .
9. If R_{E_1} was shorted, the voltage gain would increase to approximately _____.
10. If R_{E_1} was shorted, the input resistance seen by the signal source would be approximately _____ Ω .

Answers

- | | |
|--------------------------|----------------------|
| 1. 185Ω | 6. $85.3\mu\text{F}$ |
| 2. $6.2\text{k}\Omega$ | 7. $2.65\mu\text{F}$ |
| 3. $2.215\text{k}\Omega$ | 8. $0.9\mu\text{F}$ |
| 4. $925\text{k}\Omega$ | 9. 164.9 |
| 5. 4.43V | 10. 18.5Ω |

The solution to questions 1 through 10 follow.

Generally speaking, the following calculations follow the procedure outlined in the common-base design guide for the emitter feedback circuit.

1. Since $I_{CQ} = 2\text{mA}$ and $r_e' = 18.5\Omega$:

$$R_{E_1} = 10r_e' = 10(18.5\Omega) = 185\Omega$$

2. To determine the value of R_C , first calculate the value required for r_L :

$$r_L = A_v(R_{E_1} + r_e') = 15(185\Omega + 18.5\Omega) = 3.05\text{k}\Omega$$

Then:

$$R_C = \frac{R_L r_L}{R_L - r_L} = \frac{6\text{k}\Omega(3.05\text{k}\Omega)}{6\text{k}\Omega - 3.05\text{k}\Omega} = 6.2\text{k}\Omega$$

3. Before R_{E_2} can be calculated, you need to determine values for V_{CBQ} , V_{EQ} , and R_E . Thus:

$$V_{CBQ} = I_{CQ}r_L = 2\text{mA}(3.05\text{k}\Omega) = 6.1\text{V}$$

$$\begin{aligned} V_{EQ} &= V_{CC} - [I_{CQ}R_C + V_{CBQ} + V_{BE}] \\ V_{EQ} &= 24\text{V} - [2\text{mA}(6.2\text{k}\Omega) + 6.1\text{V} + 0.7\text{V}] \\ V_{EQ} &= 24\text{V} - 19.2\text{V} = 4.8\text{V} \end{aligned}$$

$$R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{4.8\text{V}}{2\text{mA}} = 2.4\text{k}\Omega$$

Now:

$$\begin{aligned} R_{E_2} &= R_E - R_{E_1} \\ R_{E_2} &= 2.4\text{k}\Omega - 185\Omega = 2.215\text{k}\Omega \end{aligned}$$

4. Since $I_{CQ} = 2\text{mA}$ and $h_{FE} = 100$, $I_{BQ} = 2\text{mA}/100$ or $20\mu\text{A}$. Thus:

$$R_B = \frac{V_{CC} - [V_{BE} + V_{EQ}]}{I_{BQ}}$$

$$R_B = \frac{24\text{V} - [0.7\text{V} + 4.8\text{V}]}{20\mu\text{A}} = 925\text{k}\Omega$$

5. C_1 charges to the DC voltage across R_{E_2} . Thus the DC voltage rating of C_2 should exceed $I_{CQ}R_{E_2}$. In this case:

$$I_{CQ}R_{E_2} = 2\text{mA}(2.215\text{k}\Omega) = 4.43\text{V}$$

6. To calculate the minimum size required for C_1 , you must first calculate R_{IN} . In this case:

$$\begin{aligned} R_{IN} &= R_{E_2} \parallel (R_{E_1} + r_{e'}) \\ R_{IN} &= 2.215\text{k}\Omega \parallel (185\Omega + 18.5\Omega) \\ R_{IN} &= 2.215\text{k}\Omega \parallel 203.5\Omega = 186.4\Omega \end{aligned}$$

Now:

$$C_1 = \frac{3.18}{f_1 R_{IN}} = \frac{3.18}{200(186.4\Omega)} = 85.3\mu\text{F}$$

$$7. \quad C_2 = \frac{3.18}{f_1 R_L} = \frac{3.18}{200(6\text{k}\Omega)} = 2.65\mu\text{F}$$

8. To determine the value of C_3 , first calculate R_{IN}' .

$$\begin{aligned} R_{IN}' &= R_B \parallel h_{fe}(R_{E_1} + r_{e'}) \\ R_{IN}' &= 925\text{k}\Omega \parallel 90(185 + 18.5\Omega) \\ R_{IN}' &= 925\text{k}\Omega \parallel 18.315\text{k}\Omega = 17.6\text{k}\Omega \end{aligned}$$

Now:

$$C_3 = \frac{3.18}{f_1 R_{IN}'} = \frac{3.18}{200(17.6\text{k}\Omega)} = 0.9\mu\text{F}$$

$$9. \quad A_V = \frac{r_L}{R_{E_1} + r_{e'}}. \text{ If } R_{E_1} = 0 \text{ then:}$$

$$A_V = \frac{r_L}{r_{e'}} = \frac{3.05\text{k}\Omega}{18.5\Omega} = 164.9$$

10. The input resistance seen by the single source in a common base amplifier is:

$$R_{IN} = R_{E_2} \parallel (R_{E_1} + r_{e'})$$

If $R_{E_1} = 0$, $R_{IN} = R_{E_2} \parallel r_{e'}$, then:

$$R_{IN} = 2.215\text{k}\Omega \parallel 18.5\Omega \approx 18.5\Omega$$

This is a very small input resistance, and would excessively load most signal sources. For this reason, a common-emitter amplifier is usually preferred for high gain, single-stage amplifiers.

COMMON-COLLECTOR AMPLIFIERS

In a common-collector amplifier, the AC input signal is applied to the base terminal and the AC output signal is taken from the emitter terminal. With such an arrangement, you will find that the output voltage closely “follows” the input voltage. For this reason, a common-collector amplifier is referred to as an **emitter-follower**.

An emitter-follower circuit has characteristics that are quite different from those of the common-emitter and common-base circuits discussed previously. As you will see, a typical emitter-follower has a large value of R_{IN} , a small value of R_O , and a voltage gain close to unity. These characteristics make the emitter-follower useful for impedance matching and buffering applications.

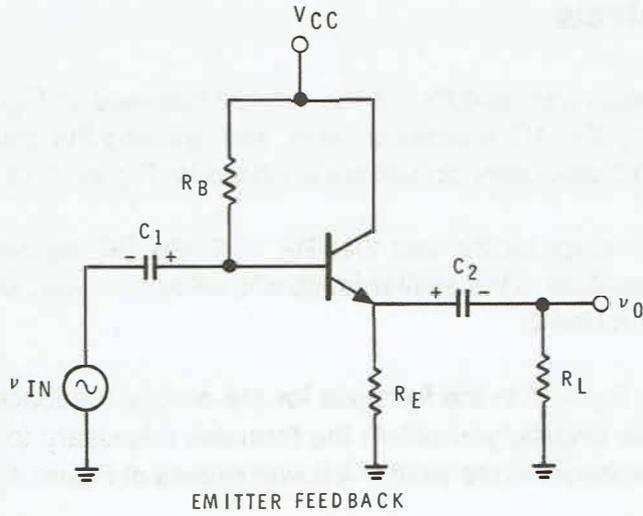
Emitter-Follower Circuits

You can convert a common-emitter amplifier to an emitter-follower as follows:

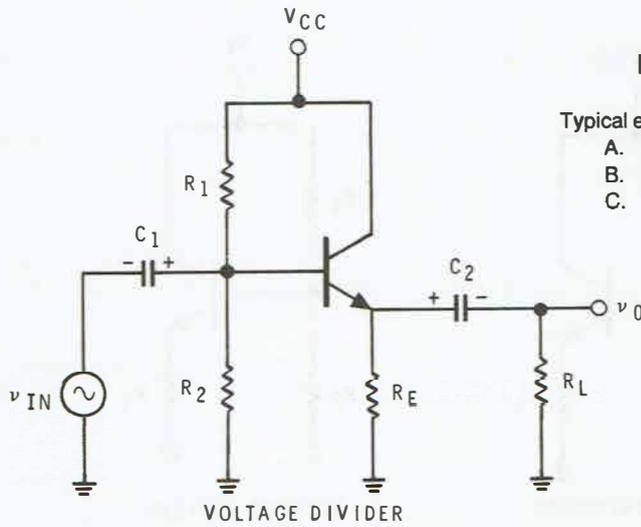
1. Set $R_C = 0$.
2. Remove the emitter bypass capacitor.
3. Take the output voltage from the emitter terminal rather than from the collector terminal.

By following these steps, you can easily obtain the circuits illustrated in Figure 4-12 from their common-emitter counterparts. These circuits represent the most frequently encountered emitter-follower amplifiers.

(A)



(B)



(C)

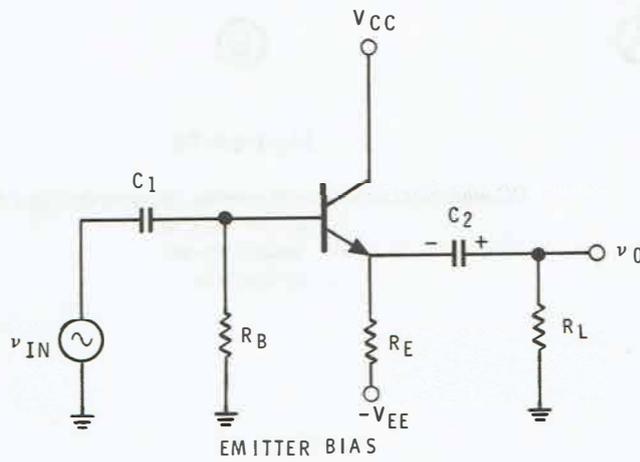


Figure 4-12

Typical emitter-follower circuits.

- A. Emitter feedback.
- B. Voltage divider.
- C. Emitter bias.

DC Analysis

The DC equivalent circuits for the emitter-followers in Figure 4-12 are obtained by reducing the AC sources to zero, and opening the coupling capacitors. The resulting DC equivalent circuits are illustrated in Figure 4-13.

Note that except for the fact that $R_C = 0$, the DC equivalent circuits in Figure 4-13 are identical to the emitter feedback, voltage divider, and emitter bias circuits discussed in Unit 2.

By setting $R_C = 0$ in the formulas for the emitter feedback, voltage divider, and emitter bias circuits, you obtain the formulas necessary to calculate the DC currents and voltages in the emitter-follower circuits of Figure 4-12.

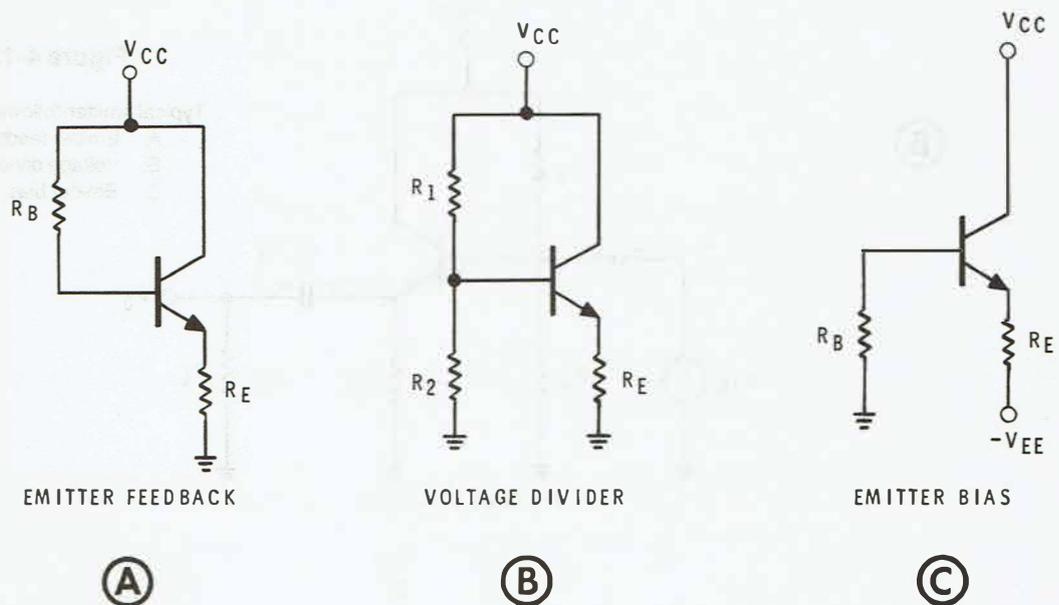


Figure 4-13

DC equivalent circuits for the emitter followers in Figure 4-12.

- A. Emitter feedback.
- B. Voltage divider.
- C. Emitter bias.

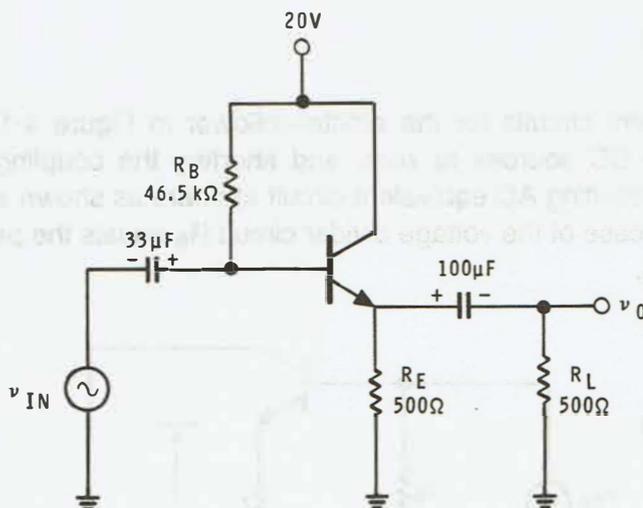


Figure 4-14

Circuit for Example 4-5.

Example 4-5

Calculate the values of I_{CQ} and V_{CEQ} for the circuit shown in Figure 4-14. Also, calculate the DC saturation current, and DC cutoff voltage. Assume the BJT in Figure 4-14 has an h_{FE} of 100.

Referring to the formulas for the emitter feedback circuit in the Biasing Summary Guide in Unit 2, you can proceed as follows:

$$I_C = \frac{V_{CC} - V_{BE}}{R_E + \frac{R_B}{\beta}} = \frac{20V - 0.7V}{500\Omega + \frac{46.5k\Omega}{100}} = 20mA = I_{CQ}$$

$$\begin{aligned} V_{CE} &= V_{CC} - I_C(R_C + R_E) \\ V_{CE} &= 20V - 20mA(0 + 500\Omega) \\ V_{CE} &= 10V = V_{CEQ} \end{aligned}$$

$$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E} = \frac{20V}{0 + 500\Omega} = 40mA$$

$$V_{CE(cut)} = V_{CC} = 20V$$

AC Analysis

The AC equivalent circuits for the emitter-follower in Figure 4-12 are obtained by reducing the DC sources to zero, and shorting the coupling capacitors. In each case, the resulting AC equivalent circuit appears as shown in Figure 4-15A. Naturally, in the case of the voltage divider circuit R_B equals the parallel combination of R_1 and R_2 .

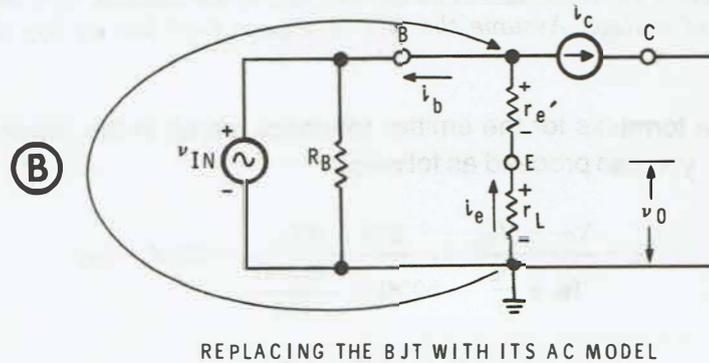
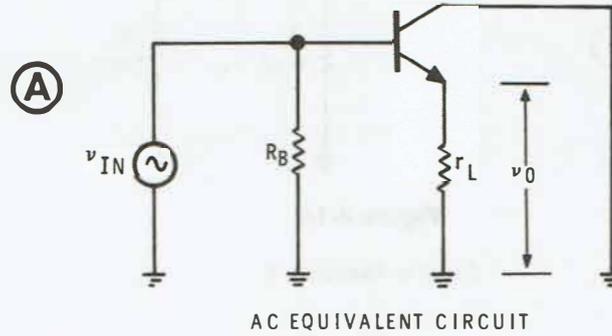


Figure 4-15

Emitter-follower AC equivalent circuits.

- A. AC equivalent circuit.
- B. Replacing the BJT with its AC model.

By replacing the BJT in Figure 4-15A with its AC model, you obtain the circuit shown in Figure 4-15B. Here, taking the indicated path, you can write the following loop equation:

$$-v_{IN} + i_e r_{e'} + i_e r_L = 0$$

Where:

$$r_L = R_E \parallel r_L$$

Solving for the AC emitter current, i_e , yields:

$$i_e = \frac{v_{IN}}{r_L + r_{e'}} \approx i_C \quad (\text{Eq. 4-17})$$

As before:

$$i_b = \frac{i_C}{\beta} = \frac{i_e}{h_{fe}}$$

In Figure 4-15B, note the direction of i_e is such that when v_{IN} is positive, v_O is also positive. Consequently, in an emitter-follower, the input and output voltages are in phase with each other.

Since $v_O = i_e r_L$ we have:

$$v_O = i_e r_L = \frac{v_{IN}}{r_L + r_{e'}} r_L$$

Solving for the ratio of v_O to v_{IN} yields:

$$A_V = \frac{v_O}{v_{IN}} = \frac{r_L}{r_L + r_{e'}} \quad (\text{Eq. 4-18})$$

Note that if $r_L \gg r_{e'}$, $A_V \approx 1$. Equation 4-18 indicates that the voltage gain of an emitter-follower can be close to 1, but it cannot exceed 1.

Since the output current is i_e , and the input current is i_b the current gain, A_i , is:

$$A_i = \frac{i_e}{i_b} \approx h_{fe}$$

Because the power gain is the product of the current gain and voltage gain:

$$A_p = A_i A_v = \frac{h_{fe} r_L}{r_L + r_{e'}} \quad (\text{Eq. 4-19})$$

The AC input resistance looking into the base equals the ratio of v_{IN} to i_b . Thus:

$$R_{IN(BASE)} = \frac{v_{IN}}{i_b} = \frac{v_{IN}}{\frac{i_C}{h_{fe}}} = \frac{h_{fe} v_{IN}}{i_C}$$

Since $i_C = \frac{v_{IN}}{r_L + r_{e'}}$ we have:

$$R_{IN(BASE)} = h_{fe}(r_L + r_{e'}) \quad (\text{Eq. 4-20})$$

From Figure 4-15, it should be clear that the input resistance seen by the signal source is:

$$R_{IN} = R_B || R_{IN(BASE)}$$

The output resistance of an emitter-follower depends on a complex relationship between numerous factors. Compared to common-emitter and common-base circuits, the output resistance of an emitter follower is quite low. By using the following formula, you can calculate a "ballpark figure" for the output resistance of the emitter followers in Figure 4-12.

$$R_O \approx [r_{e'} + \frac{R_B || R_S}{h_{fe}}] || R_E \quad (\text{Eq. 4-21})$$

Where R_S is the output resistance of the signal source driving the emitter follower.

A summary of the AC formulas for the emitter-follower circuits in Figure 4-12 is provided in Table 4-2.

Parameter	Approximate Formula
AC emitter current	$i_e = \frac{v_{IN}}{R_L + r_{e'}}$
AC collector current	$i_C \approx i_e$
AC base current	$i_b = \frac{i_C}{h_{fe}}$
Voltage gain	$A_V = \frac{r_L}{r_L + r_{e'}}$
Current gain	$A_i = h_{fe}$
Power gain	$A_p = \frac{h_{fe} r_L}{r_L + r_{e'}}$
Input resistance (base)	$R_{IN(BASE)} = h_{fe}(r_L + r_{e'})$
Input resistance (total)	$R_{IN} = R_B h_{fe}(r_L + r_{e'})$
Output resistance	$R_O \approx [r_{e'} + \frac{R_B R_S}{h_{fe}}] R_E$
<u>Comments</u>	
R_{IN} is large, R_O small, and $A_V \approx 1$.	
Applications include buffers and impedance matching.	
v_O and v_{IN} are in phase with each other.	

TABLE 4-2

Emitter-follower AC formula summary guide

Emitter-Follower AC Load Line

In the DC equivalent circuits of Figure 4-13, the resistance between the collector and emitter terminals equals R_E . Therefore, the DC load lines have a slope equal to $-1/R_E$.

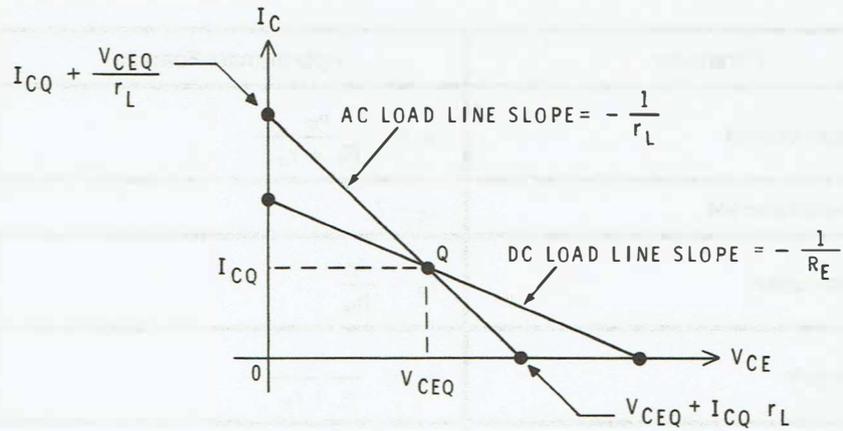


Figure 4-16

Emitter-follower load lines.

Similarly, in the AC equivalent circuit of Figure 4-15A the resistance between the collector and emitter terminals equals r_L . For this reason, the AC load line has a slope of $-1/r_L$, as shown in Figure 4-16.

By applying the general equation $y - y_1 = m(x - x_1)$ to Figure 4-16, you obtain:

$$I_C = I_{CQ} = \frac{-1}{r_L} (V_{CE} - V_{CEQ}) \quad (\text{Eq. 4-22})$$

The intercept values and clipping levels are obtained as before. In this case:

$$i_{C(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{r_L} \quad (\text{Eq. 4-23})$$

$$v_{CE(\text{cut})} = V_{CEQ} + I_{CQ}r_L \quad (\text{Eq. 4-24})$$

$$V^+ = I_{CQ}r_L \quad (\text{Eq. 4-25})$$

$$V^- = V_{CEQ} \quad (\text{Eq. 4-26})$$

Buffers and Impedance Matching

By carefully selecting component values, the voltage gain of an emitter follower will be almost unity. In addition, the output voltage will be in phase with the input voltage. Hence, the output voltage, in a well designed emitter follower, is almost identical to the input voltage.

The principle use of an emitter follower is as an **impedance matching device**. The following example serves to illustrate this concept.



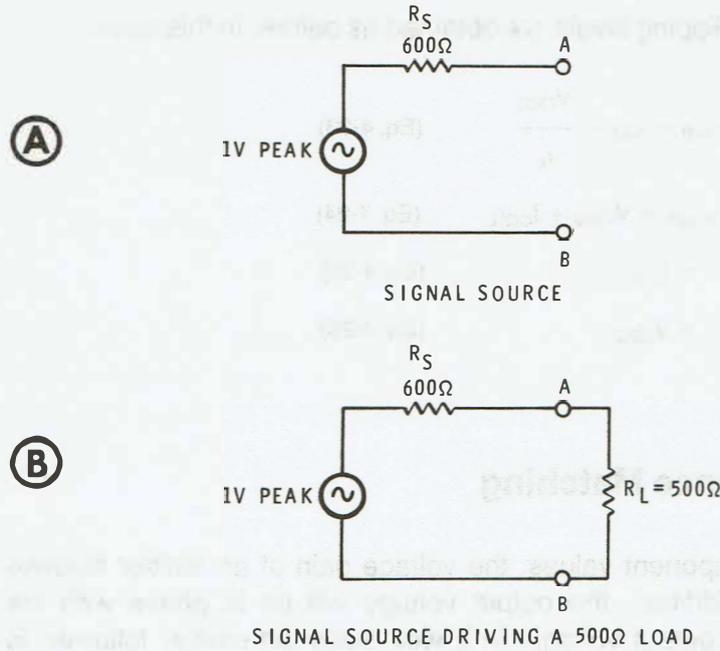
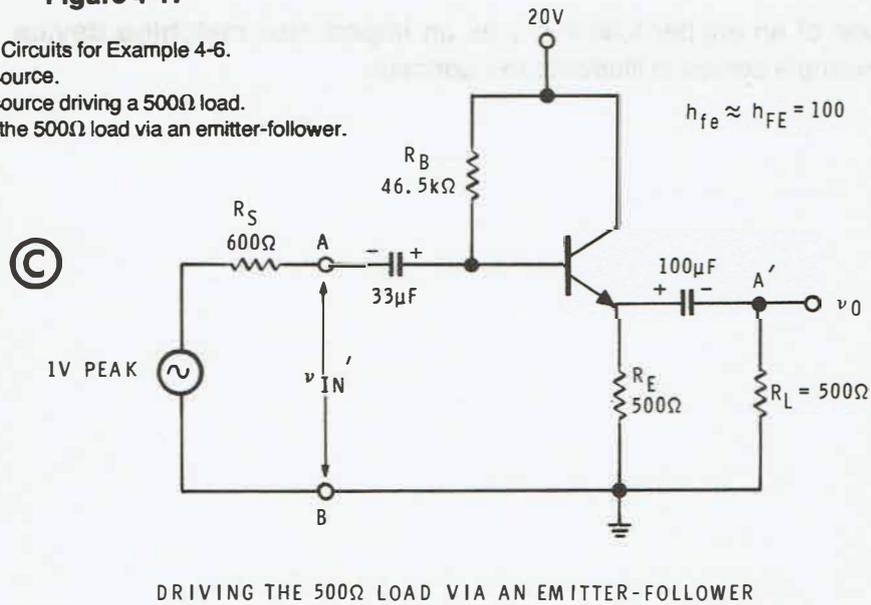


Figure 4-17

Circuits for Example 4-6.

- A. Signal source.
- B. Signal source driving a 500Ω load.
- C. Driving the 500Ω load via an emitter-follower.



Example 4-6

Figure 4-17A depicts a signal source whose output resistance, R_S , is 600Ω . Calculate the voltage developed across a 500Ω load assuming:

- (a) The signal source is connected directly to the 500Ω load as shown in Figure 4-17B.

(b) The signal source is connected to the 500Ω load through the emitter-follower circuit as shown in Figure 4-17C.

(a) Using voltage division, the output voltage is:

$$v_O = v_{AB} = \frac{1V(500\Omega)}{600\Omega + 500\Omega} = 0.454V \text{ peak}$$

In this case, only 45.4% of the signal voltage is developed across the 500Ω load. The remaining 54.6% is dropped across the 600Ω output resistance of the signal source. Since R_L is not large compared to R_S there is excessive loading of the signal source.

(b) The emitter follower in Figure 4-17C was partially analyzed in Example 4-5. Recall that:

$$I_{CQ} = 20\text{mA} \\ V_{CEQ} = 10\text{V}$$

Since the emitter follower is between the signal source and load, the effective load resistance seen by the signal source is the input resistance of the emitter follower. This concept is illustrated in Figure 4-18.

Since $I_{CQ} = 20\text{mA}$:

$$r_e' = \frac{37\text{mV}}{20\text{mA}} = 1.85\Omega$$

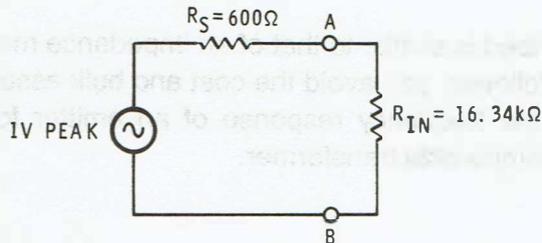


Figure 4-18

The effective load resistance seen by the signal source in Figure 4-17C equals the input resistance, R_{IN} , of the emitter-follower. Here,

$$R_{IN} = R_B || h_{ie}(r_L + r_e')$$

Also, since $R_B = 46.5\text{k}\Omega$, $h_{fe} = 100$ and $r_L = 250\Omega$, the value of R_{IN} is:

$$\begin{aligned} R_{IN} &= R_B \parallel h_{fe}(r_L + r_{e'}) \\ R_{IN} &= 46.5\text{k}\Omega \parallel 100(250\Omega + 1.85\Omega) \\ R_{IN} &= 46.5\text{k}\Omega \parallel 25.185\text{k}\Omega \\ R_{IN} &= 16.34\text{k}\Omega \end{aligned}$$

Clearly, since $R_{IN} \gg R_S$ there will be very little loading of the signal source. The portion of the 1V peak signal that is applied to the input terminals of the emitter follower is, by voltage division:

$$v_{IN}' = \frac{1\text{V}(16.34\text{k}\Omega)}{600\Omega + 16.34\text{k}\Omega} = 0.964\text{V peak}$$

v_{IN}' is the voltage "amplified" by the emitter follower. To predict the load voltage, you must calculate the voltage gain of the emitter follower. Here:

$$A_V = \frac{r_L}{r_L + r_{e'}} = \frac{250\Omega}{250\Omega + 1.85\Omega} = 0.993$$

Since $v_O = A_V v_{IN}'$, the voltage developed across the 500Ω load is:

$$v_O = A_V v_{IN}' = 0.993(0.964\text{V}) = 0.957\text{V peak}$$

In this example, the emitter follower functioned as an impedance matching device. Specifically, as far as the signal source was concerned, the emitter follower stepped up the relatively low, 500Ω , load resistance to approximately $16.34\text{k}\Omega$. Since the voltage gain of the emitter follower is almost 1, nearly all the source voltage was developed across the 500Ω load.

The action just described is similar to that of an impedance matching transformer. By using an emitter follower, you avoid the cost and bulk associated with a transformer. In addition, the frequency response of an emitter follower is generally superior to that of a comparable transformer.

Example 4-7

Sketch the Thevenin equivalent circuit, as viewed from the 500Ω load in Figure 4-17C. The equivalent circuit represents the "equivalent signal source" that drives the 500Ω load resistor.

Since the emitter follower in Figure 4-17C has a voltage gain close to 1, and a large value of R_{IN} compared to R_S , the Thevenin output voltage is approximately equal to v_{IN} , or 1V peak in this example.

The output resistance of the emitter-follower is the Thevenin resistance of the "equivalent signal source" driving the 500Ω load. Thus:

$$R_O = [r_{e'} + \frac{R_B \parallel R_S}{h_{fe}}] \parallel R_E$$

$$R_O = [1.85\Omega + \frac{46.5k\Omega \parallel 600\Omega}{100}] \parallel 500\Omega$$

$$R_O = 7.77\Omega \parallel 500\Omega = 7.65\Omega$$

The equivalent signal source seen by the 500Ω load applies as shown in Figure 4-19.

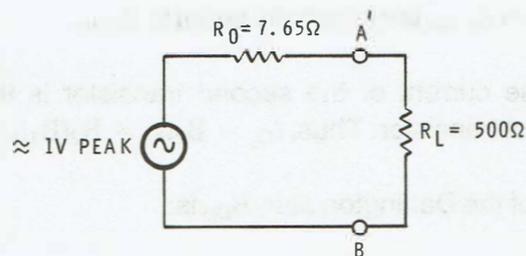


Figure 4-19

The equivalent signal source driving the 500Ω load in Figure 4-17C

Incidentally, a circuit used to isolate a low impedance load from a high impedance signal source is often referred to as a **buffer**. For this reason, emitter followers are also called buffers.

Darlington Pairs

Two transistors can be connected to form what is referred to as a **Darlington Pair**, as shown in Figure 4-20A. In this arrangement, note that the emitter current of the first transistor is the base current of the second transistor.

Darlington pairs can be formed with two discrete transistors as shown in Figure 4-20A. In addition, single-unit Darlington packages are available from most manufacturers. In any event, a given Darlington pair can be modeled as a single equivalent transistor, as shown in Figure 4-20B.

Starting with Figure 4-20A, the equivalent transistor model can be developed as follows.

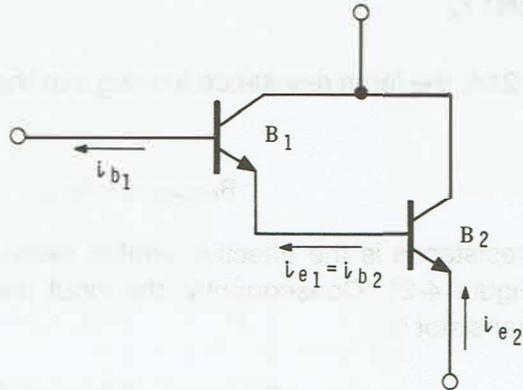
EQUIVALENT B

1. Assuming the AC base current of the first transistor is i_{b_1} , the collector current is $B_1 i_{b_1}$.
2. Since $i_e \approx i_c$, i_e is essentially equal to $B_1 i_{b_1}$.
3. The base current of the second transistor is the emitter current of the first transistor. Thus, $i_{b_2} = B_2 i_{b_1} = B_2 (B_1 i_{b_1}) = B_1 B_2 i_{b_1}$.

Ideally, the effective B of the Darlington pair, B_{Dp} is:

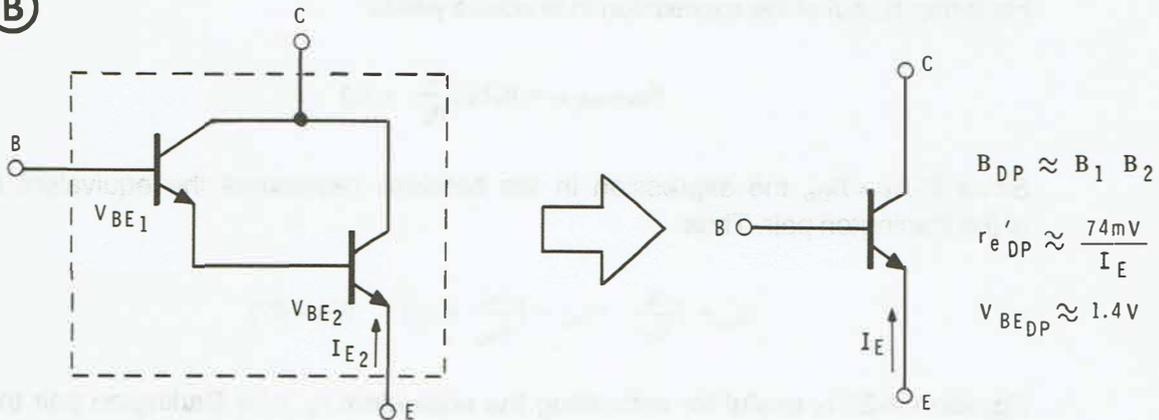
$$B_{Dp} = B_1 B_2 = h_{fe(Dp)} \quad (\text{Eq. 4-26})$$

A



CONNECTING TWO BJT'S IN A DARLINGTON PAIR

B



DARLINGTON PACKAGE AND APPROXIMATE EQUIVALENT

Figure 4-20

The Darlington pair configuration.

- A. Connecting two BJT's in a Darlington pair.
- B. Darlington package and Approximate equivalent.

EQUIVALENT $r_{e'}$

In Figure 4-21A, the input resistance looking into the base of the second transistor is:

$$R_{IN(BASE\ 2)} = B_2 r_{e'}$$

This input resistance is the effective emitter resistance of the first transistor, as shown in Figure 4-21. Consequently, the input resistance looking into the base of the first transistor is:

$$R_{IN(BASE\ 1)} = B_1 [r_{e'} + R_{E_1}]$$

$$R_{IN(BASE\ 1)} = B_1 [r_{e'} + B_2 r_{e_2}]$$

Factoring B_2 out of the expression in brackets yields:

$$R_{IN(BASE\ 1)} = B_1 B_2 \left[\frac{r_{e'}}{B_2} + r_{e_2} \right]$$

Since $B_1 B_2 = B_{DP}$ the expression in the brackets represents the equivalent $r_{e'}$ of the Darlington pair. Thus:

$$r_{e_{op}} = \left[\frac{r_{e'}}{B_2} + r_{e_2} \right] = \left[\frac{r_{e'}}{h_{FE_2}} + r_{e_2} \right] \quad (\text{Eq. 4-27})$$

Equation 4-27 is useful for estimating the equivalent $r_{e'}$ of a Darlington pair that uses two discrete BJT's. This expression can be further simplified. Look at the following.

$$\text{Clearly, } r_{e_1} = \frac{37\text{mV}}{I_{E_1}} \text{ and } r_{e_2} = \frac{37\text{mV}}{I_{E_2}}.$$

In a Darlington pair, I_{E_1} is I_{B_2} . Therefore:

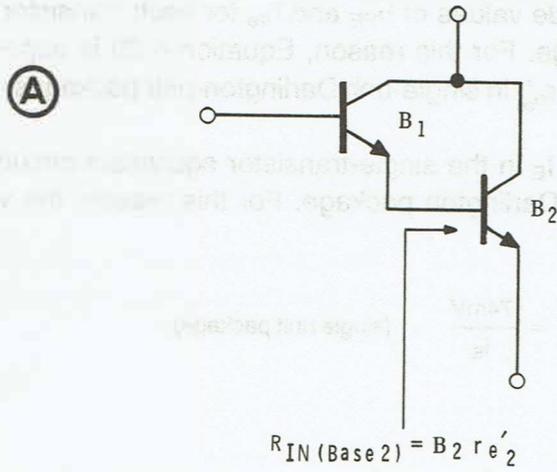
$$I_{E_2} = h_{FE_2} I_{B_2} = h_{FE_2} I_{E_1}$$

Solving for I_{E_1} , gives us:

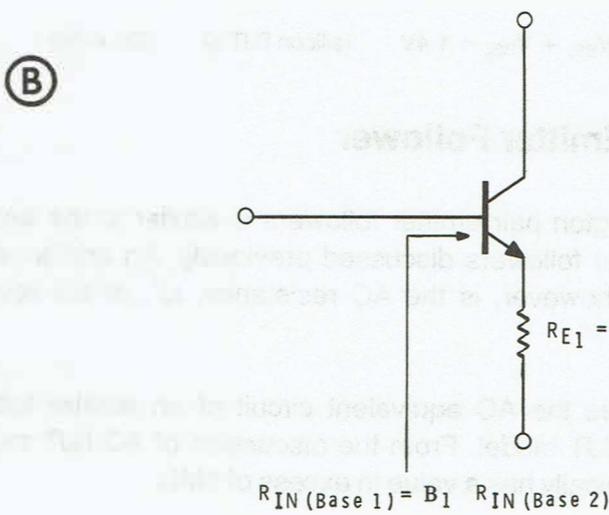
$$I_{E_1} = \frac{I_{E_2}}{h_{FE_2}}$$

Now:

$$r_{e_1} = \frac{37\text{mV}}{I_{E_1}} = \frac{37\text{mV}}{\frac{I_{E_2}}{h_{FE_2}}} = \frac{h_{FE_2} 37\text{mV}}{I_{E_2}} = h_{FE_2} r_{e_2}$$



INPUT RESISTANCE LOOKING INTO BASE 2



INPUT RESISTANCE LOOKING INTO BASE

Figure 4-21

- Darlington input resistances.
- A. Input resistance looking into base 2.
 - B. Input resistance looking into base 1.

Substituting $h_{FE_2} r_{e'_2}$ for $r_{e'_1}$ into Equation 4-27 yields:

$$r_{e'_{op}} = \frac{h_{FE_2} r_{e'_2}}{h_{fe_2}} + r_{e'_2} \quad (\text{Eq. 4-28})$$

Assuming the DC beta, h_{FE_2} , is essentially equal to the AC beta, h_{fe_2} , the previous relationship reduces to:

$$r_{e'_{op}} = 2r_{e'_2} = \frac{74\text{mV}}{I_{E_2}} \quad (\text{Eq. 4-29})$$

Manufacturers rarely provide values of h_{FE} and h_{fe} for each transistor in a single-unit Darlington-pair package. For this reason, Equation 4-29 is especially useful for estimating the values of $r_{e'_{dp}}$ in single-unit Darlington-pair packages.

In Figure 4-20B, note that I_E in the single-transistor equivalent circuit equals the value of I_{E_2} in the original Darlington package. For this reason, the value of $r_{e'_{dp}}$ in a single-unit package, is:

$$r_{e'} = \frac{74\text{mV}}{I_E} \quad (\text{single unit package})$$

EQUIVALENT V_{BE}

Since a Darlington pair uses two transistors, connected as shown in Figure 4-20A, it is obvious that the effective V_{BE} is:

$$V_{BE_{dp}} = V_{BE_1} + V_{BE_2} = 1.4\text{V} \quad (\text{silicon BJT's}) \quad (\text{Eq. 4-30})$$

Darlington Pair Emitter Follower

The analysis of Darlington pair emitter followers is similar to the analysis of the single-transistor emitter followers discussed previously. An additional factor that must be considered, however, is the AC resistance, r_c' , of the reverse biased collector-base diode.

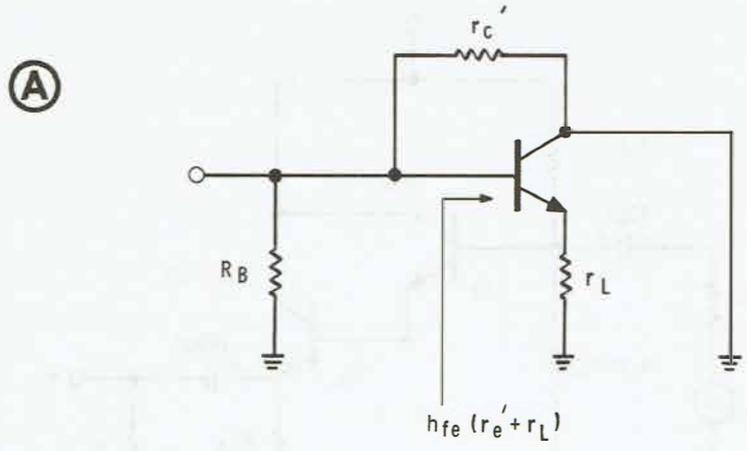
Figure 4-22A illustrates the AC equivalent circuit of an emitter follower, when r_c' is included in the BJT model. From the discussion of AC BJT models in Unit 3, you know that r_c' typically has a value in excess of $1\text{M}\Omega$.

By redrawing the circuit in Figure 4-22A, you obtain the circuit shown in Figure 4-22B. Here, it is apparent that r_c' is in parallel with R_B , and the input resistance looking into the base, $h_{fe}(r_{e'} + r_L)$. Thus, the input resistance of the circuit is:

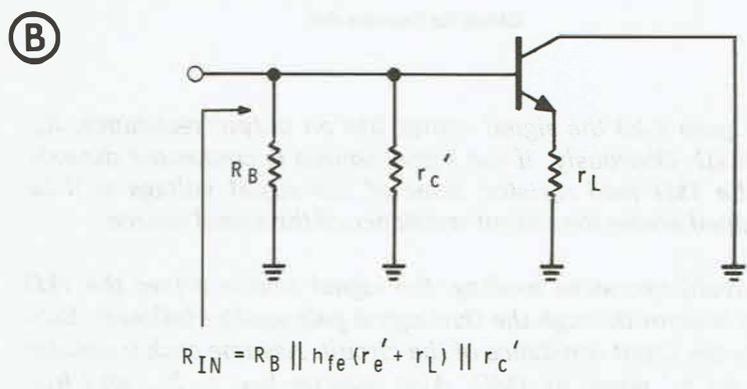
$$R_{IN} = R_B \| h_{fe}(r_{e'} + r_L) \| r_c' \quad (\text{Eq. 4-31})$$

In a single-transistor emitter follower, the $h_{fe}(r_{e'} + r_L)$ product is small compared to the value of r_c' . In this case, Equation 4-31 is closely approximated by:

$$R_{IN} = R_B \| h_{fe}(r_{e'} + r_L)$$



EMITTER-FOLLOWER AC EQUIVALENT CIRCUIT THAT INCLUDES r_c'



REDRAWING THE CIRCUIT

Figure 4-22

Emitter-follower AC equivalent circuits that illustrate the effect r_c' has on the circuit's input resistance.

- A. Emitter-follower AC equivalent circuit that includes r_c' .
- B. Redrawing the circuit.

This is the reason why r_c' is usually neglected in single-transistor emitter followers.

In Darlington pair emitter followers, r_c' cannot be neglected. The following example illustrates how to analyze a Darlington pair emitter follower.

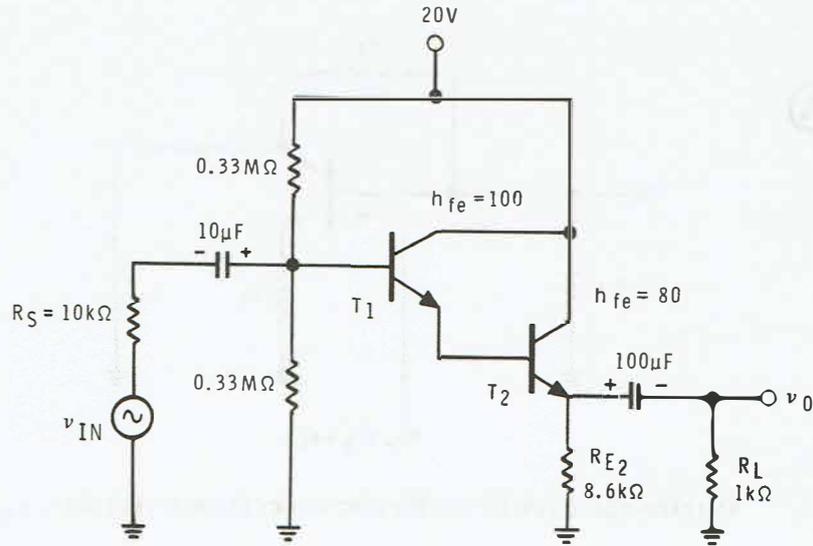


Figure 4-23

Circuit for Example 4-8.

Example 4-8

In Figure 4-23 the signal source has an output resistance, R_S , of $10\text{k}\Omega$. Obviously, if the signal source is connected directly to the $1\text{k}\Omega$ load resistor, most of the signal voltage will be dropped across the output resistance of the signal source.

To avoid excessive loading, the signal source drives the $1\text{k}\Omega$ load resistor through the Darlington pair emitter follower. Estimate the input resistance of the circuit. Assume each transistor has an r_C' equal to $5\text{M}\Omega$. Also assume $h_{FE_1} \approx h_{fe_1}$ and $h_{FE_2} \approx h_{fe_2}$.

The base voltage of the first transistor, T_1 , is, using voltage division:

$$V_{B_1} = \frac{20\text{V}(0.33\text{M}\Omega)}{0.33\text{M}\Omega + 0.33\text{M}\Omega} = 10\text{V}$$

Thus, the emitter voltage of T_1 is:

$$\begin{aligned} V_{E_1} &= V_{B_1} - V_{BE} \\ V_{E_1} &= 10\text{V} - 0.7\text{V} = 9.3\text{V} \end{aligned}$$

In a Darlington pair, $V_{E_1} = V_{B_2}$. Thus:

$$\begin{aligned} V_{E_2} &= V_{B_2} - V_{BE} \\ V_{E_2} &= 9.3\text{V} - 0.7\text{V} = 8.6\text{V} \end{aligned}$$

Since $V_{E_2} = 8.6\text{V}$ and $R_{E_2} = 8.6\text{k}\Omega$ the emitter current I_{E_2} is:

$$I_{E_2} = \frac{V_{E_2}}{R_{E_2}} = \frac{8.6\text{V}}{8.6\text{k}\Omega} = 1\text{mA}$$

And $r_{e_2}' = \frac{37\text{mV}}{I_{E_2}}$, $r_{e_2}' = \frac{37\text{mV}}{1\text{mA}} = 37\Omega$

The AC load resistance, r_L is:

$$r_L = R_{E_2} \parallel R_L$$

$$r_L = 8.6\text{k}\Omega \parallel 1\text{k}\Omega = 896\Omega$$

Therefore, the input resistance looking into the base of transistor T_1 is:

$$R_{\text{IN(BASE 2)}} = h_{fe_2}(r_{e_2}' + r_L) \parallel r_{C_2}'$$

$$R_{\text{IN(BASE 2)}} = 80(37\Omega + 896\Omega) \parallel 5\text{M}\Omega$$

$$R_{\text{IN(BASE 2)}} = 74.64\text{k}\Omega \parallel 5\text{M}\Omega \approx 74.64\text{k}\Omega$$

Note that since $h_{fe_2}(r_{e_2}' + r_L) \ll r_{C_2}'$, the parallel combination of $h_{fe_2}(r_{e_2}' + r_L)$ and r_{C_2}' essentially equals $h_{fe_2}(r_{e_2}' + r_L)$. You will find that in most Darlington pair emitter followers, r_{C_2}' can be neglected.

$R_{\text{IN(BASE 2)}}$ is the **effective emitter resistance**, R_{E_1} , of the first transistor, T_1 . For this reason, the input resistance looking into the base of T_1 is:

$$R_{\text{IN(BASE 1)}} = h_{fe_1}(r_{e_1}' + R_{E_1}) \parallel r_{C_1}'$$

Since $I_{E_2} = 1\text{mA}$ and $h_{FE_2} \approx 80$, I_{B_2} equals $1\text{mA}/80$ or $12.5\mu\text{A}$. Thus:

$$I_{B_2} = I_{E_1} = 12.5\mu\text{A}$$

$$r_{e_1}' = \frac{37\text{mV}}{I_{E_1}} = \frac{37\text{mV}}{12.5\mu\text{A}} = 2.96\text{k}\Omega$$

Therefore, the input resistance looking into the base of T_1 is:

$$R_{\text{IN(BASE 1)}} = h_{fe_1}(r_{e_1}' + R_{E_1}) \parallel r_{C_1}'$$

$$R_{\text{IN(BASE 1)}} = 100(2.96\text{k}\Omega + 74.64\text{k}\Omega) \parallel 5\text{M}\Omega$$

$$R_{\text{IN(BASE 1)}} = 7.76\text{M}\Omega \parallel 5\text{M}\Omega$$

$$R_{\text{IN(BASE 1)}} = 3.04\text{M}\Omega$$

Note that since $h_{fe_1}(r_{e_1}' + R_{E_1})$ is not small compared to r_{C_1}' , you should not neglect r_{C_1}' .

The input resistance of the Darlington pair circuit can now be calculated in this manner:

$$\begin{aligned} R_{IN} &= R_B \parallel R_{IN(\text{BASE } 1)} \\ R_{IN} &= 0.33\text{M}\Omega \parallel 0.33\text{M}\Omega \parallel 3.04\text{M}\Omega \\ R_{IN} &= 0.165\text{M}\Omega \parallel 3.04\text{M}\Omega \\ R_{IN} &= 156.5\text{k}\Omega \end{aligned}$$

Example 4-9

Example 4-8 illustrated how to analyze a Darlington pair emitter follower constructed from two discrete transistors. Rework Example 4-8 by doing the following:

1. Convert the Darlington package in Figure 4-23 to an equivalent transistor.
 2. Sketch, and solve, the single-transistor equivalent circuit for R_{IN} .
1. To convert the Darlington pair in Figure 4-23 to an equivalent transistor, you can proceed as follows:

$$\beta_{DP} = h_{fe_{DP}} = h_{fe_1} h_{fe_2} = 100(80) = 8000$$

$$V_{BE_{DP}} = 1.4\text{V}$$

Example 4-8 indicated that r_{C_2}' is usually negligible. Hence, the effective value of $r_{C_{DP}}'$ essentially equals the value of r_{C_1}' . Thus:

$$r_{C_{DP}}' \approx r_{C_1}' = 5\text{M}\Omega$$

2. The single-transistor equivalent is illustrated in Figure 4-24. Here, R_{IN} is calculated in this way:

$$V_B = \frac{20\text{V}(0.33\text{M}\Omega)}{0.33\text{M}\Omega + 0.33\text{M}\Omega} = 10\text{V}$$

$$\begin{aligned} V_E &= V_B - V_{BE} \\ V_E &= 10\text{V} - 1.4\text{V} = 8.6\text{V} \end{aligned}$$

$$I_E = \frac{V_E}{R_E} = \frac{8.6\text{V}}{8.6\text{k}\Omega} = 1\text{mA}$$

$$r_{e_{DP}}' = \frac{74\text{mV}}{I_E} = 74\Omega$$

$$r_L = R_E \parallel R_L = 8.6\text{k}\Omega \parallel 1\text{k}\Omega = 896\Omega$$

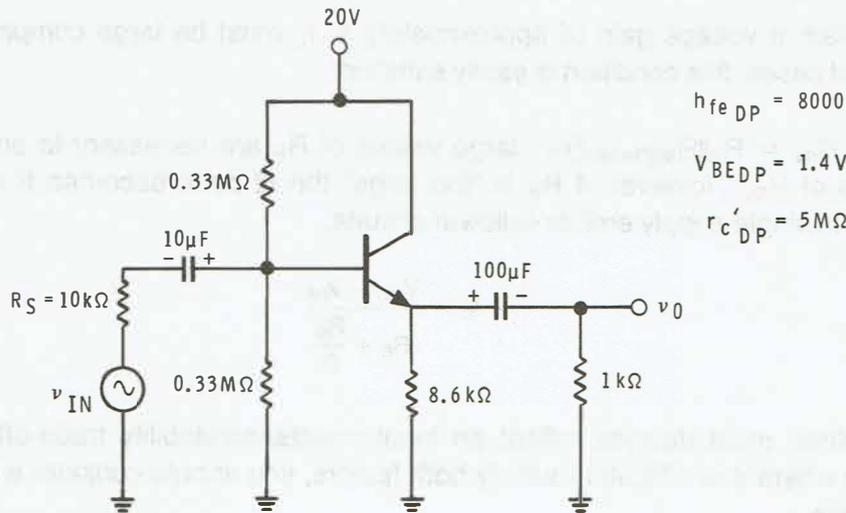


Figure 4-24

Single transistor equivalent circuit for Figure 4-23.

The input resistance looking into the base is therefore:

$$\begin{aligned} R_{IN(BASE)} &= h_{fe_{DP}}(r_{e_{DP}}' + r_L) \parallel r_{c_{DP}}' \\ R_{IN(BASE)} &= 8000(74\Omega + 896\Omega) \parallel 5M\Omega = 3.04M\Omega \end{aligned}$$

Now the input resistance of the circuit is:

$$\begin{aligned} R_{IN} &= R_B \parallel R_{IN(BASE)} \\ R_{IN} &= 0.33M\Omega \parallel 0.33M\Omega \parallel 3.04M\Omega = 156.5k\Omega \end{aligned}$$

Comparing Example 4-8 with Example 4-9, you can see that the equivalent transistor approach requires fewer calculations. For this reason, the equivalent transistor approach is the preferred method.

Design Consideration

Generally speaking, when you design an emitter follower, you must make trade-offs relative to the following factors:

1. Obtaining a near unity voltage gain.
2. Obtaining a large value of R_{IN} .
3. Obtaining a Q point near the center of the AC load line.
4. Obtaining a stable Q point.

To obtain a voltage gain of approximately 1, r_L must be large compared to r_e' . In most cases, this condition is easily satisfied.

Since $R_{IN} = R_B \parallel R_{IN(BASE)} \parallel r_C'$, large values of R_B are necessary to ensure large values of R_{IN} . However, if R_B is "too large" the Q point becomes B dependent since, in single-supply emitter-follower circuits:

$$I_C = \frac{V_{CC} - V_{BE}}{R_E + \frac{R_B}{\beta}}$$

Therefore, most designs reflect an input resistance/stability trade-off. In those cases where it is difficult to satisfy both factors, you should consider a Darlington package.

Centered Q Point

In single-supply emitter-follower circuits the DC collector-to-emitter voltage, V_{CEQ} , is:

$$V_{CEQ} = V_{CC} - I_{CQ}R_E$$

The AC load line indicates that the Q point will be centered when:

$$V_{CEQ} = I_{CQ}r_L$$

Equating the two expressions, and solving for I_{CQ} yields:

$$I_{CQ} = \frac{V_{CC}}{R_E + r_L} \quad (\text{Eq. 4-32})$$

Equation 4-32 indicates the value of I_{CQ} required to locate the Q point near the center of the AC load line.

Design Procedure

Based on Equation 4-32, you can use the following procedure to design elementary emitter-follower, single-supply, circuits.

1. Select R_E . As a guide, R_E is chosen to be 1 to 5 times larger than R_L .
2. Calculate r_L . Since $R_E = 1$ to 5 times R_L , the value of r_L will be between 83% and 91% of R_L . By making r_L as large as possible, you obtain the largest possible value of $R_{IN(BASE)}$.
3. Calculate I_{CQ} . By using Equation 4-32, you can determine the value of I_{CQ} required to produce a Q point near the center of the AC load line.
4. Calculate the values of the biasing resistors required to produce the value of I_{CQ} calculated in step 3.
5. Calculate the required capacitor values.

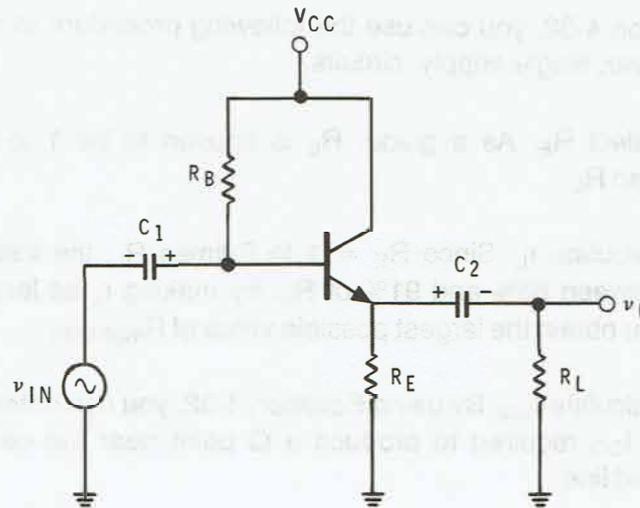
Once steps 1 through 5 have been implemented, you should evaluate the resulting circuit to make sure the voltage gain, input resistance, signal swing, etc. satisfy your specifications.

Design Guide

The following design guide uses the procedure just described for single-supply emitter-follower circuits. In addition, a similar procedure is provided for the emitter bias circuit. In this case, it is assumed that the designer has the freedom to specify values for the supply voltages.

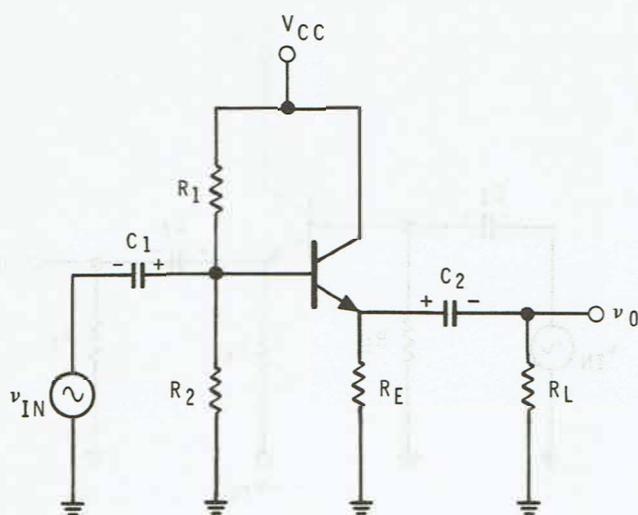
To design Darlington emitter followers, you must use, where appropriate, $r_{e_{dp}}'$, B_{Dp} , and $V_{BE_{Dp}}$. Also, remember to include r_C' in your calculations for R_{IN} .

EMITTER-FOLLOWER DESIGN GUIDE



EMITTER FEEDBACK

1. Select R_E . $R_E = 1 \text{ to } 5 \text{ times } R_L$
2. Calculate r_L . $r_L = \frac{R_E R_L}{R_E + R_L}$
3. Calculate I_{CQ} . $I_{CQ} = \frac{V_{CC}}{R_E + r_L}$
4. Calculate V_{EQ} . $V_{EQ} = I_{CQ} R_E$
5. Calculate V_{CEQ} . $V_{CEQ} = V_{CC} - V_{EQ}$
6. Calculate R_B . $R_B = \frac{V_{CC} - [V_{BE} + V_{EQ}]}{I_{BQ}}$
7. Select capacitors. $C_1 \geq \frac{3.18}{f_1 R_{IN}}$
 $C_2 \geq \frac{3.18}{f_1 R_L}$



VOLTAGE DIVIDER

1. Select R_E .

$$R_E = 1 \text{ to } 5 \text{ times } R_L$$

2. Calculate r_L .

$$r_L = \frac{R_E R_L}{R_E + R_L}$$

3. Calculate I_{CQ} .

$$I_{CQ} = \frac{V_{CC}}{R_E + r_L}$$

4. Calculate V_{EQ} .

$$V_{EQ} = I_{CQ} R_E$$

5. Calculate V_{CEQ} .

$$V_{CEQ} = V_{CC} - V_{EQ}$$

6. Select R_2 .

$$R_2 \approx 10R_E$$

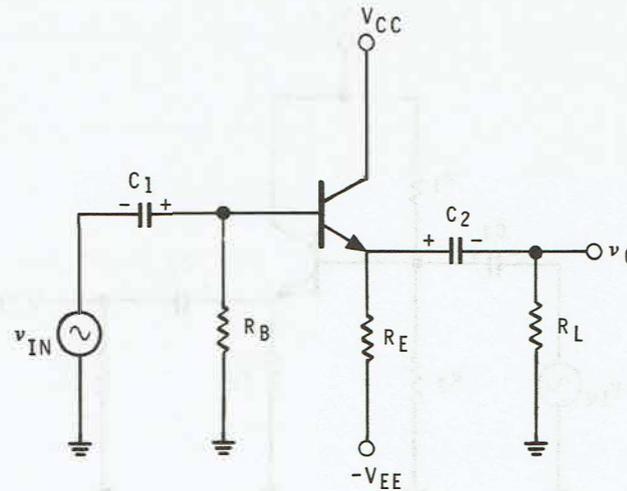
7. Calculate R_1 .

$$R_1 = \frac{R_2(V_{CC} - V_{BEQ})}{V_{BEQ}}$$

8. Select capacitors.

$$C_1 \geq \frac{3.18}{f_1 R_{IN}}$$

$$C_2 \geq \frac{3.18}{f_1 R_L}$$



EMITTER BIAS

1. Select V_{CC} .
2. Select R_E .
3. Calculate r_L .
4. Calculate I_{CQ} .
5. Calculate V_{EE} .
6. Select R_B .
7. Select capacitors.

$V_{CC} \approx$ desired clipping level.

$R_E = 1$ to 5 times R_L

$$r_L = \frac{R_E R_L}{R_E + R_L}$$

$$I_{CQ} = \frac{V_{CC} + 0.7V}{r_L}$$

$$V_{EE} = I_{CQ} R_E + 0.7V$$

$$R_B \approx 10R_E$$

$$C_1 \geq \frac{3.18}{f_1 R_{IN}}$$

$$C_2 \geq \frac{3.18}{f_1 R_L}$$

Example 4-10

Design an emitter follower according to the following specifications:

1. $V_{CC} = 12V$
2. $h_{fe} \approx h_{FE} = 100$
3. Use a voltage divider circuit.
4. $f_1 = 100Hz$

The following steps correspond to the steps in the design guide for the voltage divider circuit.

1. Select $R_E = R_L = 100\Omega$
2. $r_L = R_E \parallel R_L = 100\Omega \parallel 100\Omega = 50\Omega$
3. $I_{CQ} = \frac{V_{CC}}{R_E + r_L} = \frac{12V}{100\Omega + 50\Omega} = 8mA$
4. $V_{EQ} = I_{CQ}R_E = 80mA(100\Omega) = 8V$
5. $V_{CEQ} = V_{CC} - V_{EQ} = 12V - 8V = 4V$
6. $R_2 = 10R_E = 1k\Omega$
7. $R_1 = \frac{R_2(V_{CC} - V_{BQ})}{V_{BQ}}$

Since $V_{EQ} = 8V$, $V_{BQ} = 8V + 0.7V$ or $8.7V$

$$R_1 = \frac{1k\Omega(12V - 8.7V)}{8.7V} = 379\Omega$$

8. To calculate C_1 , you must first calculate R_{IN} . Since $I_{CQ} = 80\text{mA} \approx I_E$ we have:

$$r_c' = \frac{37\text{mV}}{I_E} = \frac{37\text{mV}}{80\text{mA}} = 0.463\Omega$$

$$R_{IN(\text{BASE})} = h_{fe}(r_c' + r_L)$$

$$R_{IN(\text{BASE})} = 100(0.463\Omega + 50\Omega) = 5046.3\Omega \approx 5.05\text{k}\Omega$$

$$R_B = R_1 \parallel R_2 = 379\Omega \parallel 1\text{k}\Omega = 275\Omega$$

$$R_{IN} = R_B \parallel R_{IN(\text{BASE})}$$

$$R_{IN} = 275\Omega \parallel 5.05\text{k}\Omega$$

$$R_{IN} = 261\Omega$$

Thus, the minimum capacitor values are:

$$C_1 = \frac{3.18}{f_1 R_{IN}} = \frac{3.18}{100(261\Omega)} = 121.8\mu\text{F}$$

$$C_2 = \frac{3.18}{f_1 R_L} = \frac{3.18}{100(100\Omega)} = 318\mu\text{F}$$

Example 4-11

The emitter follower designed in Example 4-10 effectively "stepped up" the load resistance, as seen from the signal source, from 100Ω to 261Ω .

If the signal source has an output resistance of 600Ω , a typical value, the 2.61:1 increase in the effective value of R_L is not sufficient to prevent significant loading of the signal source.

For this reason, the circuit is to be redesigned using a Darlington pair configuration. Assume that two transistors like the one used in Example 4-10 are available for the design. Also assume r_c' for each transistor is $5M\Omega$.

First estimate the equivalent parameters for the Darlington package:

$$B_{DP} = B_1 B_2 = 100(100) = 10\,000$$

In practice, the actual value of B_{DP} , when the Darlington package is composed of two discrete transistors, will be less than the B_1B_2 product.

For this reason, we will **derate** the calculated value of B_{DP} by 40%. Thus:

$$B_{DP} = 0.6 B_1 B_2$$

$$B_{DP} = 0.6(10\ 000) = 6\ 000$$

$$V_{BE_{DP}} = 1.4V$$

$$r'_{C_{DP}} = r_{C_1} = 5M\Omega$$

The first five steps in the design process are the same as in Example 4-10. We will simply note the results.

1. $R_E = 100\Omega$
2. $r_L = 50\Omega$
3. $I_{CQ} = 80mA$
4. $V_{EQ} = 8V$
5. $V_{CEQ} = 4V$
6. In a Darlington package, the equivalent values of h_{fe} and h_{FE} are very large. For this reason, $R_{IN(BASE)}$ is also quite large. Because of this, larger values of R_1 and R_2 can be used without loading the voltage divider.

With a single transistor, R_2 is usually chosen so that $R_2 \leq 10R_E$. As a guide, you can select $R_2 = 100R_E$ if a Darlington arrangement is used. Thus:

$$R_2 = 100R_E = 100(100\Omega) = 10k\Omega$$

$$7. R_1 = \frac{R_2(V_{CC} - V_{BQ})}{V_{BQ}}$$

Since $V_{EQ} = 8V$ and the equivalent value of V_{BE} is 1.4V, $V_{BQ} = 8V + 1.4V$ or 9.4V. Thus:

$$R_1 = \frac{10k\Omega(12V - 9.4V)}{9.4V} = 2.76k\Omega$$

8. First estimate $R_{IN(BASE)}$:

$$R_{IN(BASE)} = h_{ie_{op}}(r_{c_{op}}' + r_L) \parallel r_{c_{op}}'$$

Since $I_E = 8\text{mA}$:

$$r_{c_{op}}' = \frac{74\text{mV}}{I_E} = \frac{74\text{mV}}{80\text{mA}} = 0.925\Omega$$

Thus:

$$R_{IN(BASE)} = 6000(0.925\Omega + 50\Omega) \parallel 5\text{M}\Omega$$

$$R_{IN(BASE)} = 305.5\text{k}\Omega \parallel 5\text{M}\Omega = 288\text{k}\Omega$$

R_{IN} equals $R_B \parallel R_{IN(BASE)}$. Therefore:

$$R_{IN} = 2.16\text{k}\Omega \parallel 288\text{k}\Omega = 2.14\text{k}\Omega$$

The minimum capacitor values are therefore:

$$C_1 = \frac{3.18}{f_1 R_{IN}} = \frac{3.18}{100(2.14\text{k}\Omega)} = 14.85\mu\text{F}$$

$$C_2 = \frac{3.18}{f_1 R_L} = \frac{3.18}{100(100\Omega)} = 318\mu\text{F}$$

In Example 4-11, note that the load resistance, as seen from the signal source, has been stepped up from 100Ω to $2.14\text{k}\Omega$.

If a larger value of R_{IN} is required, you can increase the values of R_1 and R_2 , while maintaining the same ratio. For example, if $R_1 = 27.6\text{k}\Omega$ and $R_2 = 100\text{k}\Omega$, R_{IN} is approximately $20.1\text{k}\Omega$.

Increasing the values of R_1 and R_2 increases the input resistance. However, at some point, the effective DC resistance between the base of the transistor and ground, $h_{FE}R_E$, begins to load the voltage divider. When this occurs, V_B is reduced. In this case, V_E and I_{CQ} will also decrease. For this reason, the Q point moves closer to the cutoff region. Thus the values selected for R_1 and R_2 represent a high input resistance/centered Q point trade-off.

Self-Test Review

Refer to Figure 4-25 for questions 11 through 18.

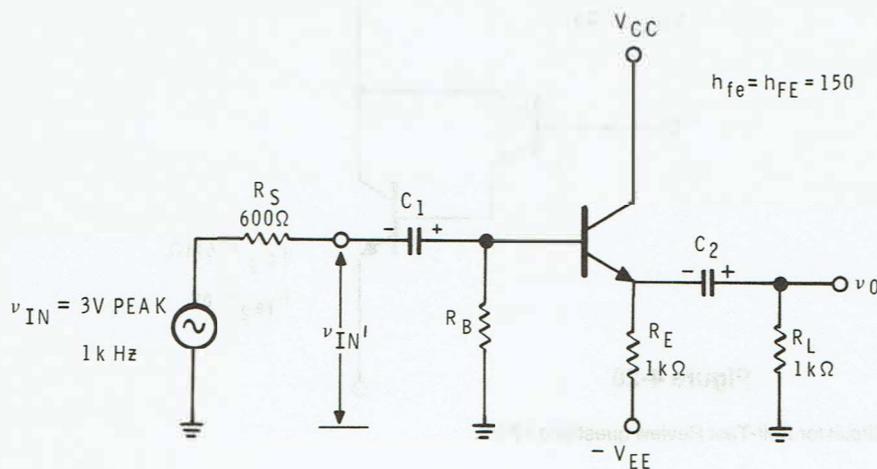


Figure 4-25

Circuit for Self-Test Review questions 11-18.

11. The circuit in Figure 4-25 is to be designed so that the clipping level is approximately 6V. A reasonable value for V_{CC} is therefore _____V.
12. Component values should be chosen so that I_{CQ} is approximately _____mA.
13. V_{EE} should be approximately _____V.
14. The input resistance seen by the 600Ω signal source is _____k Ω .
15. Assuming $v_{IN} = 3V$ peak, v_{IN}' is about _____V peak.
16. Assuming $v_{IN} = 3V$ peak, v_O is about _____V peak.
17. C_1 should be larger than approximately _____ μ F.
18. C_2 should be larger than approximately _____ μ F.

Refer to Figure 4-26 for questions 19 through 22.

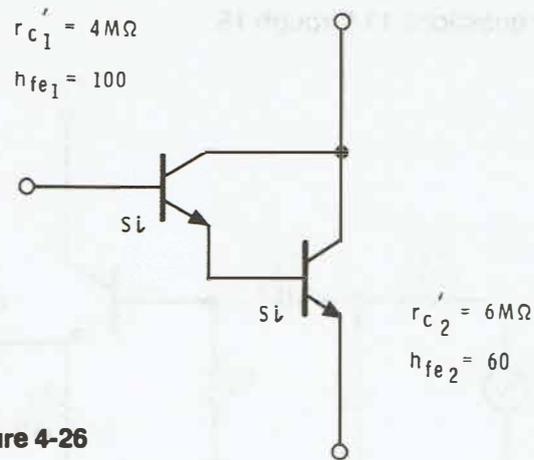


Figure 4-26

Circuit for Self-Test Review questions 19-22.

19. $h_{fe_{Dp}}$ ideally equals _____.
20. For purposes of design, a reasonable value to assume for $h_{fe_{Dp}}$ is _____.
21. $r_{C_{Dp}}'$ is approximately _____ $M\Omega$.
22. $V_{BE_{Dp}}$ is approximately _____ V.

Answers

- | | |
|-------------------|-----------------|
| 11. 6V | 17. $0.36\mu F$ |
| 12. 13.4mA | 18. $3.18\mu F$ |
| 13. -14.1V | 19. 6000 |
| 14. $8.83k\Omega$ | 20. 3600 |
| 15. 2.81V peak | 21. $4M\Omega$ |
| 16. 2.79V peak | 22. 1.4V |

The solution to questions 11 through 22 follow.

11. In an emitter bias circuit, V_{CC} should be approximately equal to the desired clipping level. Therefore, V_{CC} should equal approximately 6V.

12. In an emitter bias circuit, $I_{CQ} = \frac{V_{CC} + 0.7V}{r_L}$

$$r_L = R_E \parallel R_L = 1k\Omega \parallel 1k\Omega = 500\Omega$$

Thus:

$$I_{CQ} = \frac{6V + 0.7V}{500\Omega} = 13.4mA$$

13. $V_{EE} = I_{CQ}R_E + 0.7V$
 $V_{EE} = 13.4mA(1k\Omega) + 0.7V = 14.1V$

14. $R_{IN} = R_B \parallel R_{IN(BASE)}$

Since $I_{CQ} = 13.4mA \approx I_E$, r_e' is:

$$r_e' = \frac{37mV}{I_E} = \frac{37mV}{13.4mA} = 2.76\Omega$$

$$R_{IN(BASE)} = h_{ie}(r_e' + r_L)$$

$$R_{IN(BASE)} = 150(2.76\Omega + 500\Omega) = 75.4k\Omega$$

$$R_B = 10R_E = 10(1k\Omega) = 10k\Omega$$

Thus:

$$R_{IN} = 10k\Omega \parallel 75.4k\Omega = 8.83k\Omega$$

15. v_{IN}' is the portion of v_{IN} developed across the input terminals of the amplifier. Since $v_{IN} = 3V$ peak, $R_S = 600\Omega$, and $R_{IN} = 8.83k\Omega$, v_{IN}' is:

$$v_{IN}' = \frac{v_{IN}R_{IN}}{R_{IN} + R_S} = \frac{3V(8.83k\Omega)}{8.83k\Omega + 600\Omega} = 2.81V \text{ peak}$$

16. The peak output voltage, v_O , equals $A_V v_{IN}'$. Thus:

$$A_V = \frac{r_L}{r_L + r_e'} = \frac{500\Omega}{500\Omega + 2.76\Omega} = 0.994$$

$$v_O = A_V v_{IN}' = 0.994(2.81V) = 2.79V \text{ peak}$$

$$17. C_1 = \frac{3.18}{f_1 R_{IN}} = \frac{3.18}{1\text{kHz}(8.83\text{k}\Omega)} = 0.36\mu\text{F}$$

$$18. C_2 = \frac{3.18}{f_1 R_L} = \frac{3.18}{1\text{kHz}(1\text{k}\Omega)} = 3.18\mu\text{F}$$

$$19. \text{ Ideally, } h_{fe_{dp}} = h_{fe_1} h_{fe_2} = 100(60) = 6000$$

20. $h_{fe_{dp}}$ calculated in question 19 should be derated by approximately 40%.
Thus:

$$h_{fe_{dp}} = 0.6(6000) = 3600$$

21. $r_{C'_{dp}}$ approximately equals $r_{C'}$, or $4\text{M}\Omega$ in this case.

22. $V_{BE_{dp}} = 2V_{BE}$ or approximately 1.4V for silicon transistors.

HYBRID PARAMETERS

The principle AC BJT parameters discussed previously include α , B , r_e' , r_b' , and r_c' . Usually, data sheets do not directly specify values for these parameters. However, most data sheets do provide “typical values” of four or more “hybrid parameters.”

In this section, you will learn what hybrid parameters are, and why selected hybrid parameters are usually provided on BJT data sheets. In addition, you will learn how to use hybrid parameter values to estimate the AC BJT parameters discussed previously.

Two-Port Networks

A pair of terminals is called a **port**. In many circuits, the input signal is applied to one port, and the output signal is taken from a second port. Such circuits are referred to as **two-port networks**.

Figure 4-27 illustrates this concept. Here, the two-port network is contained inside an imaginary “black box,” which is assumed to be a “sealed unit.”

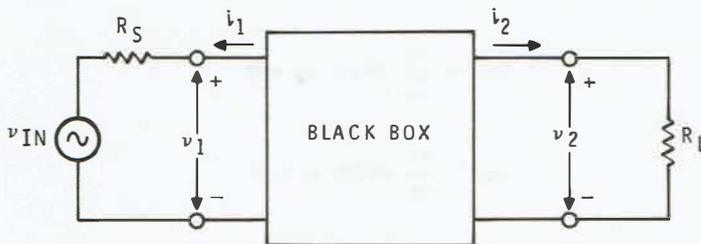


Figure 4-27

A generalized two-part network.

The signal source is connected to the input port, and the load, R_L , is connected to the output port. Note the initial assumptions for current directions, and voltage polarities.

The only information available to us concerning the contents of the black box are the terminal currents, i_1 and i_2 , and terminal voltages, v_1 and v_2 .

Naturally, values for the terminal currents and voltages could be obtained by making appropriate measurements. If a measured current direction, or voltage polarity, differs from the assumed direction or polarity in Figure 4-27, the measured quantity is considered negative.

Two-Port Equations

The terminal currents and terminal voltages in a two-port network are described, mathematically, by the following set of equations:

$$v_1 = h_{11}i_1 + h_{12}v_2$$

$$i_2 = h_{21}i_1 + h_{22}v_2$$

Where: v_1 and i_1 are the input voltage and current.
 v_2 and i_2 are the output voltage and current.
 h_{11} , h_{12} , h_{21} , and h_{22} are constants.

As you will see, you can obtain values for the constants by making appropriate measurements. Once you know the values for the constants, you can construct an equivalent circuit for the two-port network contained in the black box.

DEFINITIONS AND UNITS

Collectively, the constants h_{11} , h_{12} , h_{21} , and h_{22} are called hybrid or h parameters. The h parameters are defined as follows:

$$h_{11} = \frac{v_1}{i_1} \text{ when } v_2 = 0$$

$$h_{21} = \frac{i_2}{i_1} \text{ when } v_2 = 0$$

$$h_{12} = \frac{v_1}{v_2} \text{ when } i_1 = 0$$

$$h_{22} = \frac{i_2}{v_2} \text{ when } i_1 = 0$$

The condition $v_2 = 0$ is equivalent to the output being short-circuited. Similarly, the condition $i_1 = 0$ is equivalent to the input being open-circuited.

It may not be practical to use an actual short-circuit or open-circuit when measuring h parameters. Frequently, a low-reactance capacitor is placed across the output terminals to simulate an AC short circuit. Likewise, a high-reactance choke is placed in series with the input terminals to simulate an AC open circuit.

The term hybrid refers to anything of mixed origin. Since h_{11} , h_{12} , h_{21} , and h_{22} have units corresponding to a resistance, voltage gain, current gain, and admittance, the term hybrid parameters is most appropriate.

A summary of the definitions of the hybrid parameters is provided in Table 4-3. In addition to being called the open-circuit reverse voltage gain, h_{12} is also referred to as the "reverse voltage transfer ratio" or the "voltage feedback ratio."

Parameter	Definition	Description
h_{11}	$\left. \frac{v_1}{i_1} \right _{v_2 = 0}$	short-circuit input impedance
h_{21}	$\left. \frac{i_2}{C_i} \right _{v_2 = 0}$	short-circuit forward current gain
h_{12}	$\left. \frac{v_1}{v_2} \right _{i_1 = 0}$	open-circuit reverse voltage gain
h_{22}	$\left. \frac{i_2}{v_2} \right _{i_1 = 0}$	open-circuit output admittance

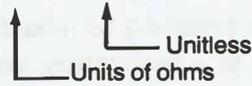
TABLE 4-3

Hybrid Parameters

Equivalent Circuits

Equation 4-33 describes the input port. Specifically:

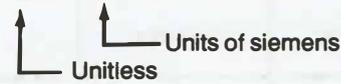
$$v_1 = h_{11}i_1 + h_{12}v_2 \quad (\text{Eq. 4-33})$$



Equation 4-33 suggests a series circuit composed of an equivalent input resistance, h_{11} , and a dependent voltage source, $h_{12}v_2$.

Similarly, Equation 4-34 describes the output port. Specifically:

$$i_2 = h_{21}i_1 + h_{22}v_2 \quad (\text{Eq. 4-34})$$



Equation 4-34 suggests a parallel circuit composed of a dependent current generator, $h_{21}i_1$, and admittance $h_{22}v_2$.

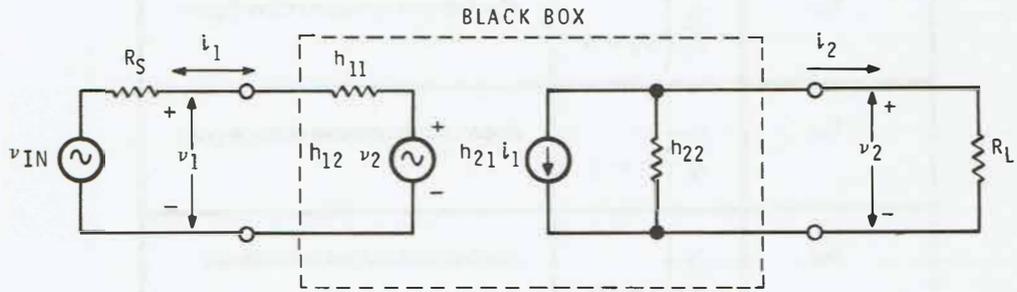


Figure 4-28

Hybrid parameter model for the generalized two-port network in Figure 4-27.

By combining the two equivalent circuits, suggested by Equation 4-33, and Equation 4-34, into a single package, you obtain the h parameter model of a two-port network illustrated in Figure 4-28.

By analyzing the equivalent circuit in Figure 4-28 it is possible to derive equations for A_i , A_v , A_p , R_{IN} , and R_O that apply to virtually any two-port network.* The results of such an analysis are provided in Table 4-4.

It is important to realize when you use the formulas in Table 4-4, that the “actual contents” of the black box are not important. If the h parameter values are known, you can calculate the responses in Table 4-4. The actual contents could be a passive circuit, filter, attenuator, or BJT amplifier.

Parameter	Formula
Current gain	$A_i = \frac{h_{21}}{1 + h_{22}r_L}$
Voltage gain	$A_v = \frac{h_{21}r_L}{h_{12}h_{21}r_L - h_{11}(1 + h_{22}r_L)}$
Power gain	$A_p = A_i A_v$
Input resistance	$R_{IN} = h_{11} - \frac{h_{12}h_{21}r_L}{1 + h_{22}r_L}$
Output resistance	$R_O = \frac{1}{h_{22} - \frac{h_{12}h_{21}}{h_{11} + R_S}}$

TABLE 4-4

Two-port network hybrid parameter formulas.

* Two-port networks for which h parameter analysis is valid must satisfy certain conditions. The “details” of these conditions have been omitted for simplicity.

BJT h Parameters

Since a transistor can be treated as a two-port device, it is possible to specify “typical values” of h_{11} , h_{12} , h_{21} , and h_{22} for a particular type transistor. It is important to realize, however, that the h parameter values will depend upon the BJT configuration.

For this reason, the h parameter values listed on a data sheet do not use the “number notation” discussed previously. Instead, a “letter notation” is used as indicated in Table 4-5.

Parameter	Description	CE	CB	CC
h_{11}	Short-circuit input impedance.	h_{ie}	h_{ib}	h_{ic}
h_{21}	Short-circuit forward current gain.	h_{fe}	h_{fb}	h_{fc}
h_{12}	Open-circuit reverse voltage gain.	h_{re}	h_{rb}	h_{rc}
h_{22}	Open-circuit output admittance.	h_{oe}	h_{ob}	h_{oc}

TABLE 4-5

BJT h parameter notation.

In Table 4-5 note that:

1. The first letter indicates whether the parameter is an input, forward, reverse, or output parameter.
2. The second subscript indicates the particular BJT configuration — common-emitter, common-base, or common-collector.

CE → CB	CE → CC
$h_{ib} = \frac{h_{ie}}{h_{fe} + 1}$ $h_{rb} = \frac{-h_{fe}}{h_{fe} + 1}$ $h_{rb} = \frac{h_{ie}h_{oe}}{h_{fe} + 1} - h_{re}$ $h_{ob} = \frac{h_{oe}}{h_{fe} + 1}$	$h_{ic} = h_{ie}$ $h_{fc} = -(h_{fe} + 1)$ $h_{rc} = 1 - h_{re} \approx 1$ $h_{oc} = h_{oe}$
CB → CE	CB → CC
$h_{ie} = \frac{h_{ib}}{h_{fb} + 1}$ $h_{fe} = \frac{-h_{rb}}{h_{fb} + 1}$ $h_{re} = \frac{h_{ib}h_{ob}}{h_{fb} + 1} - h_{rb}$ $h_{oe} = \frac{h_{ob}}{h_{fb} + 1}$	$h_{ic} = \frac{h_{ib}}{h_{fb} + 1}$ $h_{fc} = \frac{-1}{h_{fb} + 1}$ $h_{rc} = \frac{1 - h_{cb}h_{ob}}{h_{fb} + 1} + h_{rb}$ $h_{oc} = \frac{h_{ob}}{h_{fb} + 1}$

TABLE 4-6

Approximate h parameter conversion formulas.

Manufacturers data sheets rarely provide a complete set of twelve h parameters for each type transistor. Usually, h parameter values are provided for the common-emitter configuration, the common-base configuration, or a combination of the two.

For this reason, it is often necessary, when working with h parameters, to convert the parameter values for one configuration to the equivalent parameter values for another configuration. Table 4-6 summarizes the most frequently required conversion formulas.

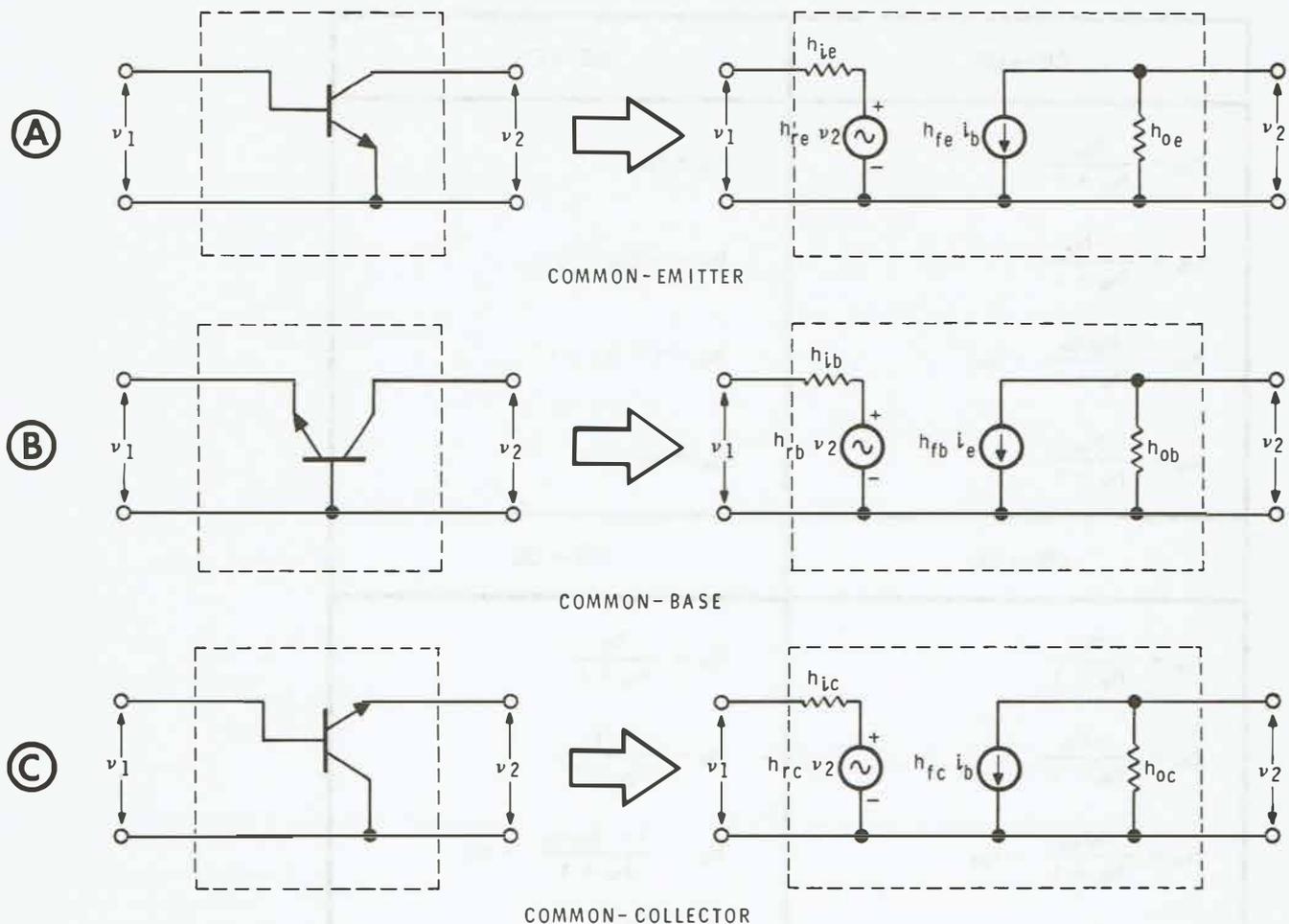


Figure 4-29

Small signal, AC, h parameter BJT models.

- A. Common-emitter.
- B. Common-base.
- C. Common-collector.

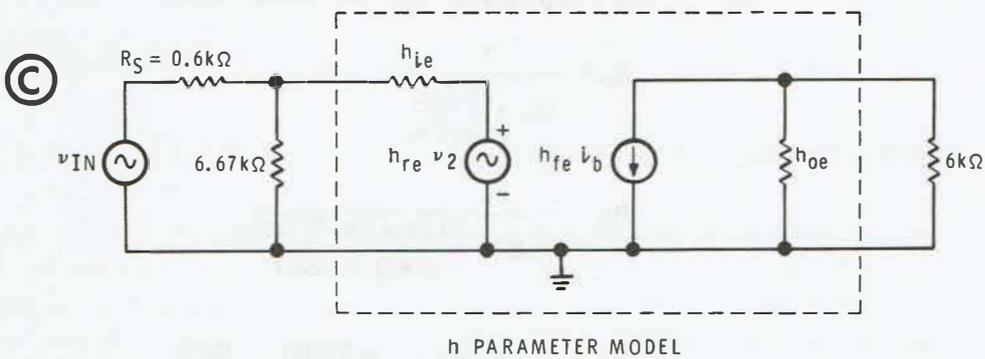
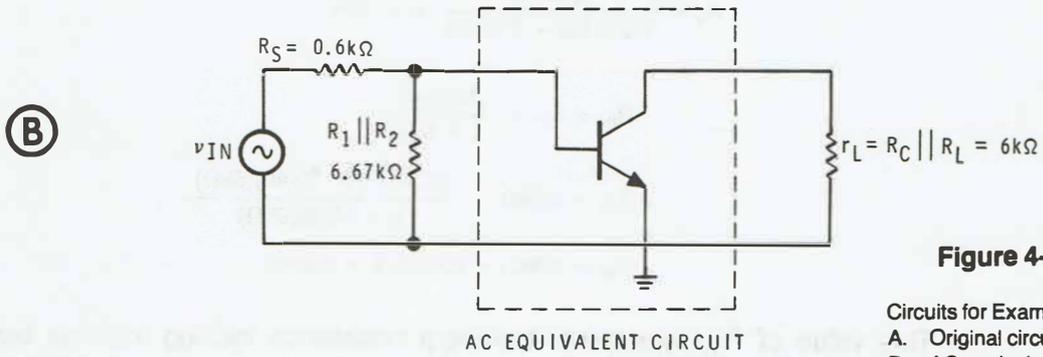
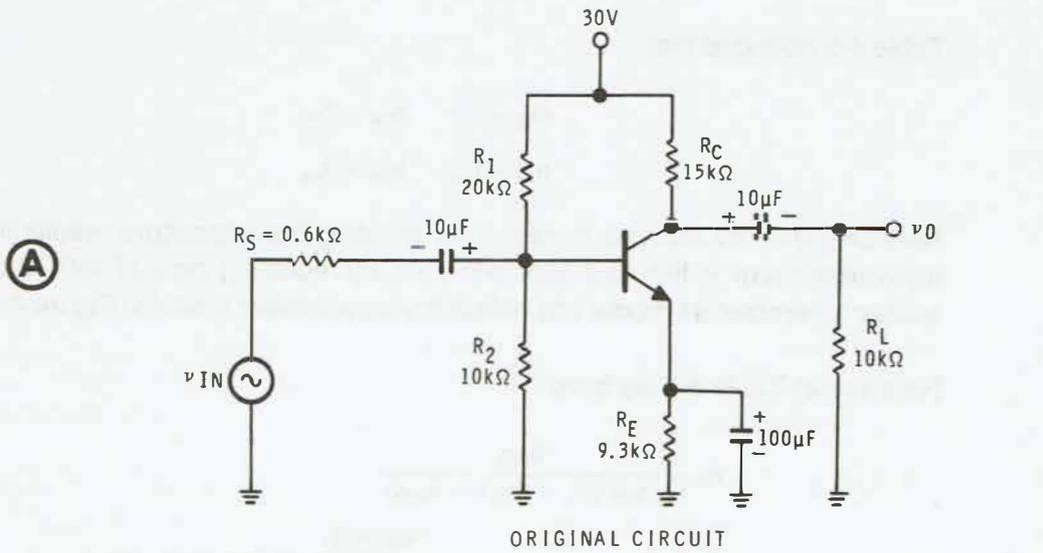
BJT h PARAMETER ANALYSIS

By substituting the appropriate letter notation, in Table 4-5, for h_{11} , h_{12} , h_{21} , and h_{22} in the general h parameter model in Figure 4-28, you obtain the AC equivalent circuits in Figure 4-29. The following example illustrates how h parameters can be used to analyze a typical amplifier.

Example 4-12

The data sheet for the BJT in Figure 4-30A lists the following h parameter values for $I_C = 1\text{mA}$.

When you are using h parameters, the units for h_{oe} is siemens, **NOT TIME**. Therefore, $13\ \mu\text{S}$ means micro siemens.



$$h_{ie} = 3.5k\Omega \quad h_{re} = 2.75 \times 10^{-4}$$

$$h_{fe} = 140 \quad h_{oe} = 13\mu S$$

Using these values, estimate A_V , R_{IN} , and R_O , for the amplifier in Figure 4-30A.

Figure 4-30

- Circuits for Example 4-12.
 A. Original circuit.
 B. AC equivalent circuit.
 C. h parameter model.

Table 4-5 indicates that:

$$h_{11} = h_{ie} \quad h_{12} = h_{re}$$

$$h_{21} = h_{fe} \quad h_{22} = h_{oe}$$

Reducing the DC sources to zero, and shorting the capacitors results in the AC equivalent circuit in Figure 4-30B. Similarly, by replacing the BJT with its common-emitter h parameter model you obtain the h parameter model in Figure 4-30C.

Referring to Table 4-4 we have:

$$A_V = \frac{h_{21}r_L}{h_{12}h_{21}r_L - h_{11}(1 + h_{22}r_L)}$$

$$A_V = \frac{140(6k\Omega)}{(2.75 \times 10^{-4})(140)(6k\Omega) - 3.5k\Omega[1 + 13\mu S(6k\Omega)]}$$

$$A_V = \frac{840k\Omega}{0.231k\Omega - 3.78k\Omega} = -236$$

$$R_{IN} = h_{11} - \frac{h_{12}h_{21}r_L}{1 + h_{22}r_L}$$

$$R_{IN} = 3.5k\Omega - \frac{2.75 \times 10^{-4}(140)(6k\Omega)}{1 + 13\mu S(6k\Omega)}$$

$$R_{IN} = 3.5k\Omega - 0.214k\Omega = 3.29k\Omega$$

This value of R_{IN} represents the input resistance looking into the base of the BJT in Figure 4-30. The input resistance seen by the signal source is therefore:

$$R_{IN} = R_B || R_{IN(BASE)} = 6.67k\Omega || 3.29k\Omega = 2.2k\Omega$$

$$R_O = \frac{1}{h_{22} - \frac{h_{12}h_{21}}{h_{11}R_S}}$$

$$R_O = \frac{1}{13\mu S - \frac{(2.75 \times 10^{-4})(140)}{3.5k\Omega + 0.6k\Omega}}$$

$$R_O = \frac{1}{13\mu S - 9.39\mu S} = 277k\Omega \quad (\text{BJT})$$

This value of R_O represents the output resistance looking back into the collector of the BJT. The output resistance of the amplifier in Figure 4-30 equals the parallel combination of R_O and R_C . Thus:

$$R_O = 277\text{k}\Omega \parallel 15\text{k}\Omega = 14.23\text{k}\Omega \quad (\text{complete circuit})$$

Example 4-13

Suppose you wanted to use the BJT in Example 4-12 in an emitter-follower, common-collector circuit. What are the appropriate h parameters values?

Since you know the common-emitter values, you can convert them, using Table 4-6, to the required common-collector values in this manner:

$$\begin{aligned} h_{ic} &= h_{ie} = 3.5\text{k}\Omega \\ h_{fc} &= -(h_{fe} + 1) = -(140 + 1) = -141 \\ h_{rc} &= 1 - h_{re} = 1 - 2.75 \times 10^{-4} \approx 1 \\ h_{oc} &= h_{oe} = 13\mu\text{S} \end{aligned}$$

Approximate Versus Hybrid Methods

Soon after transistors were introduced, the use of h parameters became the preferred method for the analysis and design of BJT circuits. Since h parameters are relatively easy to measure, manufacturers supplied, and continue to supply, h parameter information on BJT data sheets.

Once h parameter methods were firmly established, the approximate methods discussed earlier became increasingly popular. Compared to h parameters, the approximate methods offer the following advantages:

1. Generally speaking, the approximate methods require fewer calculations than the h parameter methods.
2. Approximate methods enable you to analyze and design many useful circuits in the absence of the BJT's data sheet. For example, most small-signal voltage amplifiers can be analyzed, or designed, by assuming $\alpha = .99$, $r_e' = \frac{37\text{mV}}{I_E}$, $r_b' \approx 0$, $B = 100$, and $r_C' \gg R_L$.

Since the approximate methods are easy to work with, they will be emphasized in this course.

Useful Conversions

In some circuits, r_b' and/or r_c' cannot be neglected. In addition, if a BJT's data sheet is available, you should use the data sheet values of α or B in your calculations. For these reasons, it is sometimes necessary to estimate values for α , B , r_e' , r_b' , and r_c' based on the h parameter values provided on the data sheet. Approximate formulas for making the appropriate "conversions" are provided in Table 4-7. Since r_e' varies with I_E , the relationship $r_e' \approx h_{ib}$ is valid only if the value of h_{ib} is specified at the value of I_E in the actual circuit.

Parameter	Approximate Equivalents
α	$\frac{1}{1 - \frac{(h_{fb} + 1)}{h_{fb}}} = \frac{h_{fe}}{h_{fe} + 1}$
B	$\frac{-h_{fb}}{h_{fb} + 1} = h_{fe}$
r_e'	$h_{ib} = \frac{h_{ie}}{h_{fe}}$
r_b'	$\frac{h_{rb}}{h_{ob}} = h_{ie} - \frac{h_{fe}h_{re}}{h_{oe}}$
r_c'	$\frac{1}{h_{ob}} = \frac{h_{fe}}{h_{oe}}$

TABLE 4-7

Useful conversions.

Example 4-14

Estimate values for α , B , r_e' , r_b' , and r_c' assuming $h_{ie} = 3.5k\Omega$, $h_{fe} = 140$, $h_{re} = 2.75 \times 10^{-4}$, and $h_{oe} = 13\mu S$.

- $$\alpha = \frac{h_{fe}}{h_{fe} + 1} = \frac{140}{141} = 0.993$$
- $$B = h_{fe} = 140$$

$$3. \quad r_{e'} = \frac{h_{ie}}{h_{fe}} = \frac{3.5\text{k}\Omega}{140} = 25\Omega$$

$$4. \quad r_{b'} = h_{ie} - \frac{h_{fe}h_{re}}{h_{oe}}$$

$$r_{b'} = 3.5\text{k}\Omega - \frac{140(2.75 \times 10^{-4})}{13\mu\text{S}}$$

$$r_{b'} = 3.5\text{k}\Omega - 2.96\text{k}\Omega = 540\Omega$$

$$5. \quad r_{c'} = \frac{h_{fe}}{h_{oe}} = \frac{140}{13\mu\text{S}} = 10.77\text{M}\Omega$$

Self-Test Review

23. A pair of terminals is referred to as a _____.
24. h_{11} represents the input impedance of a two-port network when the output terminals are _____.
25. h_{22} represents the output admittance of a two-port network when the input terminals are _____.

Use the following h parameter values for questions 26 through 32.

$$\begin{array}{ll} h_{ie} = 2\text{k}\Omega & h_{re} = 1.1 \times 10^{-4} \\ h_{fe} = 130 & h_{oe} = 14\mu\text{S} \end{array}$$

26. h_{ib} approximately equals _____ Ω .
27. h_{re} approximately equals _____.
28. Assuming the BJT is used in a common-emitter circuit, and $r_L = 10\text{k}\Omega$, the voltage gain is approximately _____.
29. $r_{e'} \approx$ _____ Ω .
30. $r_{b'} \approx$ _____ Ω .
31. $r_{c'} \approx$ _____ $\text{M}\Omega$.
32. $B \approx$ _____.

Answers

- | | |
|---------------------|------------|
| 23. port | 28. -608.3 |
| 24. short-circuited | 29. 15.27Ω |
| 25. open-circuited | 30. 980Ω |
| 26. 15.27Ω | 31. 9.29MΩ |
| 27. 1 | 32. 130 |

The solutions to questions 26 through 32 follow.

26. Refer to the CE to CB formulas in Table 4-6.

$$h_{ib} = \frac{h_{ie}}{h_{fe} + 1} = \frac{2k\Omega}{130 + 1} = 15.27\Omega$$

27. Refer to the CE to CC formulas in Table 4-6.

$$h_{rc} = 1 - h_{re} = 1 - 1.1 \times 10^{-4} \approx 1$$

28. From Table 4-4:

$$A_v = \frac{h_{21}r_L}{h_{12}h_{21}r_L - h_{11}(1 + h_{22}r_L)}$$

In this case, $h_{11} = h_{ie} = 2\text{k}\Omega$, $h_{21} = h_{fe} = 130$, $h_{12} = h_{re} = 1.1 \times 10^{-4}$, and $h_{22} = h_{oe} = 14\mu\text{S}$. Therefore:

$$A_v = \frac{130(10\text{k}\Omega)}{(1.1 \times 10^{-4})(130)(10\text{k}\Omega) - 2\text{k}\Omega[1 + 14\mu\text{S}(10\text{k}\Omega)]}$$

$$A_v = \frac{1300\text{k}\Omega}{0.143\text{k}\Omega - 2.28\text{k}\Omega} = -608.3$$

29. From Table 4-7 $r_e' = h_{ib}$. Since h_{ib} was calculated to be 15.27Ω in question 26, $r_e' \approx 15.27\Omega$.

30. From Table 4-7:

$$r_b' = h_{ie} - \frac{h_{fe}h_{re}}{h_{oe}}$$

$$r_b' = 2\text{k}\Omega - \frac{130(1.1 \times 10^{-4})}{14\mu\text{S}}$$

$$r_b' = 2\text{k}\Omega - 1.02\text{k}\Omega = 980\Omega$$

31. From Table 4-7:

$$r_c' = \frac{h_{fe}}{h_{oe}} = \frac{130}{14\mu\text{S}} = 9.29\text{M}\Omega$$

32. From Table 4-7:

$$B = h_{fe} = 130$$

SUMMARY

The analysis and design of common-base amplifiers is similar to the analysis and design of common-emitter amplifiers. Unlike common-emitter amplifiers, the input and output signals in a common-base amplifier are in phase with each other.

The principle disadvantage of a common-base amplifier is that it usually has low input resistance. Since common-emitter amplifiers have larger input resistances, they are preferred for low and mid-frequency applications.

Common-collector amplifiers are referred to as emitter followers. Typically, emitter followers are characterized by a voltage gain of approximately 1, large values of R_{IN} , and small values of R_O .

These characteristics make emitter followers ideal for impedance matching and buffering applications. Like the common-base amplifier, the input and output signals in an emitter follower are in phase with each other.

Darlington pairs are used when an emitter follower is required to have a very large input resistance. You can obtain Darlington pairs by using two discrete BJTs, or purchasing a single-unit package. In any event, when you analyze Darlington pair emitter followers, you must remember to include the effects of r_C' .

By referring to the emitter-follower design guide, you should be able to design useful emitter follower circuits. In many cases, the final design will require a compromise between large values of R_{IN} , and a centered Q point.

BJT data sheets usually provide values for selected hybrid or h parameters. Examples are provided to illustrate how h parameters can be used to analyze BJT circuits.

Since the approximate methods are easy to use, they are the methods emphasized in this course. Various tables are provided that should assist you when you work with h parameters. Table 4-7 is especially useful, since it lets you convert h parameter values to the AC BJT parameters introduced in the previous units.

UNIT EXAMINATION

The following multiple choice examination is designed to test your understanding of the material presented in this unit. Place a check beside the multiple choice answer (A, B, C, or D) that you feel is most correct. When you have completed the examination, compare your answers with the correct ones that appear after the exam.

1. In Figure 4-31, the voltage gain is approximately:

- A. -11.87.
- B. 11.87.
- C. -108.1.
- D. Unity.

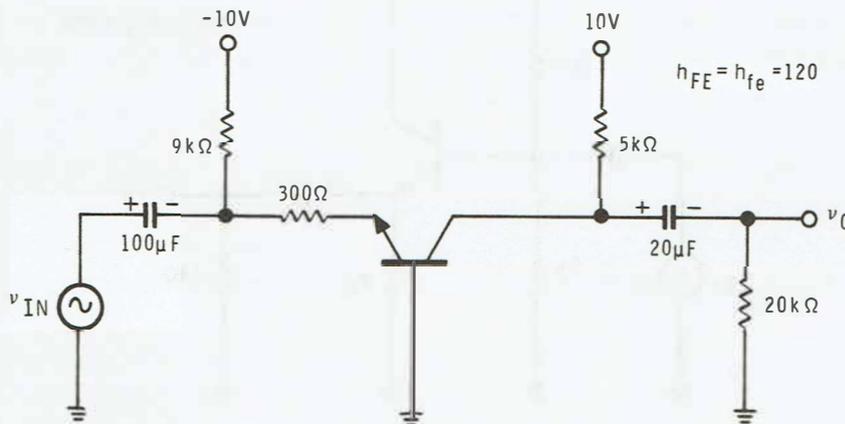


Figure 4-31

Circuit for questions 1 to 3.

2. In Figure 4-31, the circuit's input resistance is approximately:

- A. 7.36kΩ.
- B. 5kΩ.
- C. 4kΩ.
- D. 324.8Ω.

3. In Figure 4-31, the output resistance is approximately:

- A. 4kΩ.
- B. 5kΩ.
- C. 20kΩ.
- D. 7.36kΩ.

4. An emitter follower is an example of a:

- A. Common-emitter amplifier.
- B. Common-base amplifier.
- C. Common-collector amplifier.
- D. High gain amplifier.

5. In Figure 4-32, a reasonable value for R_E is:

- A. $5M\Omega$.
- B. $500k\Omega$.
- C. $50k\Omega$.
- D. $5k\Omega$.

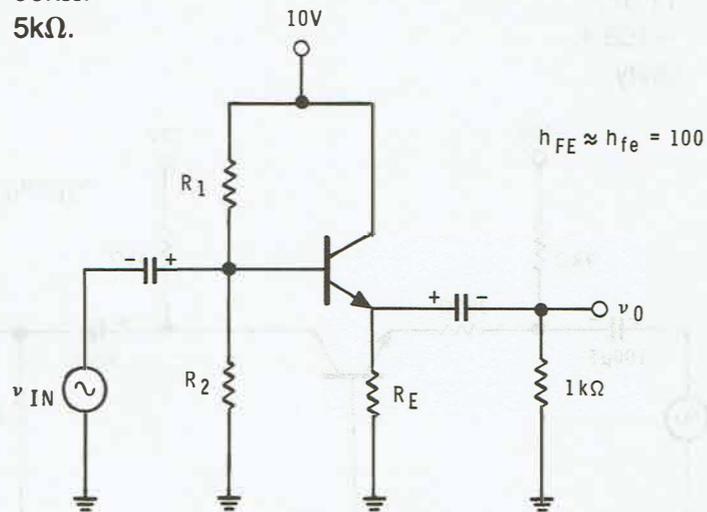


Figure 4-32

Circuit for questions 5 to 7.

6. In Figure 4-32 if $R_2 = 10R_E$, R_1 , should equal:

- A. $8.14k\Omega$.
- B. $22k\Omega$.
- C. $33k\Omega$.
- D. $50k\Omega$.

7. In Figure 4-32 R_{IN} equals approximately:

- A. $50k\Omega$.
- B. $12.2k\Omega$.
- C. $9.76k\Omega$.
- D. $6.47k\Omega$.

The following h parameter values apply to questions 8 through 11.

$$\begin{array}{ll} h_{ie} = 3\text{k}\Omega & h_{re} = 1.2 \times 10^{-4} \\ h_{fe} = 115 & h_{oe} = 8\mu\text{S} \end{array}$$

8. h_{rb} approximately equals:

- A. 0.87×10^{-4} .
- B. 1.63×10^{-4} .
- C. 2.25×10^{-4} .
- D. 6.3×10^{-4} .

9. h_{ob} approximately equals:

- A. $0.069\mu\text{S}$.
- B. $1.27\mu\text{S}$.
- C. $5.63\mu\text{S}$.
- D. $8\mu\text{S}$.

10. r_C' approximately equals:

- A. $8.49\text{M}\Omega$.
- B. $10.63\text{M}\Omega$.
- C. $14.49\text{M}\Omega$.
- D. $23\text{M}\Omega$.

11. r_b' approximately equals:

- A. 12.6Ω .
- B. 126Ω .
- C. 37Ω .
- D. $1.26\text{k}\Omega$.

EXAMINATION ANSWERS

1. B — In a common-base circuit, $A_V = \frac{r_L}{R_{E_1} + r_{e'}}$.

$$I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{10V - 0.7V}{9.3k\Omega} = 1mA$$

$$r_{e'} = \frac{37mV}{I_E} = \frac{37mV}{1mA} = 37\Omega$$

$$r_L = R_C || R_L = 5k\Omega || 20k\Omega = 4k\Omega$$

Since $R_{E_1} = 300\Omega$:

$$A_V = \frac{4k\Omega}{300\Omega + 37\Omega} = 11.87$$

2. D — $R_{IN} = R_E || (R_{E_1} + r_{e'})$
 $R_{IN} = 9k\Omega || (300\Omega + 37\Omega)$
 $R_{IN} = 324.8\Omega$

3. B — In a common-base circuit, $R_O \approx R_C$. Thus, $R_O \approx 5k\Omega$.

4. C — A common-collector amplifier is referred to as an emitter follower.

5. D — As a guide R_E equals 1 to 5 times the value of R_L . Since $R_L = 1k\Omega$, a reasonable choice for R_E is $5k\Omega$.

6. A — To calculate R_1 , you must first calculate values for V_{BQ} and R_2 . Thus:

$$I_{CQ} = \frac{V_{CC}}{R_E + r_L} = \frac{10V}{5k\Omega + 5k\Omega || 1k\Omega}$$

$$I_{CQ} = \frac{10V}{5.833k\Omega} = 1.71mA$$

$$V_{EQ} = I_{CQ}R_E = 1.71mA(5k\Omega) = 8.6V$$

$$V_{BQ} = V_{EQ} + 0.7V = 9.3V$$

$$R_2 = 10R_E = 10(5k\Omega) = 50k\Omega$$

$$R_1 = \frac{R_2(V_{CC} - V_{BQ})}{V_{BQ}} = \frac{50k\Omega(10V - 9.3V)}{9.3V} = 3.76k\Omega$$

7. D — $R_B = R_1 \parallel R_2 = 8.14\text{k}\Omega \parallel 50\text{k}\Omega = 7\text{k}\Omega$

$$R_{IN(BASE)} = h_{ie}(r_L + r_e')$$

Since $I_{CQ} = 1.71\text{mA}$ and $r_e' = 37\text{mV}/1.71\text{mA}$ or 21.64Ω :

$$R_{IN(BASE)} = 100(833\Omega + 21.64\Omega) = 85.5\text{k}\Omega$$

Finally:

$$R_{IN} = R_B \parallel R_{IN(BASE)} = 7\text{k}\Omega \parallel 85.5\text{k}\Omega = 6.47\text{k}\Omega$$

8. A — From Table 4-6:

$$h_{rb} = \frac{h_{ie}h_{oe}}{h_{fe} + 1} - h_{re}$$

$$h_{rb} = \frac{3\text{k}\Omega(8\mu\text{S})}{115 - 1} - 1.2 \times 10^{-4}$$

$$h_{rb} = \frac{240 \times 10^{-4}}{116} - 1.2 \times 10^{-4} = 0.87 \times 10^{-4}$$

9. A — From Table 4-6:

$$h_{ob} = \frac{h_{oe}}{h_{fe} + 1} = \frac{8\mu\text{S}}{115 + 1} = 0.069\mu\text{S}$$

10. C — From Table 4-7:

$$r_{c'} = \frac{1}{h_{ob}} = \frac{1}{0.069\mu\text{S}} = 14.49\text{M}\Omega$$

11. D — From Table 4-7:

$$r_{b'} = \frac{h_{rb}}{h_{ob}} = \frac{0.87 \times 10^{-4}}{0.069\mu\text{S}} = 12.6 \times 10^2\Omega$$

$$r_{b'} = 1.26\text{k}\Omega$$

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UNIT 5

POWER AMPLIFIERS

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POWER AMPLIFIERS

INTRODUCTION

Generally speaking, amplifiers may be described as being either voltage or power amplifiers. Units 3 and 4 discussed the analysis and design of voltage amplifiers. In this unit we will consider the analysis and design of selected power amplifiers.

As you know, voltage amplifiers are used to increase signal levels. Once sufficient voltage levels are available, a power amplifier is employed to drive the actual load device. Thus, the power amplifier is the last stage of amplification in a typical amplifier system.

Since the current and voltage swings in power amplifiers are quite large, power amplifiers are also called "large signal" amplifiers. Both voltage (small signal) and power (large signal) amplifiers may operate in the **class A**, **class AB**, **class B**, or **class C** modes. You will examine all four of these operating modes in this unit.

In addition, examples illustrating the design of class A and class AB power amplifiers will be provided.

UNIT OBJECTIVES

When you have completed this unit, you should be able to:

1. Analyze and design the following types of power amplifiers:
 - A. Class A RC coupled.
 - B. Class A transformer coupled.
 - C. Class AB push-pull, complementary-symmetry.
2. Sketch circuits for Darlington and quasi-complementary symmetry circuits.
3. Discuss the operation of a basic class C amplifier.
4. Perform a three-point distortion analysis.
5. Explain how harmonic and crossover distortion can be minimized in typical power amplifiers.

UNIT ACTIVITY GUIDE

- Read the section on "Power Amplifier Fundamentals".
- Answer Self-Test Review questions 1-15.
- Read the discussion of distortion in the section on "Distortion, class B, class AB, and class C Amplifiers".
- Perform Experiment 8 in Unit 9.
- Finish reading the section on "Distortion, class B, class AB, and class C Amplifiers".
- Answer Self-Test Review questions 16-25.
- Perform Experiment 9 in Unit 9.
- Study the Summary.
- Complete the Unit Examination.
- Check the Examination Answers.



POWER AMPLIFIER FUNDAMENTALS

Of the various types of amplifiers available, class A amplifiers are the least efficient. For this reason, class A amplifiers are usually limited to relatively low power applications.

In this portion of the unit we will discuss essential power amplifier concepts. In addition, several examples illustrating the analysis and design of class A power amplifiers will be provided.

Voltage Versus Power Amplifiers

A typical amplifier system consists of a signal source, one or more voltage amplifiers, a power amplifier, and the load. This concept is illustrated by the simplified public address system shown in Figure 5-1. Note that the amplifier chain between the signal source (microphone) and load (speaker) consists of three voltage amplifiers and one power amplifier.

When several voltage amplifiers are cascaded, as in Figure 5-1, the first stage is usually referred to as a **preamplifier**. Similarly, the stage preceding the power amplifier is called the **driver**. In Figure 5-1, note that, as the signal moves through each stage, its power level increases. Compared to power amplifiers, the signal amplitudes and power levels in voltage amplifiers are relatively small. Therefore, voltage amplifiers are considered low-level stages, and power amplifiers high-level stages.

The essential difference between voltage and power amplifiers is the amount of quiescent and signal power associated with each amplifier. Naturally, the transistors used in power amplifiers (power transistors) will have current and voltage ratings considerably larger than their small-signal counterparts.

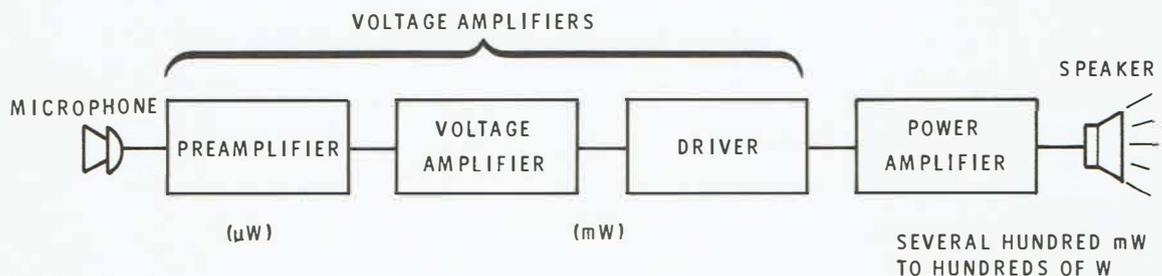


Figure 5-1

An elementary public address system.

Modes of Operation

Power amplifiers are classified according to their mode of operation. The four fundamental modes include class A, class AB, class B, and class C. For a given amplifier, the particular mode of operation is determined by the quiescent conditions. The fundamental modes of operation are described in the next four paragraphs.

CLASS A

In this mode, AC collector current flows during the entire cycle, 360° , of the AC input voltage as shown in Figure 5-2A. To achieve class A operation, the Q point is located in the middle of the AC load line. Class A operation assumes the amplitude of the AC input signal is small enough to avoid clipping. Also, since class A amplifiers operate in the linear region, distortion is minimum.

CLASS AB

Here, AC collector current flows for more than 180° but less than 360° of the AC input cycle. The collector current produced in a class AB amplifier is illustrated in Figure 5-2B. Class AB operation is achieved by locating the Q point closer to either the saturation or cutoff end of the AC load line.

CLASS B

When AC collector current flows for 180° , or exactly one-half of the AC input cycle, you have class B operation as shown in Figure 5-2C. Class B operation is achieved by locating the Q point at cutoff. Consequently, a class B amplifier amplifies only one-half of the AC input voltage.

CLASS C

In this mode, AC collector current flows for less than 180° of the AC input cycle as shown in Figure 5-2D. To achieve class C operation, the Q point is located "beyond cutoff". This means that the emitter-base junction is actually reversed biased. Hence, the AC input voltage must overcome the reverse-bias voltage before the transistor can conduct. For this reason, a class C amplifier amplifies only a small portion of the AC input signal.

Clearly, the collector currents in class AB, class B, and class C amplifiers are **distorted versions** of the AC input signal. In the second part of this unit, you will see how these distorted waveforms can be processed to obtain output voltages that closely resemble the original AC input voltage.

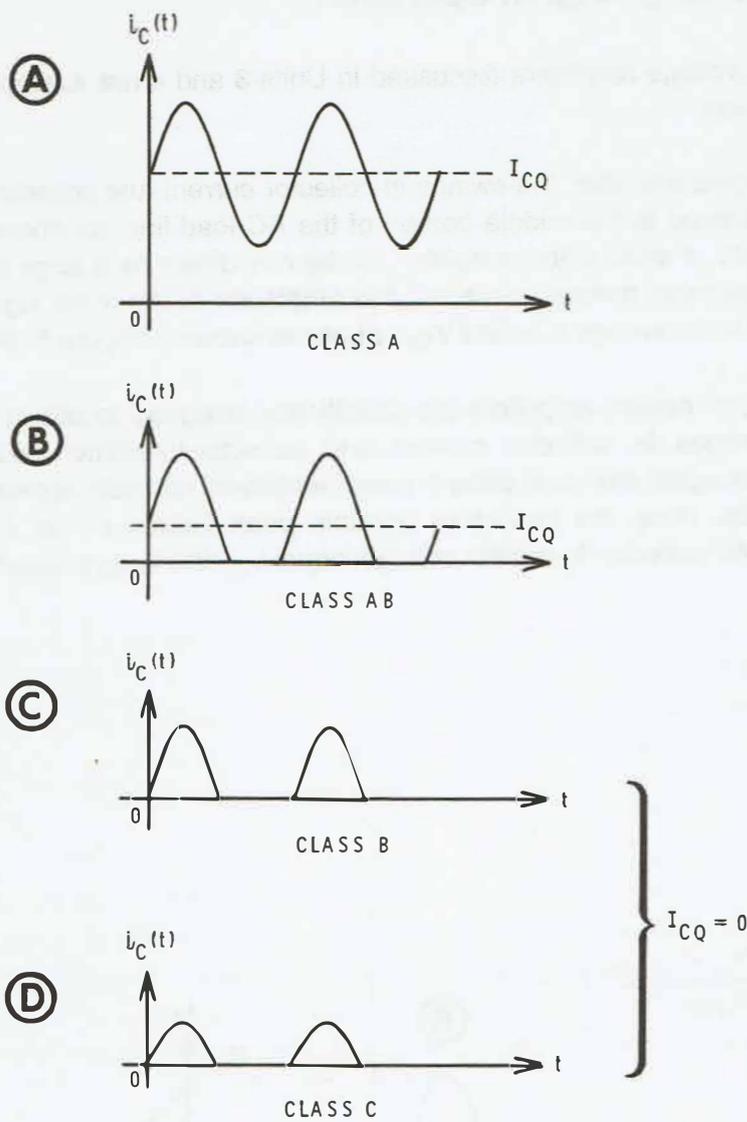


Figure 5-2

Collector current in a class A, class AB, class B, and class C amplifier.

- A. Class A.
- B. Class AB.
- C. Class B.
- D. Class C.

Small and Large Signal Operation

The class A voltage amplifiers discussed in Units 3 and 4 are examples of small signal amplifiers.

In a small signal amplifier, the swings in collector current and collector-to-emitter voltage are limited to the middle portion of the AC load line, as shown in Figure 5-3A. Naturally, a small signal amplifier can be overdriven by a large input signal. However, assuming normal operation, the amplitude of the input signal is small enough so that the swings in I_C and V_{CE} appear as shown in Figure 5-3A.

Large signal, or power, amplifiers are specifically designed to obtain the largest possible changes in collector current and collector-to-emitter voltage. Consequently, the signal swings in class A power amplifiers normally appear as shown in Figure 5-3B. Here, the maximum possible **peak values** of the AC collector current, and AC collector-to-emitter voltage, equal I_{CQ} and V_{CEQ} respectively.

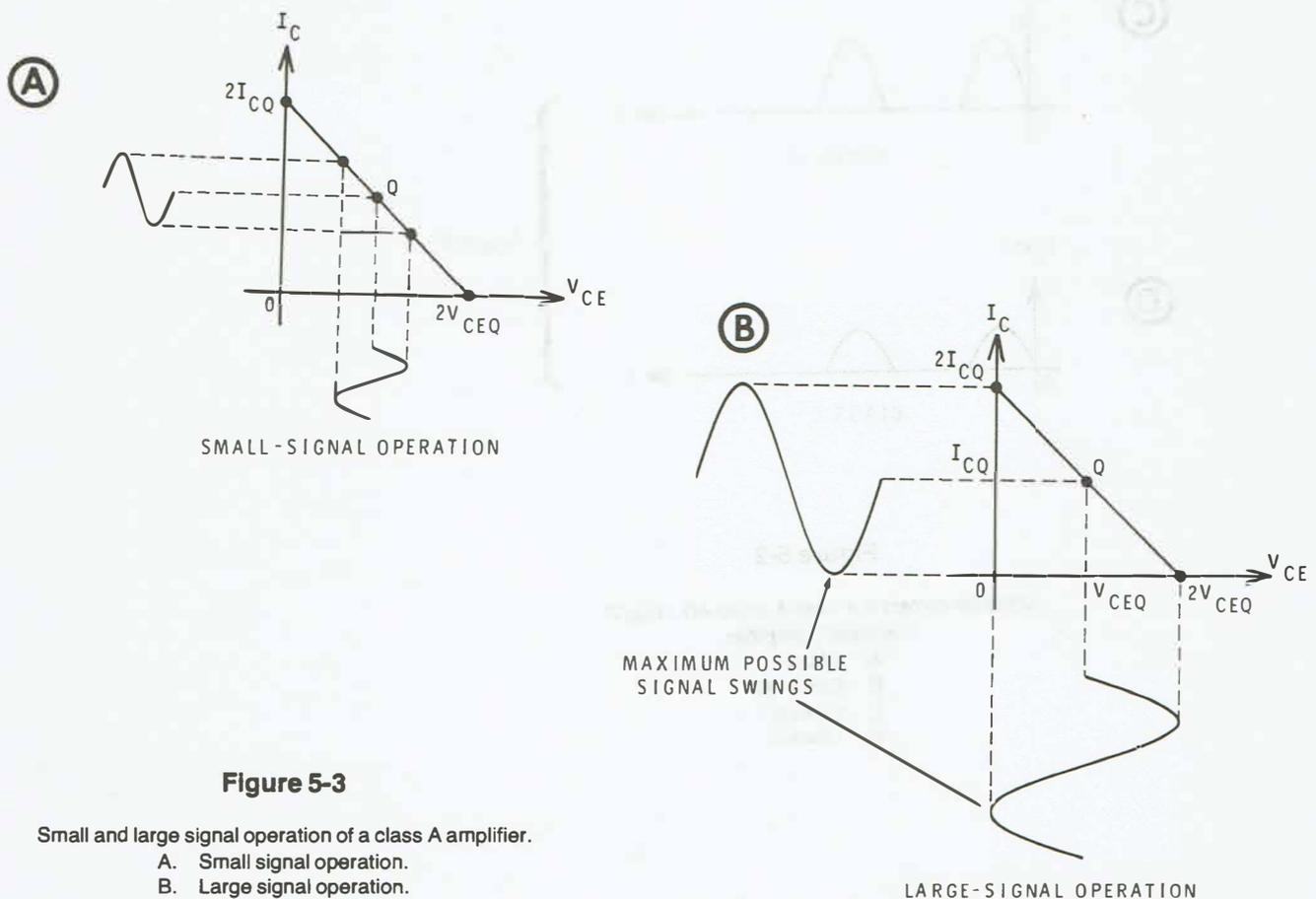


Figure 5-3

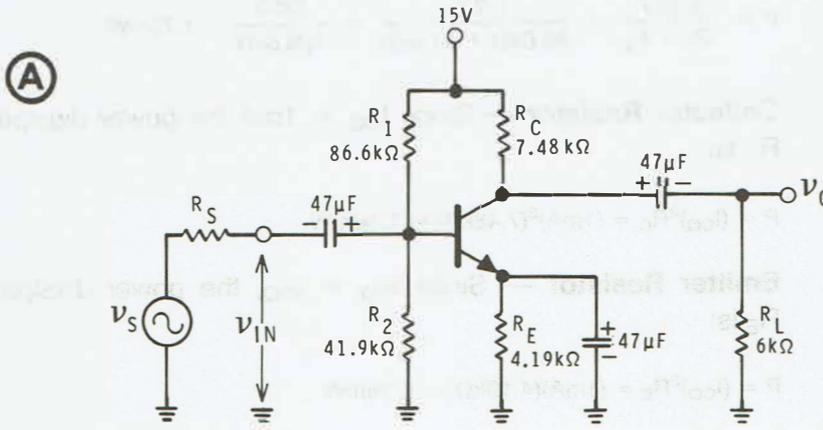
Small and large signal operation of a class A amplifier.

- A. Small signal operation.
- B. Large signal operation.

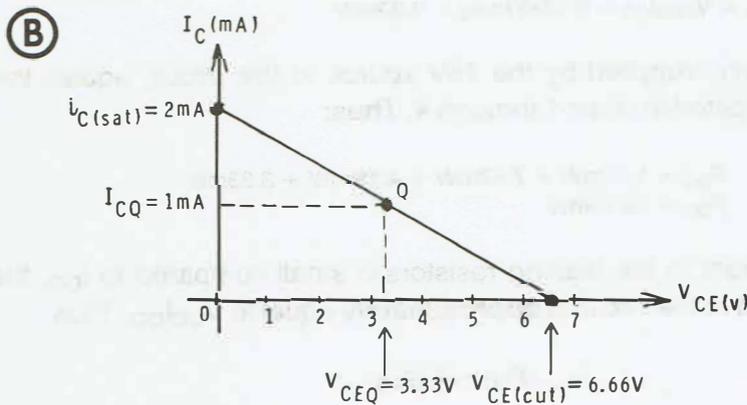
Power Calculations in Class A Amplifiers

The formulas used to compute power in DC circuits, $P = VI$, $P = I^2R$, and $P = V^2/R$, apply to AC circuits if the values of V and I are **rms values**.

By way of introduction, we will calculate the various powers associated with the class A voltage amplifier shown in Figure 5-4A. The AC load line for this amplifier is sketched in Figure 5-4B.



CLASS A VOLTAGE AMPLIFIER



A C LOAD LINE

Figure 5-4

Class A voltage amplifier, and its AC load line.

- A. Class A voltage amplifier.
- B. AC load line.

DC INPUT POWER

In Figure 5-4A, DC power is dissipated by the biasing resistors, collector resistors, emitter resistor, and the transistor. These DC powers are calculated as follows:

1. **Biasing Resistors** — Neglecting the small DC base current, I_B , resistors R_1 and R_2 are connected in series across the 15V supply voltage. Thus:

$$P = \frac{(V_{CC})^2}{R_1 + R_2} = \frac{(15V)^2}{86.6k\Omega + 41.9k\Omega} = \frac{225V}{128.5k\Omega} = 1.75mW$$

2. **Collector Resistor** — Since $I_{CQ} = 1mA$ the power dissipated by R_C is:

$$P = (I_{CQ})^2 R_C = (1mA)^2 (7.48k\Omega) = 7.48mW$$

3. **Emitter Resistor** — Since $I_{EQ} \approx I_{CQ}$, the power dissipated by R_E is:

$$P = (I_{CQ})^2 R_E = (1mA)^2 (4.19k\Omega) = 4.19mW$$

4. **Transistor** — Recall from Unit 2 that the power dissipated by a transistor under quiescent conditions is:

$$P_{DQ} = V_{CEQ} I_{CQ} = 3.33V(1mA) = 3.33mW$$

The total DC power, supplied by the 15V source to the circuit, equals the sum of the powers computed in steps 1 through 4. Thus:

$$\begin{aligned} P_{DC} &= 1.75mW + 7.48mW + 4.19mW + 3.33mW \\ P_{DC} &= 16.75mW \end{aligned}$$

Since the DC current in the biasing resistors is small compared to I_{CQ} , the total DC power supplied to the circuit is **approximately** equal to $V_{CC} I_{CQ}$. Thus:

$$P_{DC} \approx V_{CC} I_{CQ}$$

For example, since $V_{CC} = 15V$ and $I_{CQ} = 1mA$, the total DC power approximately equals $15V (1mA)$, or $15mW$. Since $15mW$ is 89.5 percent of $16.75mW$, you can see that the approximate formula is reasonably accurate.

AC OUTPUT POWER

The AC equivalent circuit for the amplifier in Figure 5-4A is shown in Figure 5-5. Here, maximum power is supplied to the AC load resistance, r_L , when i_C and v_{CE} are maximum.

In a class A amplifier, the maximum possible peak values of i_C and v_{CE} equal I_{CQ} and V_{CEQ} respectively. Also, when calculating AC power, rms values must be employed. Thus, the maximum possible AC output power is:

$$P = (0.707 V_{CEQ})(0.707 I_{CQ})$$

$$P = [(0.707)(3.33V)][(0.707)(1mA)] = 1.67mW$$

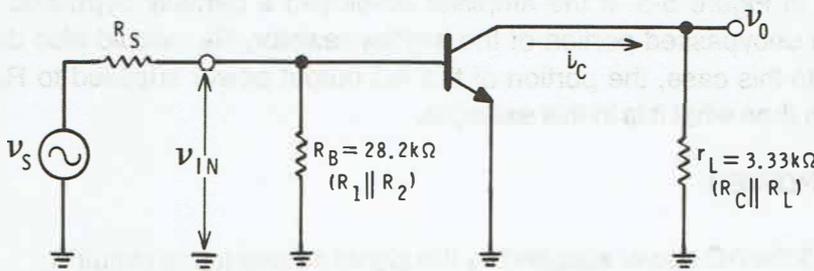


Figure 5-5

AC equivalent circuit of the amplifier in Figure 5-4A.

It is important to realize that **only a portion** of the AC output power is supplied to the actual load device, R_L . The remaining portion is dissipated by the collector resistor, R_C . Referring back to Figure 5-4, you can see that the AC power supplied to R_L is:

$$P = \frac{(0.707V_{CEQ})^2}{R_L} = \frac{[0.707(3.33V)]^2}{6k\Omega} = 0.924mW$$

Similarly, the AC power supplied to R_C is:

$$P = \frac{(0.707V_{CEQ})^2}{R_C} = \frac{[0.707(3.33V)]^2}{7.48k\Omega} = 0.741mW$$

Note that the sum of the power dissipated by R_L and R_C equals the power dissipated by r_L in Figure 5-5. If the amplifier employed a partially bypassed emitter resistor, the unbypassed portion of the emitter resistor, R_{E1} , would also dissipate AC power. In this case, the portion of the AC output power supplied to R_L would be even less than what it is in this example.

AC INPUT POWER

In Figure 5-5 the AC power supplied by the signal source to the circuit is:

$$P = \frac{v_{IN}^2}{R_{IN}}$$

Where R_{IN} equals $R_B || R_{IN(BASE)}$.

For example, if v_{IN} is 14.3mV rms and R_{IN} is 1k Ω , the AC input power equals $(14.3mV)^2/1k\Omega$ or, approximately, 0.2 μ W.

Clearly, when you are discussing the "power" associated with a particular amplifier, it is important to distinguish between the DC input power, the AC output power, the portion of the AC output power supplied to R_L , and the AC input power.

Useful Class A Power Formulas

The DC input power equals the product of the supply voltage and the current drawn from the supply. Thus:

$$P_{DC} = V_{CC}(I_{CQ} + I_{R_1}) \approx V_{CC}I_{CQ} \quad (\text{Eq. 5-1})$$

The portion of the DC input power dissipated by the transistor under quiescent conditions is:

$$P_{DQ} = V_{CEQ}I_{CQ} \quad (\text{Eq. 5-2})$$

Recall that the remaining portion of the DC input power is dissipated in the biasing, collector, and emitter resistors.

At different portions of the AC input cycle, the transistor will dissipate power less than, equal to, and greater than the quiescent value. However, for a symmetrical input voltage, the **average power** dissipated by the transistor equals the quiescent value.

The AC output power equals $v_{CE}i_C$, where v_{CE} and i_C are rms values. Usually, when the term AC output power is used, it refers to the maximum possible AC output power. Since the maximum possible peak values of v_{CE} and i_C are V_{CEQ} and I_{CQ} respectively, we have:

$$\begin{aligned} P_{AC} &= (0.707V_{CEQ})(0.707I_{CQ}) \\ P_{AC} &= 0.5V_{CEQ}I_{CQ} \end{aligned}$$

Since $P_{DQ} = V_{CEQ}I_{CQ}$, the maximum possible AC output power, P_{AC} , is:

$$P_{AC} = 0.5P_{DQ} \quad (\text{Eq. 5-3})$$

Thus, in a class A amplifier, the maximum possible AC output power equals one-half the power dissipated by the transistor under quiescent conditions. For example, if the no signal power dissipated by the transistor is 10W, the maximum possible AC output power is 5W.

Recall that only a portion of the AC output power is supplied to the load, R_L . Assuming a fully bypassed emitter resistor, the AC output power divides between R_C and R_L as follows:

$$P_{R_L} = \frac{(V_{CEQ})^2}{2R_L} \quad (\text{Eq. 5-4})$$

$$P_{R_C} = \frac{(V_{CEQ})^2}{2R_C} \quad (\text{Eq. 5-5})$$

Finally, recall that the AC input power supplied by the signal source to the circuit, P_{IN} , is:

$$P_{IN} = \frac{(v_{IN})^2}{R_{IN}} \quad (\text{Eq. 5-6})$$

Efficiency

Efficiency is a measure of the ability of an amplifier to convert the DC input power to AC output power. The **collector efficiency** of a power amplifier is defined as follows:

$$\eta = \frac{P_{AC}}{P_{DC}} \times 100 \quad (\text{Eq. 5-7})$$

where: η = collector efficiency in percent.

P_{AC} = AC output power in watts.

P_{DC} = DC input power in watts.

For example, if $P_{AC} = 1\text{W}$ and $P_{DC} = 10\text{W}$, the collector efficiency, η , would be 10%. This means that 10% of the DC input power is converted into AC output power.

Since $P_{AC} = 0.5$, $P_{DQ} = 0.5V_{CEQ}I_{CQ}$, and $P_{DC} \approx V_{CC}I_{CQ}$, Equation 5-7 can be written as follows:

$$\eta = \frac{V_{CEQ}}{2V_{CC}} \times 100 \quad (\text{Eq. 5-8})$$

We are especially interested in how effective an amplifier is in supplying AC power to the load, R_L . Consequently, we will define **conversion efficiency**, η' , as follows:

$$\eta' = \frac{\text{AC power supplied to } R_L}{\text{DC input power}} \times 100$$

Thus:

$$\eta' = \frac{(V_{CEQ})^2}{2V_{CC}I_{CQ}R_L} \times 100 \quad (\text{Eq. 5-9})$$

Comparing Equation 5-9 with Equation 5-8 indicates:

$$\eta' = \frac{\eta V_{CEQ}}{I_{CQ}R_L}$$

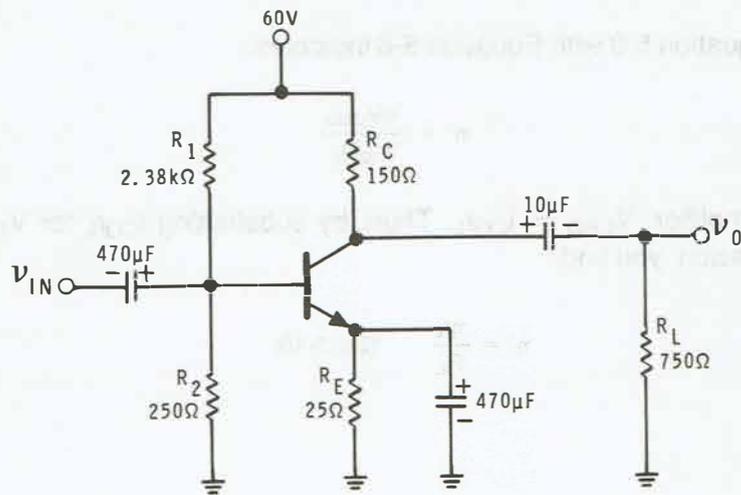
In a class A amplifier, $V_{CEQ} = I_{CQ}r_L$. Thus, by substituting $I_{CQ}r_L$ for V_{CEQ} in the previous expression, you find:

$$\eta' = \frac{\eta r_L}{R_L} \quad (\text{Eq. 5-10})$$

Example 5-1

For the class A power amplifier in Figure 5-6, work out values for the following quantities:

- A. The power dissipated by the transistor under quiescent conditions.
- B. The DC input power.
- C. The AC output power.
- D. The AC power supplied to R_L .
- E. The collector efficiency.
- F. The conversion efficiency.

**Figure 5-6**

Circuit for Example 5-1.

- A. In order to calculate P_{DQ} you must first calculate values for V_{CEQ} and I_{CQ} . Thus:

$$V_B = \frac{V_{CC}R_2}{R_1 + R_2} = \frac{60V(250\Omega)}{2.38k\Omega + 250\Omega} = 5.7V$$

$$V_E = V_B - V_{BE} = 5.7V - 0.7V = 5V$$

$$I_E = \frac{V_E}{R_E} = \frac{5V}{25\Omega} = 0.2A = I_{CQ}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$V_{CE} = 60V - 0.2A(150\Omega + 25\Omega) = 25V = V_{CEQ}$$

$$P_{DQ} = V_{CEQ}I_{CQ} = 25V(0.2A) = 5W$$

B. $P_{DC} \approx V_{CC}I_{CQ} = 60V(0.2A) = 12W$

C. $P_{AC} = 0.5P_{DQ} = 0.5(5W) = 2.5W$

D. $P_{R_L} = \frac{(V_{CEQ})^2}{2R_L} = \frac{(25V)^2}{2(750\Omega)} = 0.417W$

Note that only a small portion of the “AC output power” is supplied to R_L .

E. $\eta = \frac{V_{CEQ}}{2V_{CC}} \times 100$

$$\eta = \frac{25V}{2(60V)} \times 100 = 20.8\%$$

This indicates that 20.8% of the DC input power is converted to AC output power. Incidentally, the **theoretical maximum value** for the collector efficiency of a class A power amplifier is 25%. Therefore, the collector efficiency of the amplifier in Figure 5-6 is near the maximum possible value!

F. $\eta' = \frac{\eta r_L}{R_L}$

$$r_L = 750\Omega || 150\Omega = 125\Omega$$

$$\eta' = \frac{20.8\%(125\Omega)}{750\Omega} = 3.47\%$$

The conversion efficiency, η' , indicates that only 3.47% of the DC input power is converted into useful AC load power! As you can see, class A amplifiers are **not** very efficient.

Maximum Dissipation Hyperbola

Every transistor has maximum ratings that cannot be exceeded without damaging the transistor. For this reason, manufacturers specify the following quantities:

1. Maximum continuous collector current — $I_{C(MAX)}$.
2. Maximum collector-to-emitter voltage — $V_{CE(MAX)}$.
3. Maximum power dissipation — $P_{D(MAX)}$.

The value of $P_{D(MAX)}$ is usually specified for an ambient temperature of 25°C. For higher ambient temperatures, $P_{D(MAX)}$ must be **derated** as per the manufacturer's specifications. In addition, even if the ambient temperature is 25°C, some circuit designers will derate $P_{D(MAX)}$ by approximately 10 to 20 percent. This is done so that the transistor operates slightly below its design limit.

The various maximum ratings impose limits on the permissible, or safe, operating region of the transistor, as shown in Figure 5-7. Thus, to operate the transistor in the safe region, the Q point must lie on or below the $P_{D(MAX)}$ curve, called the maximum dissipation hyperbola, shown in Figure 5-7.

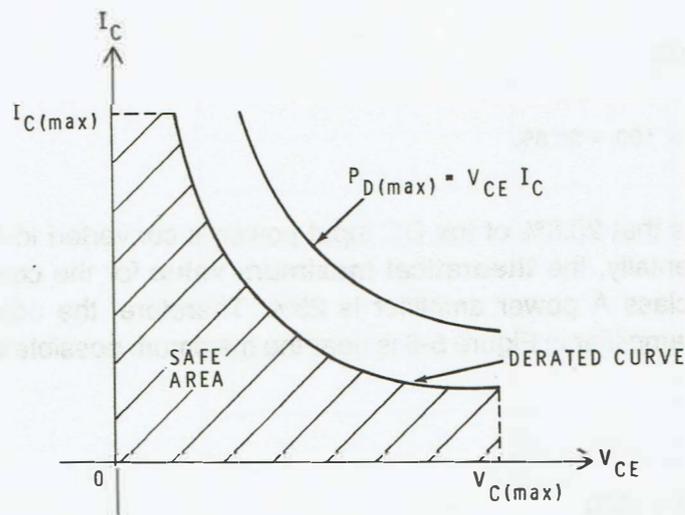


Figure 5-7

Maximum dissipation hyperbola.

Example 5-2

The data sheet for a power transistor lists the following values:

$$\begin{aligned} I_{C(\text{MAX})} &= 1.5\text{A} \\ V_{CE(\text{MAX})} &= 20\text{V} \\ P_{D(\text{MAX})} &= 1.875\text{W} \end{aligned}$$

Assuming $P_{D(\text{MAX})}$ is derated by 20%, sketch the transistor's dissipation hyperbola.

The maximum dissipation hyperbola is simply a graph of the equation $P_{D(\text{MAX})} = V_{CE}I_C$. In this example, $P_{D(\text{MAX})}$ is to be derated by 20%. Thus:

$$\begin{aligned} P'_{D(\text{MAX})} &= 0.8P_{D(\text{MAX})} \\ P'_{D(\text{MAX})} &= 0.8(1.875\text{W}) = 1.5\text{W} \end{aligned}$$

By assuming values for V_{CE} , you can calculate the corresponding values of I_C from:

$$I_C = \frac{P'_{D(\text{MAX})}}{V_{CE}} \quad (\text{Eq. 5-11})$$

For example, when $V_{CE} = 20\text{V}$, the corresponding value of I_C , which results in a power dissipation of 1.5W, is $1.5\text{W}/20\text{V}$ or 75mA. The results of similar calculations for additional values of V_{CE} are provided in Table 5-1.

V_{CE} (V)	$I_C = 1.5\text{W}/V_{CE}$ (mA)
1	1500
2	750
3	500
4	375
5	300
6	250
7	214.3
8	187.5
9	166.7
10	150
15	100
20	75

TABLE 5-1

Values of V_{CE} and I_C that result in a power dissipation of 1.5W.

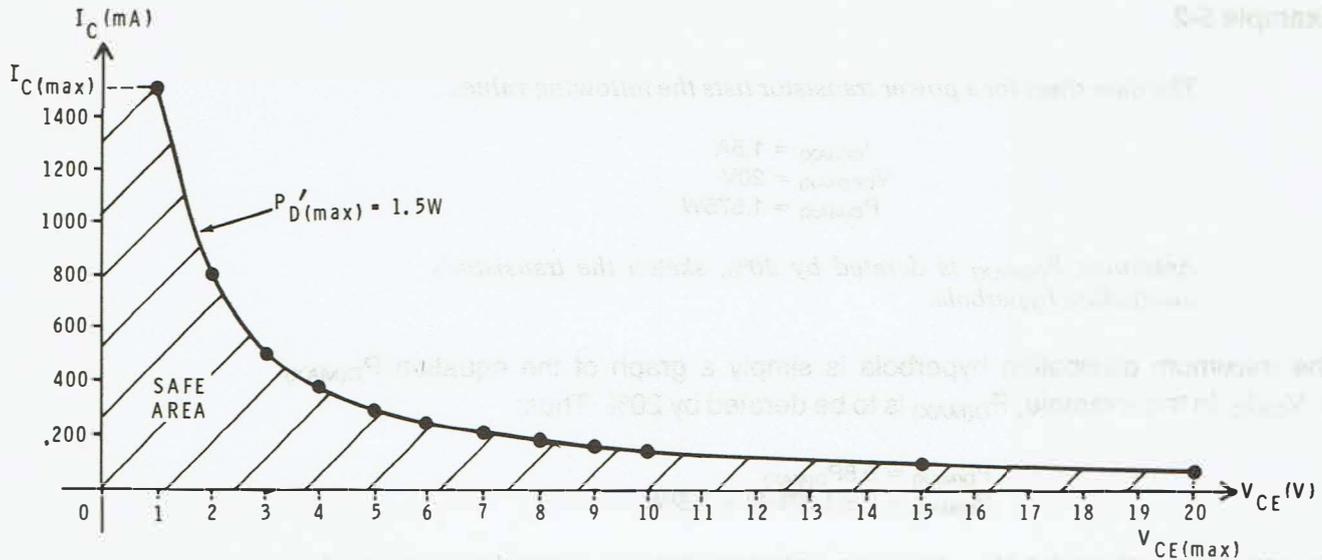


Figure 5-8

Maximum dissipation hyperbola for Example 5-2.

The power dissipation hyperbola is obtained by graphing the data in Table 5-1 as shown in Figure 5-8.

With calculus, it is possible to prove the following important points:

1. If the AC load line is tangent to the maximum dissipation hyperbola, the **maximum possible** AC output power will be obtained.
2. At the tangent point, the slope of the maximum dissipation hyperbola is the same as the slope of the AC load line, $-1/r_L$.

These concepts are graphically illustrated in Figure 5-9. Here, note that two AC load lines have been chosen so that the respective Q points, Q_1 and Q_2 , are tangent to the maximum dissipation hyperbola. Specifically:

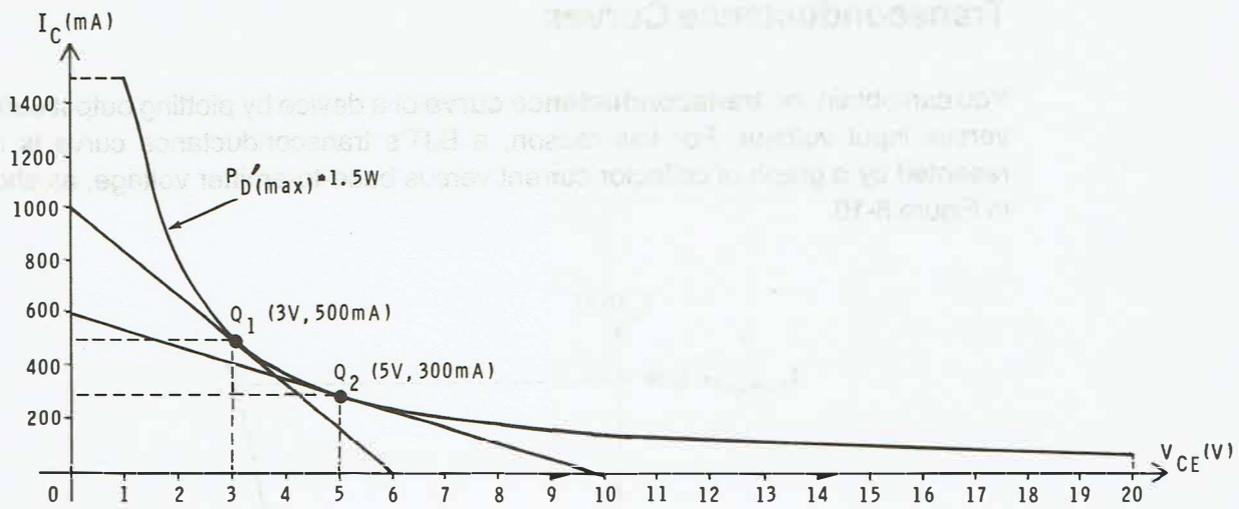


Figure 5-9

Any AC load line chosen so that it is tangent to the maximum dissipation hyperbola, at the Q point, results in the **maximum possible AC output power**. See text for details.

At Q_1 , $V_{CEQ} = 3V$ and $I_{CQ} = 500mA$.

Thus:

$$P_{DQ} = V_{CEQ}I_{CQ} = 3V(500mA) = 1.5W$$

$$P_{AC} = \frac{P_{DQ}}{2} = \frac{1.5W}{2} = 0.75W$$

Similarly, at Q_2 $V_{CEQ} = 5V$ and $I_{CQ} = 300mA$. Thus:

$$P_{DQ} = V_{CEQ}I_{CQ} = 5V(300mA) = 1.5W$$

$$P_{AC} = \frac{P_{DQ}}{2} = \frac{1.5W}{2} = 0.75W$$

In each case, the maximum possible AC output power, 0.75W, was obtained because both AC load lines were tangent to the maximum dissipation hyperbola.

The AC load resistance, r_L , corresponding to each load line in Figure 5-9, can be calculated from the Q point values as follows:

$$r_{L1} = \frac{V_{CEQ1}}{I_{CQ1}} = \frac{3V}{500mA} = 6\Omega$$

$$r_{L2} = \frac{V_{CEQ2}}{I_{CQ2}} = \frac{5V}{300mA} = 16.67\Omega$$

Transconductance Curves

You can obtain the **transconductance curve** of a device by plotting output current versus input voltage. For this reason, a BJT's transconductance curve is represented by a graph of collector current versus base-to-emitter voltage, as shown in Figure 5-10.

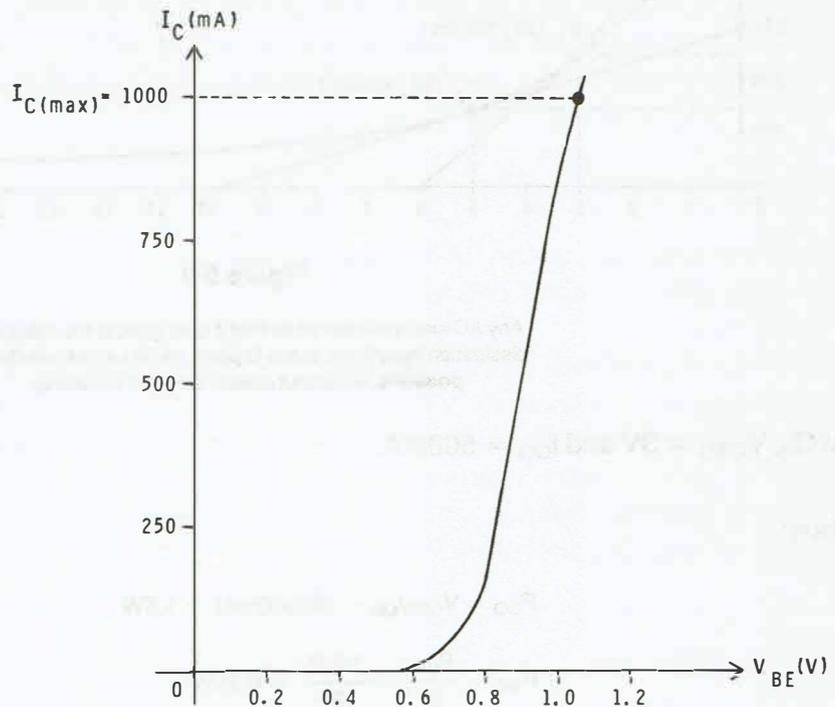


Figure 5-10

BJT transconductance curve.

At each point on the curve in Figure 5-10, the value of the BJT's **transconductance** equals the ratio of collector current to base-to-emitter voltage. It is useful to distinguish between two types of average transconductance values as follows:

SMALL SIGNAL VALUE

$$g_m = \frac{\Delta I_C}{\Delta V_{BE}} \quad (\text{Eq. 5-12})$$

Where: ΔI_C and ΔV_{BE} represent **small changes** in the collector current and collector-to-emitter voltage respectively.

LARGE SIGNAL VALUE

$$G_M = \frac{\Delta I_C}{\Delta V_{BE}} \quad (\text{Eq. 5-13})$$

Where: ΔI_C and ΔV_{BE} represents **large changes** in the collector current and collector-to-emitter voltages respectively.

Since $I_E \approx I_C$, transconductance represents the AC conductance of the emitter diode. Also, since resistance is the reciprocal of conductance, the small-signal, $r_{e'}$, and large-signal, $r_{E'}$, AC emitter diode resistances are approximately:

$$r_{e'} = \frac{1}{g_m} \quad \text{and} \quad r_{E'} = \frac{1}{G_M}$$

For a given BJT, the values of g_m and G_M are different. For this reason, the values of $r_{e'}$ and $r_{E'}$ are also different.

In small-signal amplifiers, you can estimate $r_{e'}$ without referring to the BJT's transconductance curve by using the formula $r_{e'} = 37\text{mV}/I_E$. Unfortunately, this formula is only valid for relatively small changes in I_C and V_{CE} . For large changes in I_C and V_{CE} , some circuit designers estimate the value of $r_{E'}$ as shown in Figure 5-11. Note that the changes in I_C and V_{CE} are measured between the points corresponding to 10% and 190% of I_{CQ} .

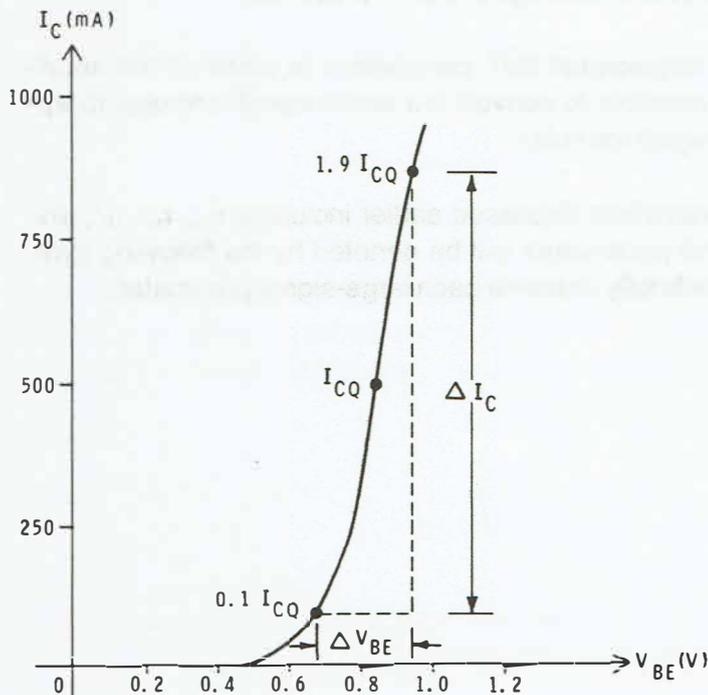


Figure 5-11

Estimating the large-signal, $r_{E'}$, AC emitter diode resistance from the BJT transconductance curve.

Example 5-3

Estimate the value of r_E' from the transconductance curve in Figure 5-11. Also estimate the value of the large-signal transconductance, G_M .

$$\Delta I_C = 1.8I_{CQ} = 1.8(500\text{mA}) = 900\text{mA}$$

$$\begin{aligned}\Delta V_{BE} &= (V_{BE} \text{ at } 1.9I_{CQ}) - (V_{BE} \text{ at } 0.1I_{CQ}) \\ \Delta V_{BE} &= 0.94\text{V} - 0.7\text{V} = 0.24\text{V}\end{aligned}$$

$$r_E' = \frac{\Delta V_{BE}}{\Delta I_C} = \frac{0.24\text{V}}{900\text{mA}} = 0.27\Omega$$

G_M is the reciprocal of r_E' . Thus:

$$G_M = \frac{1}{r_E'} = \frac{1}{0.27\Omega} = 3.7\text{S}$$

Large-Signal Parameters and Equations

The equations for gains, input resistance, and output resistance developed in Units 3 and 4 were based upon small-signal BJT models. Therefore, these formulas are **not directly applicable** to power amplifiers, where the swings in current and voltage are quite large. For this reason, some circuit designers prefer graphical methods for the analysis and design of power amplifiers.

Nevertheless, by employing large-signal BJT parameters in place of the small-signal BJT parameters, it is possible to convert the small-signal formulas to **approximate**, but useful, large-signal formulas.

The principle small-signal parameters discussed earlier included: h_{fe} , r_e' , r_b' , and r_c' . The analogous large-signal parameters will be denoted by the following symbols: h_{FE} , r_E' , r_B' , and r_C' . Let's briefly examine each large-signal parameter.

h_{FE} — In a class A power amplifier, the maximum peak-to-peak value of the collector current is, approximately, $1.9I_{CQ} - 0.1I_{CQ}$ or $1.8I_{CQ}$. For this reason, we will assume the large-signal value of h_{FE} corresponds to the value of h_{FE} at $I_C = 1.8I_{CQ}$.

$r_{E'}$ — As demonstrated previously, $r_{E'}$ is estimated from the BJT's transconductance curve between $I_C = 0.1I_{CQ}$, and $I_C = 1.9I_{CQ}$. Specifically,

$$r_{E'} = \frac{1}{G_M} = \frac{\Delta V_{BE}}{1.8I_{CQ}}$$

$r_{B'}$ — This is the large-signal base spreading resistance. For large values of I_B , the $I_B r_{B'}$ voltage drop may be neglected if $r_{B'} \leq \frac{h_{FE} r_{E'}}{10}$. If $r_{B'}$ is significant, the effective voltage gain will be decreased. Frequently, values for $r_{B'}$ are best determined experimentally.

$r_{C'}$ — In a typical power amplifier, $r_{C'}$ is much larger than r_L . Consequently, $r_{C'} \parallel r_L \approx r_L$. For this reason, $r_{C'}$ can usually be neglected.

Assuming $r_{B'}$ and $r_{C'}$ are negligible, the small-signal formulas can be converted to approximate large-signal formulas by:

1. Replacing r_e with $r_{E'}$.
2. Replacing h_{fe} with h_{FE} .

Example 5-4

The power amplifier in Figure 5-6 was partially analyzed in Example 5-1. Recall that $I_{CQ} = 0.2A$, and $r_L = 125\Omega$. Assuming r_B' and r_C' are negligible, estimate the amplifier's voltage gain and input resistance.

For a comparable small-signal amplifier:

$$A_V = \frac{-r_L}{r_{e'}} \quad \text{and} \quad R_{IN} = R_1 \parallel R_2 \parallel h_{fe} r_{e'}$$

Thus, the analogous large-signal equations are:

$$A_V = \frac{-r_L}{r_{E'}} \quad \text{and} \quad R_{IN} = R_1 \parallel R_2 \parallel h_{FE} r_{E'}$$

Values for the large-signal parameters, $r_{E'}$ and h_{FE} , are obtained as follows:

$$I_{CQ} = 0.2A = 200mA$$

$$0.1I_{CQ} = 0.1(200mA) = 20mA$$

$$1.9I_{CQ} = 1.9(200mA) = 380mA$$

$$\Delta I_C = 1.8I_{CQ} = 1.8(200mA) = 360mA$$

Referring to the transconductance curve in Figure 5-12A:

$$r_{E'} = \frac{\Delta V_{BE}}{\Delta I_C} = \frac{0.82V - 0.68V}{360mA} = 0.39\Omega$$

From Figure 5-12B, we note that the value of h_{FE} corresponding to $1.8I_{CQ}$, 360mA, is 55. Thus:

$$A_V = \frac{-r_L}{r_{E'}} = \frac{-125\Omega}{0.39\Omega} \approx -321$$

$$R_{IN} = R_1 \parallel R_2 \parallel h_{FE} r_{E'}$$

$$R_{IN} = 2.38k\Omega \parallel 250\Omega \parallel 55(0.39\Omega)$$

$$R_{IN} = 226.2\Omega \parallel 21.45\Omega = 19.6\Omega$$

Note that the input resistance of a class A, common-emitter, power amplifier is quite low.

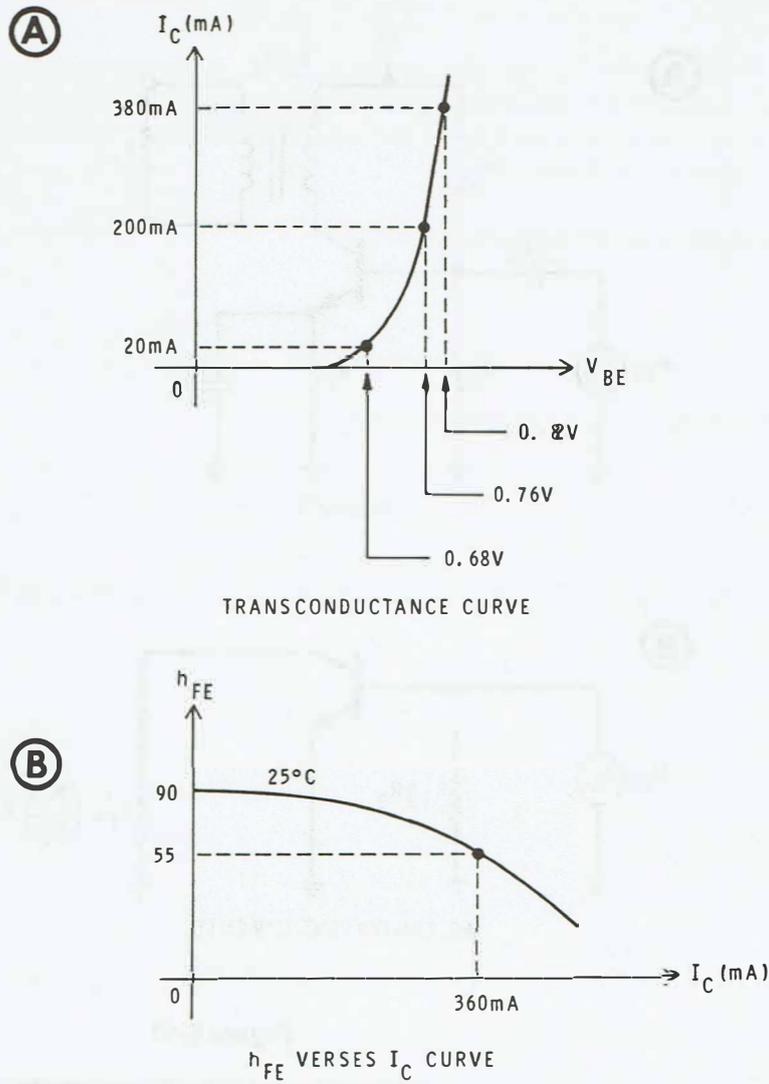


Figure 5-12

Estimating the large-signal parameters, $r_{E'}$ and h_{FE} , for Example 5-4.

- A. Transconductance curve.
- B. h_{FE} versus I_C curve.

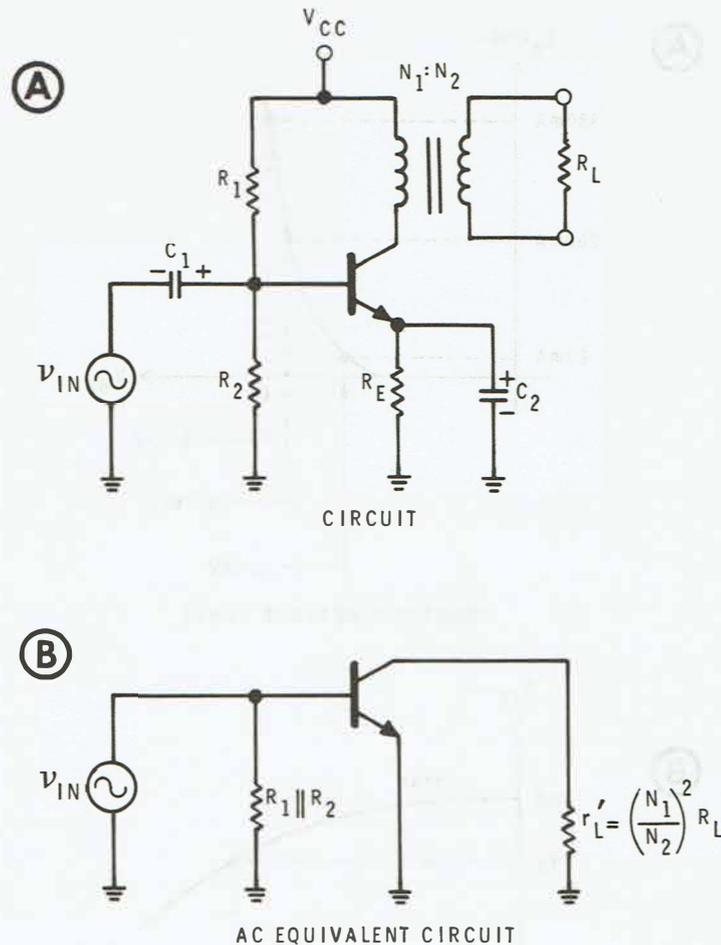


Figure 5-13

Transformer-coupled, class A power amplifier.

- A. Circuit.
B. AC equivalent circuit.

Transformer Coupled Amplifier

Class A power amplifiers can be transformer coupled, as shown in Figure 5-13A. The AC equivalent circuit is provided in Figure 5-13B. Here, note that the **effective AC load resistance**, r'_L , equals the square of the transformer turns ratio times the actual load resistance, r_L .

The principle advantage of a transformer-coupled class A amplifier is increased efficiency. In fact, the theoretical maximum value of the collector efficiency of such an amplifier approaches 50% — or double the value of a comparable RC coupled amplifier. The following example illustrates the analysis of a class A, transformer-coupled, power amplifier.

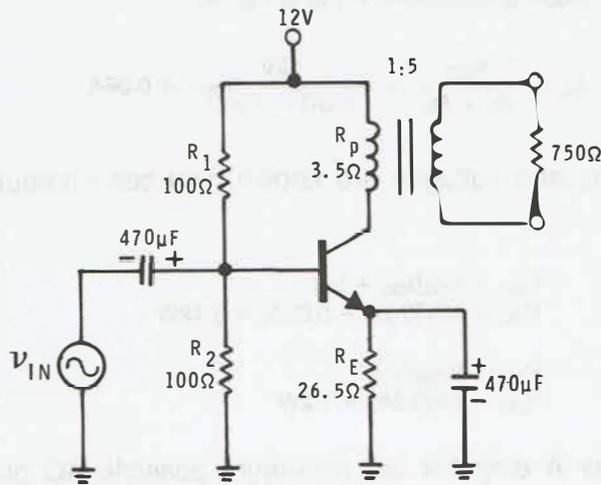


Figure 5-14

Circuit for Example 5-5.

Example 5-5

For the circuit in Figure 5-14, calculate the collector efficiency, conversion efficiency, and power supplied to the 750Ω load. Assume the transformer has a primary resistance of 3.5Ω, and an efficiency of 69.5%.

Begin by calculating the DC currents and voltages.

$$V_B = \frac{12V(100\Omega)}{100\Omega + 100\Omega} = 6V$$

$$V_E = V_B - V_{BE} = 6V - 0.7V = 5.3V$$

$$I_E = \frac{V_E}{R_E} = \frac{5.3V}{26.5\Omega} = 0.2A = I_{CQ}$$

The DC collector-to-ground voltage, V_C , equals the supply voltage minus the drop across the primary resistance of the transformer. Thus:

$$V_C = V_{CC} - I_C R_P$$

$$V_C = 12V - 0.2A(3.5\Omega) = 11.3V$$

$$V_{CE} = V_C - V_E$$

$$V_{CE} = 11.3V - 5.3V = 6V$$

The DC current in the biasing resistors, R_1 and R_2 , is:

$$I_{R_1} = \frac{V_{CC}}{R_1 + R_2} = \frac{12V}{100\Omega + 100\Omega} = 0.06A$$

Once the DC currents and voltages are known, you can compute the various powers as follows:

$$P_{DC} = V_{CC}[I_{CQ} + I_{R_1}]$$

$$P_{DC} = 12V[0.2A + 0.06A] = 3.12W$$

$$P_{DQ} = V_{CEQ}I_{CQ}$$

$$P_{DQ} = 6V(0.2A) = 1.2W$$

Recall that in a class A amplifier the maximum possible AC output power is one-half P_{DQ} . Thus:

$$P_{AC} = \frac{P_{DQ}}{2} = \frac{1.2W}{2} = 0.6W$$

Since the maximum possible AC output power is 0.6W and the DC input power is 3.12W, the collector efficiency is:

$$\eta = \frac{P_{AC}}{P_{DC}} \times 100$$

$$\eta = \frac{0.6W}{3.12W} \times 100 = 19.2\%$$

Similarly, since the transformer has an efficiency, η_t , of 69.5%, the portion of the AC output power supplied to the load is:

$$P_{r_L} = \eta_t P_{AC}$$

$$P_{r_L} = 69.5\%(0.6W) \quad (\text{Eq. 5-14})$$

$$P_{r_L} = 0.417W$$

Thus, the conversion efficiency, η' is:

$$\eta' = \frac{P_{r_L}}{P_{DC}} \times 100$$

$$\eta' = \frac{0.417W}{3.12W} \times 100 = 13.4\%$$

Comparing the results of Example 5-5 with those obtained in Example 5-1, we note that the transformer-coupled design has a significantly larger conversion efficiency. Disadvantages of the transformer-coupled design include the size, cost, and bulk of the transformer. In addition, the frequency response of the amplifier is limited by the frequency characteristics of the transformer.

Designing Class A Power Amplifiers

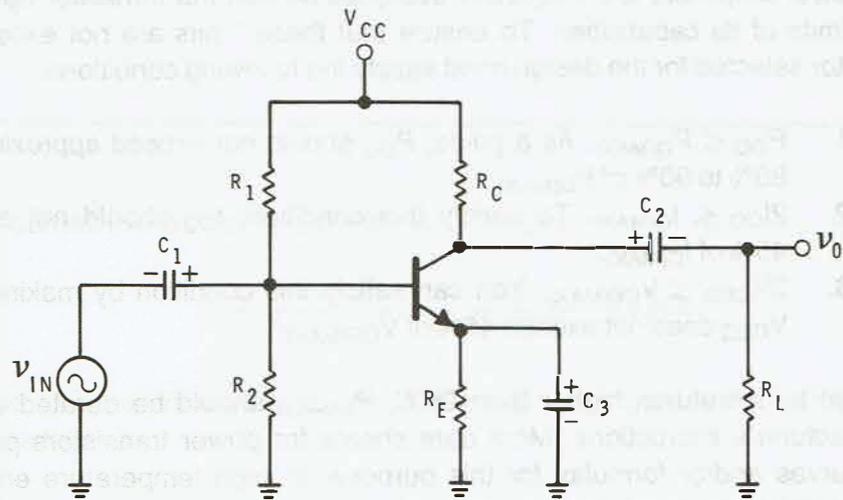
Class A power amplifiers are frequently designed so that the transistor operates near the limits of its capabilities. To ensure that these limits are not exceeded, the transistor selected for the design must satisfy the following conditions:

1. $P_{DQ} \leq P_{D(MAX)}$. As a guide, P_{DQ} should not exceed approximately 80% to 90% of $P_{D(MAX)}$.
2. $2I_{CQ} \leq I_{C(MAX)}$. To satisfy this condition, I_{CQ} should not exceed 45% of $I_{C(MAX)}$.
3. $2V_{CEQ} \leq V_{CE(MAX)}$. You can satisfy this condition by making sure V_{CEQ} does not exceed 45% of $V_{CE(MAX)}$.

For ambient temperatures higher than 25°C, $P_{D(MAX)}$ should be derated as per the manufacturer's instructions. Most data sheets for power transistors provide derating curves and/or formulas for this purpose. In high temperature environments, heat sinks and/or cooling fans may be required to remove excessive heat.

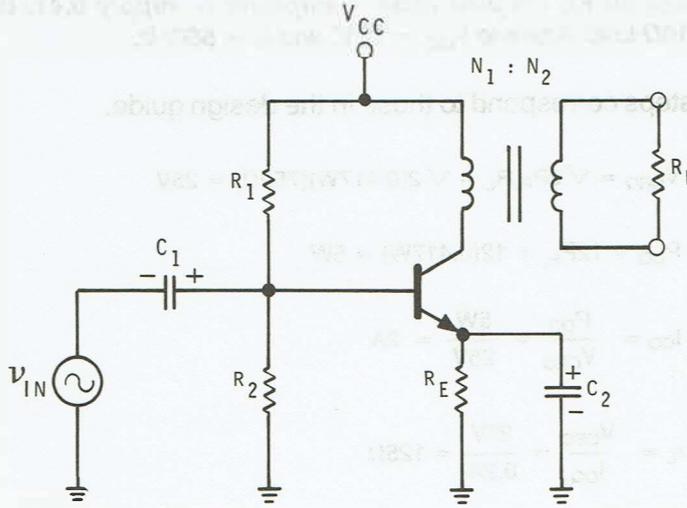
The following design guides and examples should help you in designing elementary class A power amplifiers.

RC COUPLED CLASS A POWER AMPLIFIER



1. Calculate V_{CEQ} $V_{CEQ} = \sqrt{2P_{R_L}R_L}$
2. Calculate P_{DQ} $P_{DQ} = 8 \text{ to } 12 \text{ times } P_{R_L}$
3. Calculate I_{CQ} $I_{CQ} = \frac{P_{DQ}}{V_{CEQ}}$
4. Calculate r_L $r_L = \frac{V_{CEQ}}{I_{CQ}}$
5. Calculate R_C $R_C = \frac{R_L r_L}{R_L - r_L}$
6. Calculate V_{EQ} $V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CEQ}]$
7. Calculate R_E $R_E = \frac{V_{EQ}}{I_{CQ}}$
8. Calculate R_2 $R_2 \leq 10R_E$
9. Calculate R_1 $R_1 = \frac{R_2 [V_{CC} - V_{BQ}]}{V_{BQ}}$
10. Select transistor, calculate resistor wattages.
11. Select capacitors $C_1 \geq \frac{3.18}{f_1 R_{IN}}, C_2 \geq \frac{3.18}{f_1 R_L}$
 $C_3 \geq \frac{3.18}{f_1 R_E}$

TRANSFORMER COUPLED CLASS A POWER AMPLIFIER



1. Calculate P_{AC} $P_{AC} = \frac{P_{R_L}}{\eta_t}$
2. Calculate P_{DQ} $P_{DQ} = 2 P_{AC}$
3. Select I_{CQ} $I_{CQ} \approx 0.1A \text{ to } 1A$
4. Calculate V_{CEQ} $V_{CEQ} = \frac{P_{DQ}}{I_{CQ}}$
5. Calculate r_L $r_L = \frac{V_{CEQ}}{I_{CQ}}$
6. Calculate $\frac{N_1}{N_2}$ $\frac{N_1}{N_2} = \sqrt{\frac{r_L}{R_L}}$
7. Calculate V_{EQ} $V_{EQ} = V_{CC} - [I_{CQ}R_P + V_{CEQ}]$
8. Calculate R_E $R_E = \frac{V_{EQ}}{I_{CQ}}$
9. Select R_2 $R_2 \leq 10R_E$
10. Calculate R_1 $R_1 = \frac{R_2[V_{CC} - V_{BQ}]}{V_{BQ}}$
11. Select transistor, calculate resistor wattages.
12. Select capacitors $C_1 \geq \frac{3.18}{f_1 R_{IN}} \quad C_2 \geq \frac{3.18}{f_1 R_E}$

Example 5-6

Design an RC coupled class A amplifier to supply 0.417W to a 750Ω load. Assume $V_{CC} = 60V$, and $f_i = 500Hz$.

The following steps correspond to those in the design guide.

$$1. \quad V_{CEQ} = \sqrt{2P_{R_L}R_L} = \sqrt{2(0.417W)(750\Omega)} = 25V$$

$$2. \quad P_{DQ} = 12P_{R_L} = 12(0.417W) = 5W$$

$$3. \quad I_{CQ} = \frac{P_{DQ}}{V_{CEQ}} = \frac{5W}{25V} = .2A$$

$$4. \quad r_L = \frac{V_{CEQ}}{I_{CQ}} = \frac{25V}{0.2A} = 125\Omega$$

$$5. \quad R_C = \frac{R_L r_L}{R_L - r_L} = \frac{750\Omega(125\Omega)}{750\Omega - 125\Omega} = 150\Omega$$

$$6. \quad V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CEQ}]$$

$$V_{EQ} = 60V - [0.2A(150\Omega) + 25V]$$

$$V_{EQ} = 60V - 55V = 5V$$

$$7. \quad R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{5V}{0.2A} = 25\Omega$$

$$8. \quad \text{Select } R_2 = 10R_E = 10(25\Omega) = 250\Omega$$

$$9. \quad R_1 = \frac{R_2[V_{CC} - V_{BQ}]}{V_{BQ}}$$

Since $V_{EQ} = 5V$, $V_{BQ} = 5V + 0.7V$ or $5.7V$. Thus:

$$R_1 = \frac{250\Omega[60V - 5.7V]}{5.7V} = 2.38k\Omega$$

$$10. \quad \text{Assuming } P_{DQ} \text{ is } 80\% \text{ of } P_{D(\text{MAX})}$$

$$P_{D(\text{MAX})} \geq \frac{P_{DQ}}{0.8}$$

$$P_{D(\text{MAX})} \geq \frac{5W}{0.8} \geq 6.25W$$

Similarly, assuming I_{CQ} and V_{CEQ} at 40% of $I_{C(MAX)}$ and $V_{CE(MAX)}$ respectively:

$$I_{C(MAX)} \geq \frac{I_{CQ}}{0.4}$$

$$I_{C(MAX)} \geq \frac{.2A}{.4} \geq 0.5A$$

$$V_{CE(MAX)} \geq \frac{V_{CEQ}}{0.4}$$

$$V_{CE(MAX)} \geq \frac{25V}{0.4} \geq 62.5V$$

Thus, the transistor selected for the design should have the following maximum ratings:

$$P_{D(MAX)} \geq 6.25W$$

$$I_{C(MAX)} \geq 0.5A$$

$$V_{CE(MAX)} \geq 62.5V$$

You can compute the power dissipated by various resistors as follows:

$$I_{R_1} = I_{R_2} = \frac{V_{CC}}{R_1 + R_2} = \frac{60V}{2.38k\Omega + 250\Omega} = 22.8mA$$

$$P_{R_1} = (22.8mA)^2(2.38k\Omega) = 1.24W$$

$$P_{R_2} = (22.8mA)^2(250\Omega) = 0.13W$$

$$I_{R_C} \approx I_{R_E} = I_{CQ} = 0.2A$$

$$P_{R_C} = (0.2A)^2(150\Omega) = 6W$$

$$P_{R_E} = (0.2A)^2(25\Omega) = 1W$$

11. Once the transistor has been selected, you can estimate r_E' , h_{FE} , and R_{IN} as shown in Example 5-4. Assuming $R_{IN} = 19.6\Omega$, the minimum capacitor values are:

$$C_1 = \frac{3.18}{f_1 R_{IN}} = \frac{3.18}{500(19.6\Omega)} = 324.5\mu F$$

$$C_2 = \frac{3.18}{f_1 R_L} = \frac{3.18}{500(750\Omega)} = 8.5\mu F$$

$$C_3 = \frac{3.18}{f_1 R_E} = \frac{3.18}{500(25\Omega)} = 254.4\mu F$$

Example 5-7

Design a transformer-coupled class A amplifier to supply 0.417W to a 750Ω load. Assume $V_{CC} = 12V$ and $f_i = 500Hz$.

Following the steps in the design guide, you proceed as follows:

$$1. \quad P_{AC} = \frac{P_{RL}}{\eta_t}$$

For this example, we will assume the transformer has an efficiency of 69.5% and a primary resistance of 3.5Ω. Thus:

$$P_{AC} = \frac{0.417W}{0.695} = 0.6W$$

$$2. \quad P_{DQ} = 2P_{AC} = 2(0.6W) = 1.2W$$

3. As a guide, for relatively small class A power amplifiers we will select I_{CQ} to be between 0.1A and 1A somewhat arbitrarily. Then we select $I_{CQ} = 0.2A$.

$$4. \quad V_{CEQ} = \frac{P_{DQ}}{I_{CQ}} = \frac{1.2W}{0.2A} = 6V$$

$$5. \quad r_L = \frac{V_{CEQ}}{I_{CQ}} = \frac{6V}{0.2A} = 30\Omega$$

6. In order to “match” the 750Ω load resistance to the 30Ω AC load resistance seen by the transistor, the required turns ratio is:

$$\frac{N_1}{N_2} = \sqrt{\frac{r_L}{R_L}} = \sqrt{\frac{30\Omega}{750\Omega}} = \sqrt{0.04} = 0.2$$

Thus, $\frac{N_1}{N_2} = \frac{0.2}{1}$, which is equivalent to a 1:5 turns ratio.

$$7. \quad \begin{aligned} V_{EQ} &= V_{CC} - [I_{CQ}R_P + V_{CEQ}] \\ V_{EQ} &= 12V - [0.2A(3.5\Omega) + 6V] \\ V_{EQ} &= 12V - 6.7V = 5.3V \end{aligned}$$

$$8. \quad R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{5.3V}{0.2A} = 26.5\Omega$$

9. $R_2 \leq 10R_E$. A 100Ω resistor would be acceptable. Thus, $R_2 = 100\Omega$.

$$10. R_1 = \frac{R_2[V_{CC} - V_{BQ}]}{V_{BQ}}$$

Since $V_{EQ} = 5.3V$, $V_{BQ} = 5.3V + 0.7V = 6V$. Thus,

$$R_1 = \frac{100\Omega[12V - 6V]}{6V} = 100\Omega$$

11. Using the same guidelines provided earlier:

$$P_{D(MAX)} \geq \frac{P_{DQ}}{0.8} \geq \frac{1.2W}{0.8} \geq 1.5W$$

$$I_{C(MAX)} \geq \frac{I_{CQ}}{0.4} \geq \frac{0.2A}{0.4} \geq 0.5A$$

$$V_{CE(MAX)} = \frac{V_{CEQ}}{0.4} = \frac{6V}{0.4} = 15V$$

The powers dissipated by the various resistors are obtained as before. Specifically:

$$I_{R_1} = I_{R_2} = \frac{V_{CC}}{R_1 + R_2} = \frac{12V}{100\Omega + 100\Omega} = 0.06A$$

$$P_{R_1} = (0.06A)^2(100\Omega) = 0.36W = P_{R_2}$$

$$I_{R_E} \approx I_{CQ} = 0.2A$$

$$P_{R_E} = (0.2A)^2(26.5\Omega) = 1.06W$$

12. To calculate R_{IN} , you would first estimate the values of r_E' and h_{FE} from the transistor's data sheet. Assuming $R_{IN} = 25\Omega$, the minimum capacitor values are:

$$C_1 = \frac{3.18}{f_1 R_{IN}} = \frac{3.18}{500(25\Omega)} = 254.4\mu F$$

$$C_2 = \frac{3.18}{f_1 R_E} = \frac{3.18}{500(26.5\Omega)} = 240\mu F$$

Self-Test Review

1. The large-signal value of h_{FE} is measured at $I_C \approx$ _____ I_{CQ} .
2. To obtain $r_{E'}$, ΔV_{BE} and ΔI_C are measured between $I_C =$ _____ I_{CQ} and $I_C =$ _____ I_{CQ} .
3. A transconductance curve is a plot of output _____ versus input _____.
4. Conversion efficiency is _____ than the collector efficiency.
(larger/smaller)
5. A transformer coupled class A amplifier is _____ efficient than an RC Coupled class A amplifier.
(more/less)

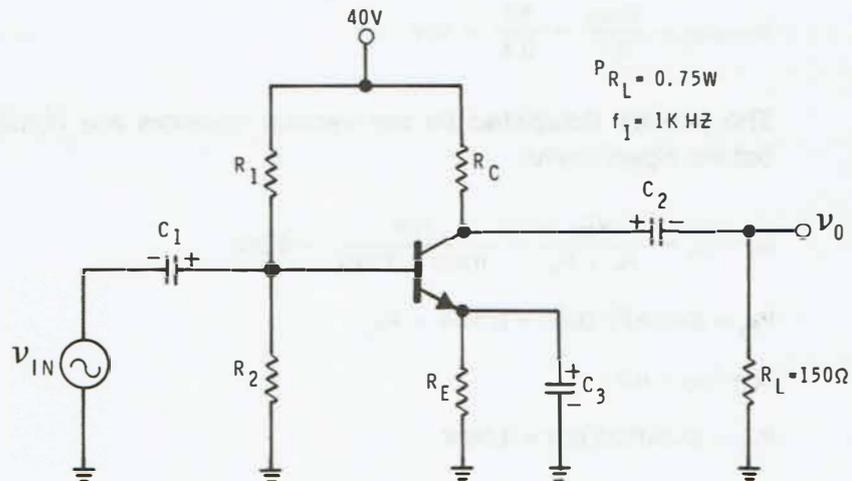


Figure 5-15

Circuit for Self-Test Review questions 6 to 15.

Refer to Figure 5-15 for questions 6 to 15.

6. V_{CEQ} should equal _____ V.
7. The quiescent power dissipated by the transistor is _____ W.
8. R_C should equal approximately _____ Ω .

9. R_E should equal approximately _____ Ω .
10. If $R_2 = 100\Omega$, R_1 should equal _____ Ω .
11. Assuming 20% derating factors, the maximum transistor ratings should equal or exceed the following values:
- $P_{D(MAX)} =$ _____ W.
- $I_{C(MAX)} =$ _____ A.
- $V_{CE(MAX)} =$ _____ V.
12. The collector efficiency is approximately _____ %.
13. The conversion efficiency is approximately _____ %.
14. Assuming ΔV_{BE} obtained from the transistor's transconductance curve is 0.5V, $r_{E'}$ is approximately _____ Ω .
15. Assuming h_{FE} at $I_C = 1.08A$ equals 80, the minimum value of C_1 is _____ μF .

Answers

- | | |
|---------------------|-------------------------|
| 1. $1.8I_{CQ}$ | 9. 11.67Ω |
| 2. 0.1, and 1.9 | 10. 419.5Ω |
| 3. current, voltage | 11. 11.25W, 1.5A, 37.5V |
| 4. smaller | 12. 18.75% |
| 5. more | 13. 3.125% |
| 6. 15V | 14. 0.463Ω |
| 7. 9W | 15. $125.2\mu\text{F}$ |
| 8. 30Ω | |

The solutions to questions 6 through 15 follow.

$$6. \quad V_{CEQ} = \sqrt{2P_{R_L}R_L} = \sqrt{2(0.75\text{W})(150\Omega)} = 15\text{V}$$

$$7. \quad P_{DQ} = 12P_{R_L} = 12(0.75\text{W}) = 9\text{W}$$

8. First calculate I_{CQ} and r_L .

$$I_{CQ} = \frac{P_{DQ}}{V_{CEQ}} = \frac{9\text{W}}{15\text{V}} = 0.6\text{A}$$

$$r_L = \frac{V_{CEQ}}{I_{CQ}} = \frac{15\text{V}}{0.6\text{A}} = 25\Omega$$

Since $R_C = \frac{R_L r_L}{R_L - r_L}$ you have:

$$R_C = \frac{150\Omega(25\Omega)}{150\Omega - 25\Omega} = 30\Omega$$

$$9. \quad \begin{aligned} V_{EQ} &= V_{CC} - [I_{CQ}R_C + V_{CEQ}] \\ V_{EQ} &= 40\text{V} - [0.6\text{A}(30\Omega) + 15\text{V}] \\ V_{EQ} &= 40\text{V} - 33\text{V} = 7\text{V} \end{aligned}$$

$$R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{7\text{V}}{0.6\text{A}} = 11.67\Omega$$

10. Since $V_{EQ} = 7V$, $V_{BQ} = 7V + 0.7V = 7.7V$.

$$R_1 = \frac{R_2[V_{CC} - V_{BQ}]}{V_{BQ}} = \frac{100\Omega[40V - 7.7V]}{7.7V} = 419.5\Omega$$

11. $P_{D(MAX)} \geq \frac{P_{DQ}}{0.8} \geq \frac{9W}{0.8} \geq 11.25W$

$$I_{C(MAX)} \geq \frac{I_{CQ}}{0.4} \geq \frac{0.6A}{0.4} \geq 1.5A$$

$$V_{CE(MAX)} \geq \frac{V_{CEQ}}{0.4} \geq \frac{15V}{0.4} \geq 37.5V$$

12. $\eta = \frac{V_{CEQ}}{2V_{CC}} \times 100 = \frac{15V}{2(40V)} \times 100 = 18.75\%$

13. $\eta' = \frac{\eta r_L}{R_L} = \frac{18.75\%(25\Omega)}{150\Omega} = 3.125\%$

14. $r_{E'} = \frac{\Delta V_{BE}}{\Delta I_C} = \frac{\Delta V_{BE}}{1.8I_{CQ}}$

Since $\Delta V_{BE} = 0.5V$ and $I_{CQ} = 0.6A$,

$$r_{E'} = \frac{0.5V}{1.8(0.6A)} = 0.463\Omega$$

15. Since $r_{E'} = 0.463\Omega$ and $h_{FE} = 80$, the input resistance looking into the base is:

$$R_{IN(BASE)} = h_{FE}r_{E'} = 80(0.463\Omega) = 37.04\Omega$$

Thus, the total input resistance is:

$$R_{IN} = R_1 \parallel R_2 \parallel R_{IN(BASE)}$$

$$R_{IN} = 419.5\Omega \parallel 100\Omega \parallel 37.04\Omega$$

$$R_{IN} = 80.75\Omega \parallel 37.04\Omega \approx 25.4\Omega$$

Hence, the minimum value of C_1 is:

$$C_1 = \frac{3.18}{f_1 R_{IN}} = \frac{3.18}{1k(25.4\Omega)} = 125.2\mu F$$

DISTORTION, CLASS B, CLASS AB, AND CLASS C AMPLIFIERS

Distortion is present in an amplifier whenever the output signal is not a faithful reproduction of the input signal. In this section, we will discuss nonlinear distortion and crossover distortion.

In addition, we will discuss the characteristics of class B, class AB, and class C power amplifiers. Due to its simplicity and popularity, the class AB complementary-symmetry amplifier will be discussed in detail.

Nonlinear Distortion

An amplifier exhibits **nonlinear distortion** whenever the shape of the output signal differs from the shape of the input signal. Due to the nonlinear characteristics of the amplifying device, some nonlinear distortion is present in all classes of amplifiers.

The nonlinear characteristics inherent in a transistor are illustrated by the transistor's transconductance curve shown in Figure 5-16. Note that the nonlinear regions are most pronounced at the lower and upper ends of the curve. For this reason, nonlinear distortion is most evident for large signal swings in I_C and V_{BE} .

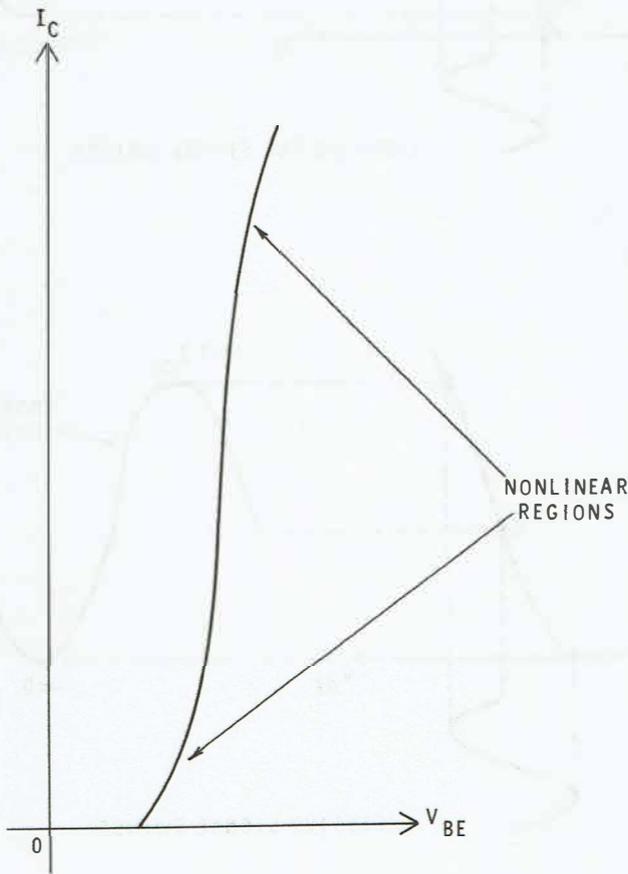


Figure 5-16

Nonlinear regions on a BJT's transconductance curve.

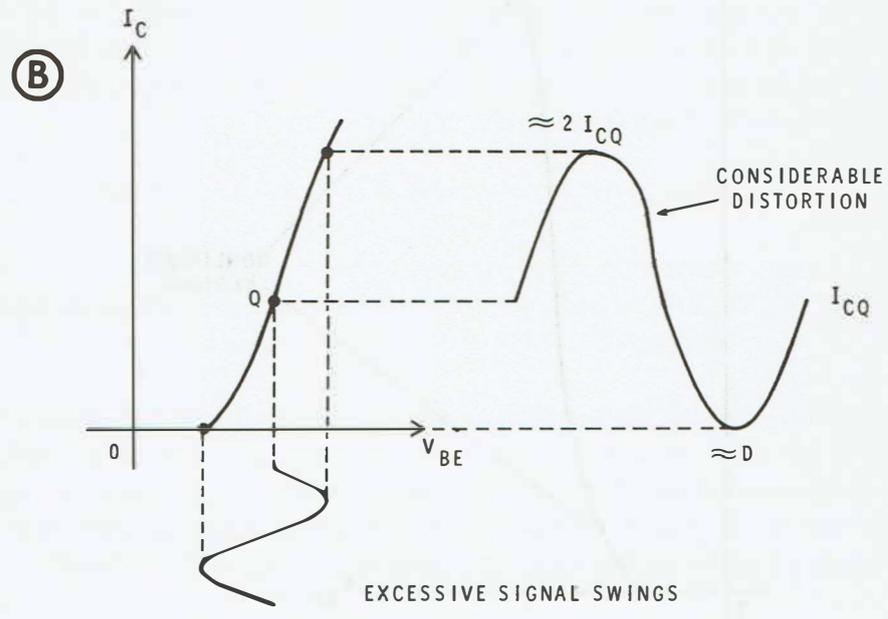
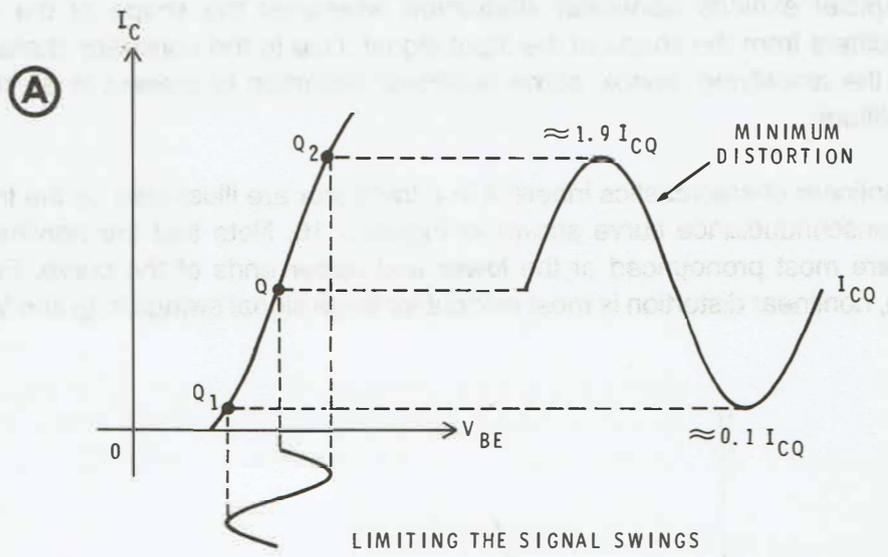


Figure 5-17

Nonlinear distortion in a class A amplifier.
 A. Limiting the signal swings.
 B. Excessive signal swings.

This concept is illustrated in Figure 5-17. In a class A amplifier, nonlinear distortion is minimized by limiting the peak input voltage as shown in Figure 5-17A. In this case, the instantaneous operating points Q_1 and Q_2 correspond approximately to collector current values of $0.1I_{CQ}$ and $1.9I_{CQ}$ respectively. This restricts the signal swings to the most linear region of the curve. Because of this, the AC collector current and AC output voltage have essentially the same shape as the AC input voltage.

If the AC input voltage is excessively large, the signal swings extend into the nonlinear portions of the curve, as shown in Figure 5-17B. In this case, both the AC collector current and AC output voltage will be distorted.

The disadvantage of limiting the signal swings, as in Figure 5-17A, is that the maximum possible AC output power is reduced. Therefore, the actual limits imposed upon the signal swings represent a power/distortion trade-off.

Describing Nonlinear Distortion

A complex wave is one that is periodic, and not sinusoidal. For this reason, a **distorted** sine wave represents a complex wave. Fourier's theorem states that complex waves can be described by the sum of a constant value and a harmonic series of sinusoids. Stated mathematically:

$$v(t) = V_0 + V_1 \cos \omega t + V_2 \cos 2\omega t + \dots V_n \cos n\omega t \quad (\text{Eq. 5-15})$$

Where: $v(t)$ = Equation of the complex wave,
 $V_1, V_2, \dots V_n$ = peak values of the various harmonic components.
 V_0 = Average DC value of the complex wave.

Viewed in this manner, the output waveform in Figure 5-17B is distorted because the nonlinear characteristics of the transistor introduce frequency components in the output waveform that are not present in the input waveform. Naturally, the amount of nonlinear, or **harmonic**, distortion depends upon the relative amplitudes of the various harmonic components. Stated mathematically:

$$D_2 = \left| \frac{V_2}{V_1} \right| \times 100 \quad (\text{Eq. 5-16})$$

$$D_3 = \left| \frac{V_3}{V_1} \right| \times 100 \quad (\text{Eq. 5-17})$$

$$D_n = \left| \frac{V_n}{V_1} \right| \times 100 \quad (\text{Eq. 5-18})$$

Where D_2 , D_3 , D_n represent the percent harmonic distortion of the various components.

You can measure the amplitudes of the harmonic components with an instrument called a **spectrum analyzer**. Physically, a spectrum analyzer resembles an oscilloscope. However, rather than plotting the measured waveform versus time, the display of a spectrum analyzer appears as shown in Figure 5-18. Here, the “frequency spectrum” of the measured waveform tells you at a glance what frequencies are contained in the waveform, and the amplitude of each harmonic component.

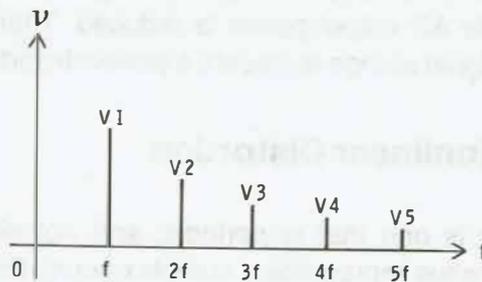


Figure 5-18

Frequency spectrum of a complex wave.

Example 5-8

A 1kHz sinusoid is amplified by a power amplifier as shown in Figure 5-19A. The output voltage is an amplified, but distorted, version of the input voltage.

To determine the amount of harmonic distortion, the output voltage is measured with a spectrum analyzer. The resulting frequency spectrum is shown in Figure 5-19B. Based on this information, calculate the percent of second, third, and fourth harmonic distortion contained in the output voltages.

The frequency of the input signal is termed the **fundamental frequency**. If no harmonic distortion is present in the output signal, the only frequency component in the output signal will be the fundamental frequency, or 1kHz in this example.

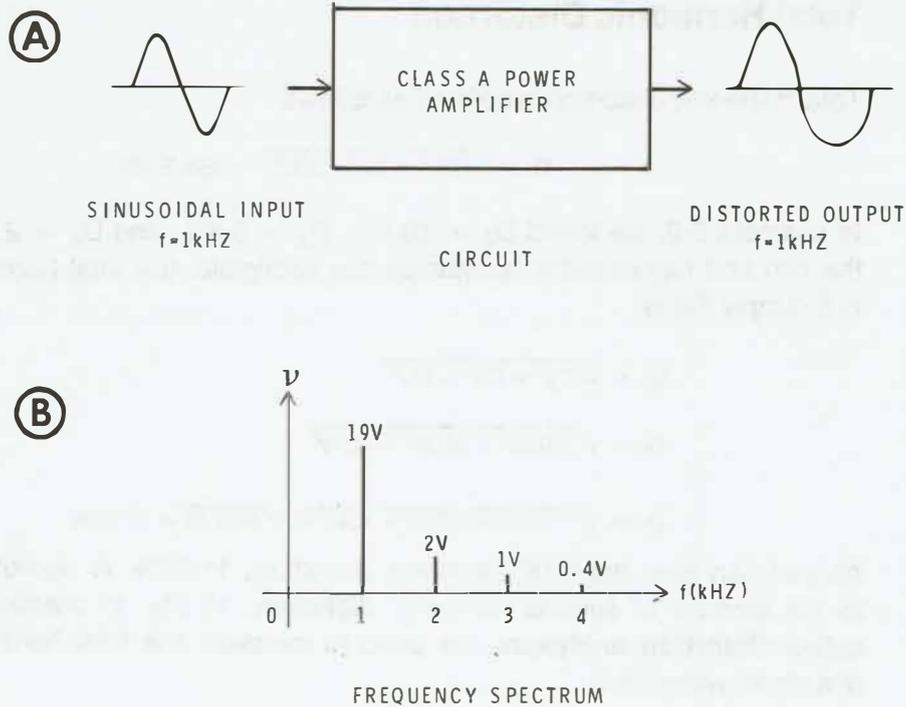


Figure 5-19

Circuit and frequency spectrum for Example 5-8.

- A. Circuit.
B. Frequency spectrum.

Figure 5-19B indicates that, in addition to the 1kHz fundamental component, the output signal contains 2kHz, 3kHz, and 4kHz harmonic components. The ratio of each harmonic component to the fundamental component determines the amount of harmonic distortion. Specifically:

$$D_2 = \left| \frac{V_2}{V_1} \right| \times 100 = \frac{2V}{19V} \times 100 = 10.5\%$$

$$D_3 = \left| \frac{V_3}{V_1} \right| \times 100 = \frac{1V}{19V} \times 100 = 5.3\%$$

$$D_4 = \left| \frac{V_4}{V_1} \right| \times 100 = \frac{0.4V}{19V} \times 100 = 2.1\%$$

Thus, the output voltage contains 10.5% second harmonic distortion, 5.3% third harmonic distortion, and 2.1% fourth harmonic distortion. Generally speaking, the second harmonic distortion is the major contributor to the total harmonic distortion.

Total Harmonic Distortion

Total harmonic distortion is defined as follows:

$$D_T = \sqrt{D_2^2 + D_3^2 + \dots + D_n^2} \quad (\text{Eq. 5-19})$$

In example 5-8, we found $D_2 = 10.5\%$, $D_3 = 5.3\%$, and $D_4 = 2.1\%$. Assuming the fifth and higher order harmonics are negligible, the total harmonic distortion in Example 5-8 is:

$$D_T = \sqrt{D_2^2 + D_3^2 + D_4^2}$$

$$D_T = \sqrt{(10.5)^2 + (5.3)^2 + (2.1)^2}$$

$$D_T = \sqrt{110.25 + 28.09 + 4.41} = \sqrt{142.75} = 11.95\%$$

As you can see, the total harmonic distortion, 11.95%, is approximately equal to the amount of second harmonic distortion, 10.5%. In practice, instruments called **distortion analyzers** are used to measure the total harmonic distortion of a signal waveform.

Three-Point Analysis

Assuming a significant amount of second harmonic distortion, the collector voltage in a large-signal amplifier typically appears as shown in Figure 5-20A. Here, note that one-half of the waveform is peaked, while the other half appears rounded.

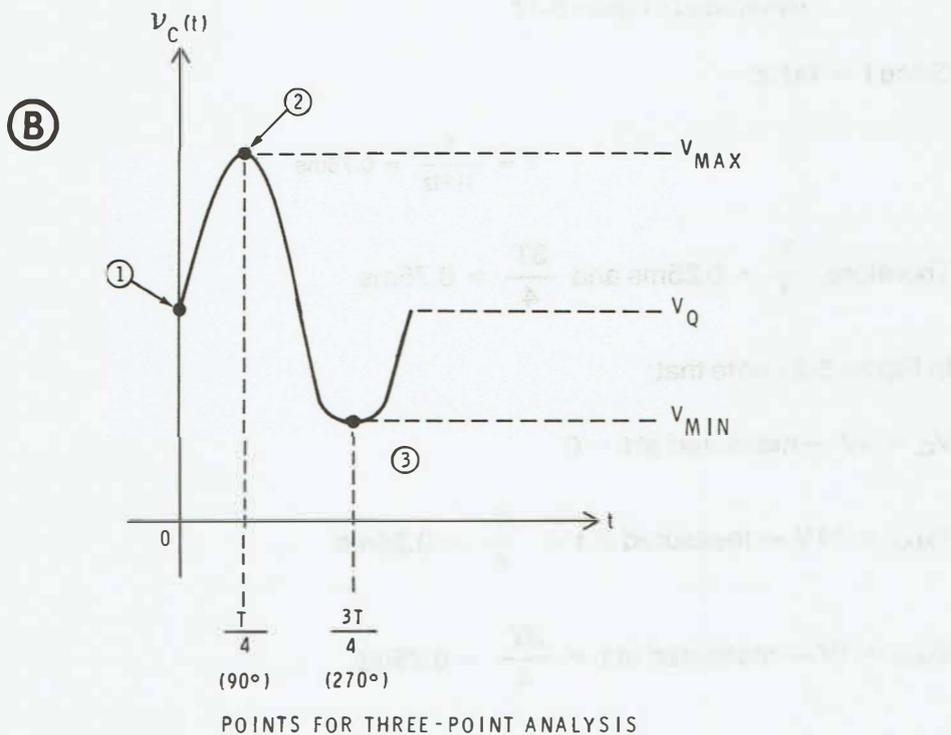
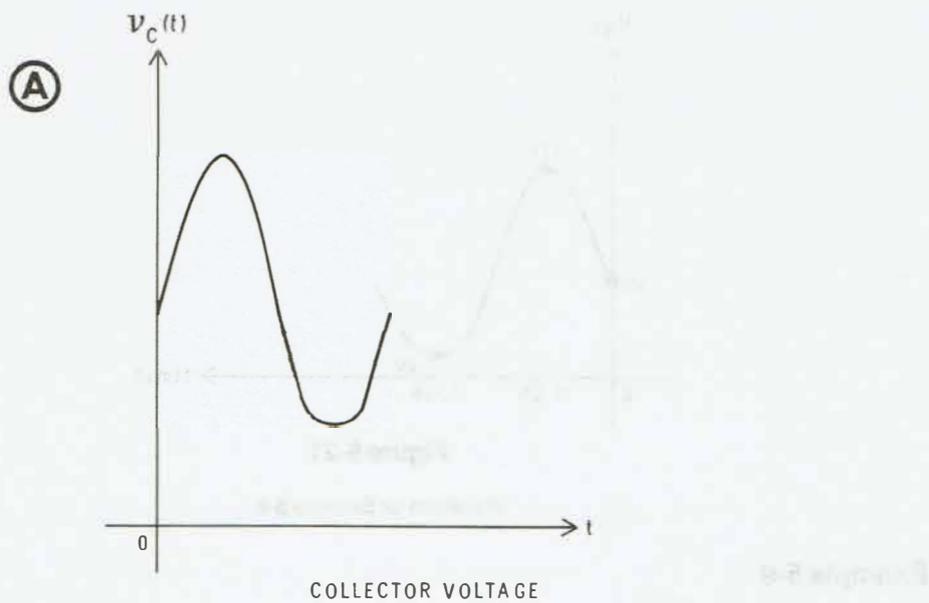
If the third and higher order harmonic components are negligible, you can estimate the degree of harmonic distortion as follows:

1. Record the values of voltage corresponding to points 1, 2, and 3 as shown in Figure 5-20B.
2. Calculate the peak value of the fundamental, V_1 , and second, V_2 , harmonic components from the following formulas.

$$V_1 = \frac{V_{\text{MAX}} - V_{\text{MIN}}}{2} \quad (\text{Eq. 5-20})$$

$$V_2 = \frac{V_{\text{MAX}} + V_{\text{MIN}} - 2V_Q}{4} \quad (\text{Eq. 5-21})$$

3. Use Equation 5-16, $D_2 = \left| \frac{V_2}{V_1} \right| \times 100$, to determine the amount of second harmonic distortion.

**Figure 5-20**

- Three-point distortion analysis.
- A. Collector voltage.
- B. Points for three-point analysis.

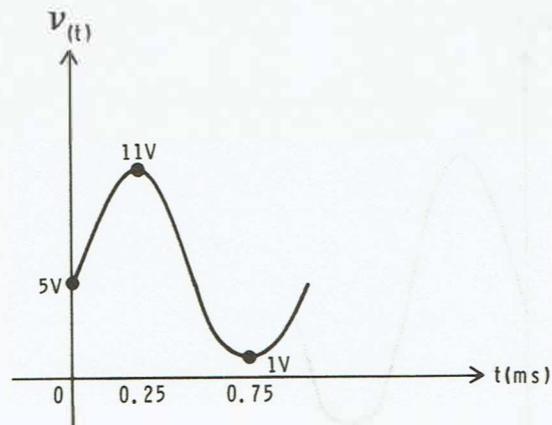


Figure 5-21

Waveform for Example 5-9.

Example 5-9

Estimate the degree of second harmonic distortion for the waveform in Figure 5-21.

Since $f = 1\text{kHz}$:

$$T = \frac{1}{1\text{kHz}} = 0.75\text{ms}$$

$$\text{Therefore, } \frac{T}{4} = 0.25\text{ms and } \frac{3T}{4} = 0.75\text{ms}$$

In Figure 5-21 note that:

$$V_Q = 5\text{V} \text{ — measured at } t = 0$$

$$V_{\text{MAX}} = 11\text{V} \text{ — measured at } t = \frac{T}{4} = 0.25\text{ms}$$

$$V_{\text{MIN}} = 1\text{V} \text{ — measured at } t = \frac{3T}{4} = 0.75\text{ms}$$

Thus:

$$V_1 = \frac{V_{\text{MAX}} - V_{\text{MIN}}}{2} = \frac{11\text{V} - 1\text{V}}{2} = 5\text{V peak}$$

$$V_2 = \frac{V_{\text{MAX}} + V_{\text{MIN}} - 2V_Q}{4} = \frac{11\text{V} + 1\text{V} - 2(5\text{V})}{4} = 0.25\text{V peak}$$

$$D_2 = \left| \frac{V_2}{V_1} \right| \times 100$$

$$D_2 = \left| \frac{0.25\text{V}}{5\text{V}} \right| \times 100 = 5\%$$

To obtain accurate values of the harmonic distortion content of a waveform, a spectrum, or distortion, analyzer is required. Since these instruments are expensive, the simple three-point method is especially useful for estimating the harmonic content of a waveform when approximate values are adequate.

The amount of harmonic distortion that is tolerable depends upon the application. In audio systems, for example, the total harmonic distortion is usually limited to from 1 to 5 percent. High-fidelity systems normally have a total harmonic distortion content that is considerably less than 1 percent.

Class B Amplifiers

The principle disadvantage of a class A amplifier is its inherent low efficiency. Recall that the quiescent power dissipated by the transistor in a class A amplifier is twice the maximum possible AC output power.

A transistor in a class B amplifier is biased at cutoff. Consequently, under ideal conditions, the quiescent power dissipated by the transistor is zero. For this reason, the conversion efficiency of a class B amplifier is considerably higher than a comparable class A amplifier. The theoretical maximum value of the conversion efficiency for a class B amplifier is 78.5%.

Remember, a single transistor biased for class B operation can only amplify one-half of the AC input voltage. In this case, the output voltage is severely distorted. Obviously, applications for a single transistor class B amplifier are quite limited.

The Push-Pull Amplifier

In order to approach the low distortion of a class A amplifier, coupled with the high efficiency of a class B amplifier, a two transistor circuit called a **push-pull amplifier** was developed.

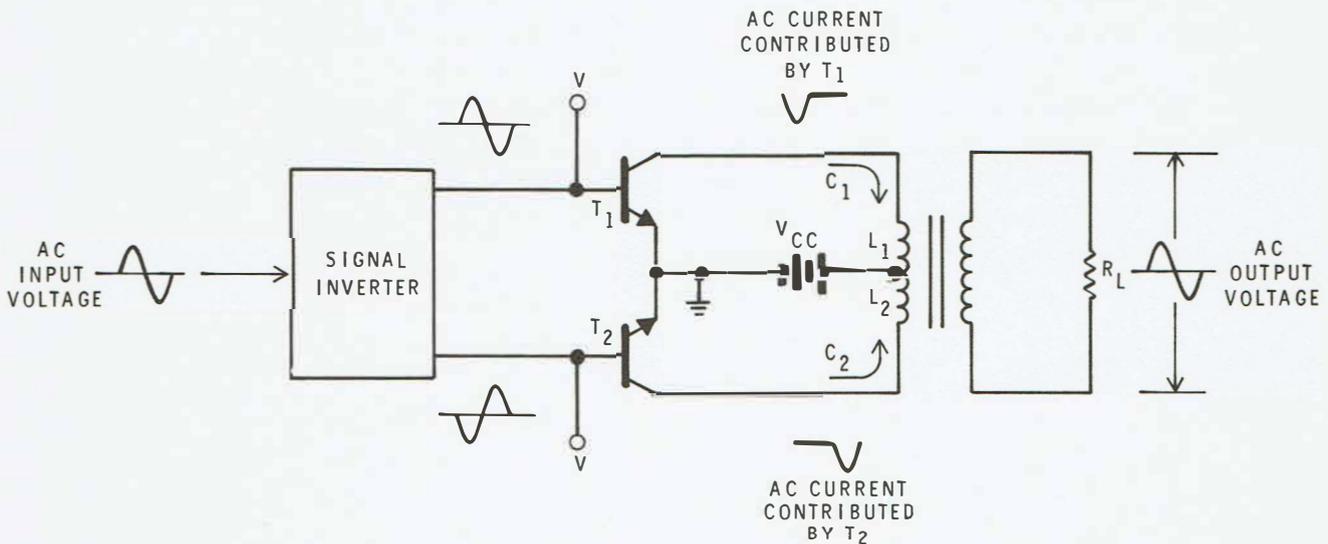


Figure 5-22

Simplified push-pull amplifier.

A simplified push-pull arrangement is illustrated in Figure 5-22. Here, note that the circuit consists of three sections — a signal inverter, followed by two transistors connected in a push-pull configuration, and a center-tapped output transformer. Briefly, the operation of the circuit in Figure 5-22 may be described as follows:

1. The AC input voltage drives the signal inverter. The function of the signal inverter is to provide two complementary output voltages. This means that each output voltage has the same amplitude and frequency, but they are 180° out of phase with respect to each other. Frequently, a center-tapped transformer is employed as the signal inverter.
2. Each output of the signal inverter is used to drive one of the two push-pull transistors. In Figure 5-22, each transistor is biased at cutoff by the DC supply voltage, V .
3. During the positive half-cycle of the AC input voltage, the signal on the base of T_1 is going positive and the signal on the base of T_2 is going negative. This causes T_1 to conduct while T_2 remains cut off. When T_1 conducts, current i_1 flows through the L_1 section of the transformer. This induces a voltage in the secondary of the transformer, which appears across R_L .
4. During the negative half-cycle of the AC input voltage, the action described in step 3 is reversed. Thus, T_2 conducts and T_1 remains cut off. In this case, current i_2 flows through the L_2 section of the transformer. As shown in Figure 5-22, the currents i_1 and i_2 flow through L_1 and L_2 respectively in **opposite directions**. For this reason, the polarity of the output voltage is positive on one half-cycle and negative on the other half-cycle. In effect, each transistor supplies one half of the AC output voltage.

A practical version of a class B push-pull amplifier is illustrated in Figure 5-23. Here, the center-tapped input transformer functions as a signal inverter. The bias voltages for the transistors are provided by the voltage divider consisting of R_1 and R_2 . For class B operation, R_2 would be small compared to R_1 .

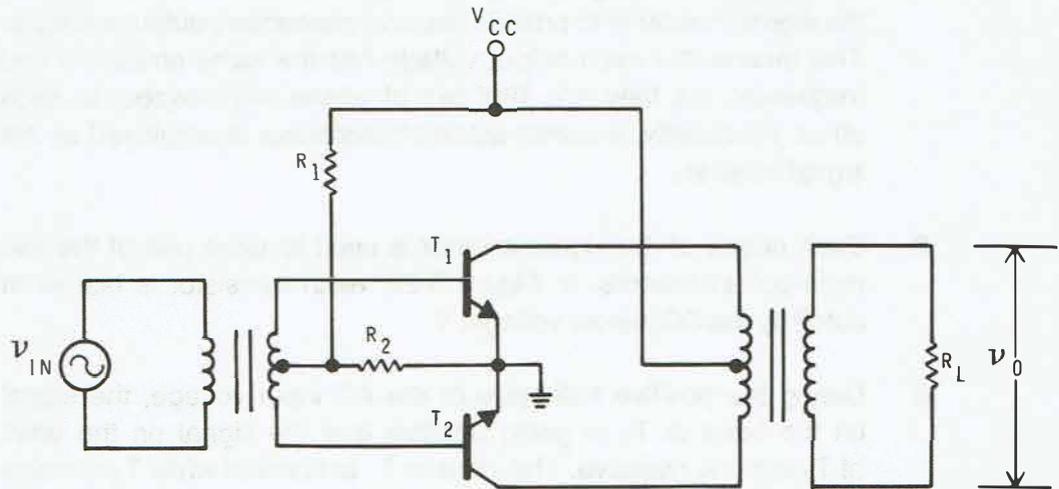


Figure 5-23

Class B push-pull power amplifier.

Harmonic Distortion In The Push-Pull Amplifier

Assuming **perfectly matched** components, a Fourier analysis of the waveforms in a class B push-pull amplifier indicates that all even harmonic components in the AC output voltage cancel. Ideally, the third-harmonic component is the principle source of nonlinear distortion in a push-pull amplifier.

In practice, components are rarely “perfectly matched”. For this reason, some second-harmonic distortion is usually present in the output of a class B push-pull amplifier.

Crossover Distortion

A significant disadvantage of class B operation in a push-pull amplifier is the resulting **crossover distortion** illustrated in Figure 5-24.

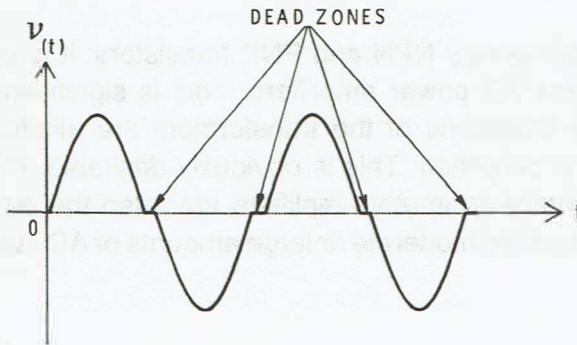


Figure 5-24

Crossover distortion.

Since the transistors in a push-pull class B amplifier are biased at cutoff, the signals driving the base of each transistor must exceed approximately 0.7V before the transistors can conduct. Consequently, when the signals driving the base of the transistors are less than 0.7V, the AC output voltage is 0V, as shown in Figure 5-24.

Since the “dead zone” regions occur between the time one transistor shuts off and the other transistor turns on, the resulting distortion is referred to as crossover distortion. To minimize crossover distortion, the transistors are biased for class AB operation rather than class B operation. In effect, each transistor is biased so that V_{BE} is approximately 0.7V. In this way, the AC output voltage changes as soon as the AC base voltage changes.

Class AB Complementary-Symmetry Amplifiers

The class B push-pull amplifier in Figure 5-23 represents the transistor counterpart of a circuit originally designed with vacuum tubes. In a general sense, vacuum tubes are analogous to NPN transistors. There is no vacuum tube counterpart of a PNP transistor.

By employing complementary NPN and PNP transistors, it is possible to design **transformerless** class AB power amplifiers. This is significant, since the cost, bulk, and frequency limitations of the transformers are eliminated! In addition, the design process is simplified. This is obviously desirable. For these reasons, class AB complementary-symmetry amplifiers are often the preferred choice for those applications requiring moderate or large amounts of AC output power.

Single Supply Circuit

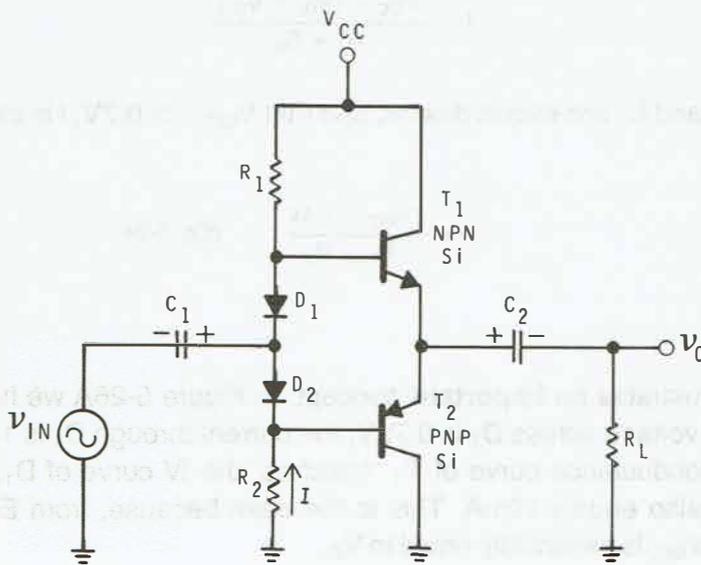


Figure 5-25

Class AB complementary-symmetry amplifier.

A very popular push-pull, class AB circuit employing complementary output transistors is illustrated in Figure 5-25. Note that:

$$V_{BE_1} = V_{D_1} + V_{D_2} - V_{BE_2}$$

Since $V_{D_2} \approx V_{BE_2}$, we have:

$$V_{BE_1} \approx V_{D_1} \quad (\text{Eq. 5-22})$$

Similarly:

$$V_{BE_2} = -V_{D_2} - V_{D_1} + V_{BE_1}$$

Since $V_{D_1} \approx V_{BE_1}$:

$$V_{BE_2} \approx -V_{D_2} \quad (\text{Eq. 5-23})$$

Equation 5-22 and Equation 5-23 indicate that the bias voltages for the transistors are provided by the two forward-biased diodes.

Neglecting the relatively small base currents, it is apparent that the current, I , flowing through R_1 , R_2 , D_1 , and D_2 is the same current. Specifically:

$$I = \frac{V_{CC} - (V_{D_1} + V_{D_2})}{R_1 + R_2}$$

Assuming D_1 and D_2 are silicon diodes, and that $V_{CC} \gg 0.7V$, I is closely approximated by:

$$I = \frac{V_{CC} - 1.4V}{R_1 + R_2} \quad (\text{Eq. 5-24})$$

Figure 5-26 illustrates an **important** concept. In Figure 5-26A we have assumed that when the voltage across D_1 is $0.72V$, the current through D_1 is $10mA$. Assuming the transconductance curve of T_1 "matches" the IV curve of D_1 , the collector current in T_1 also equals $10mA$. This is the case because, from Equation 5-22, we know that V_{BE_1} is essentially equal to V_{D_1} .

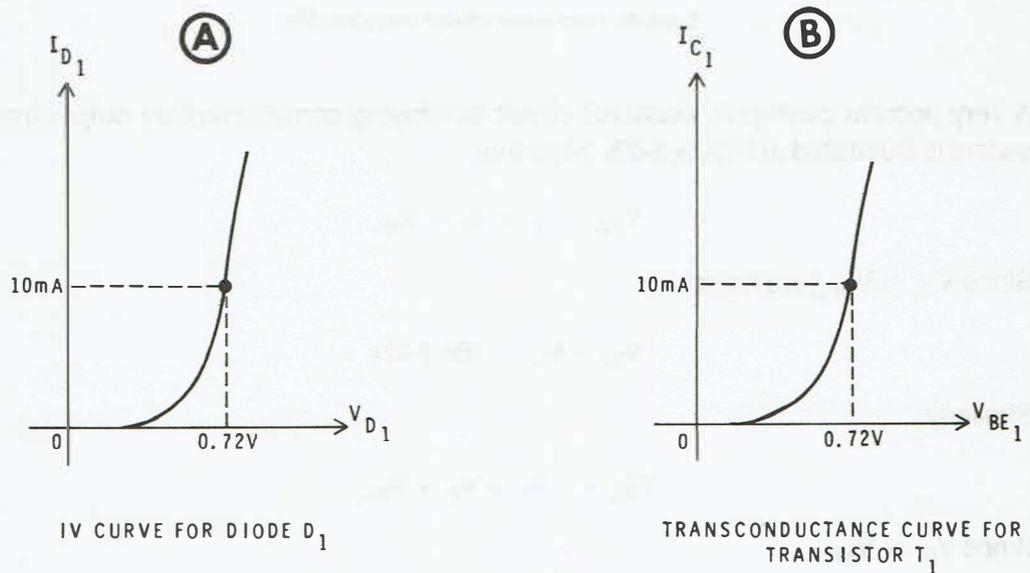


Figure 5-26

An example of a matched diode IV curve and BJT transconductance curve.

- A. IV curve for diode D_1 .
- B. Transconductance curve for transistor T_1 .

By a similar argument, I_{C_2} must equal I_{D_2} if the IV curve for D_2 is a close match to the transconductance curve of T_2 .

For these reasons, assuming the diodes and transistors in Figure 5-25 are closely matched, it is apparent that:

$$I_{C_1} \approx I_{C_2} \approx I \quad (\text{Eq. 5-25})$$

In a class AB amplifier, the value of I is **small** compared to the maximum possible peak collector current. The purpose of I is to provide a slight forward bias, through D_1 and D_2 , for T_1 and T_2 . In this way, crossover distortion is minimized.

Since T_1 and T_2 are effectively connected in series, and have similar characteristics, the DC collector-to-emitter voltages essentially equal one-half the supply voltage. Thus:

$$|V_{CE_1}| \approx |V_{CE_2}| = \frac{V_{CC}}{2} \quad (\text{Eq. 5-26})$$

By a combination of inspection, looking, and appropriate loop equations, the following DC formulas may be obtained.

$$V_{B_1} = V_{CC} - IR_1 = \frac{V_{CC}}{2} - 0.7V \quad (\text{Eq. 5-27})$$

$$V_{E_1} = V_{E_2} = \frac{V_{CC}}{2} \quad (\text{Eq. 5-28})$$

$$V_{C_1} = V_{CC} \quad (\text{Eq. 5-29})$$

$$V_{B_2} = IR_2 \quad (\text{Eq. 5-30})$$

$$V_{C_2} = 0 \quad (\text{Eq. 5-31})$$

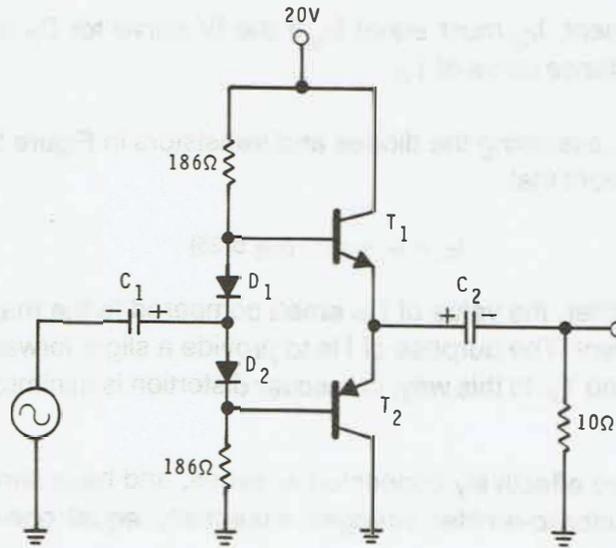


Figure 5-27

Circuit for Example 5-10.

Example 5-10

Estimate the collector currents and collector-to-emitter voltages for the transistors in Figure 5-27. Also calculate the quiescent power dissipated by each transistor.

$$I = \frac{V_{CC} - 1.4V}{R_1 + R_2} = \frac{20V - 1.4V}{186\Omega + 186\Omega} = \frac{18.6V}{372\Omega} = 50mA$$

Thus:

$$I_{C1} \approx I_{C2} \approx 50mA$$

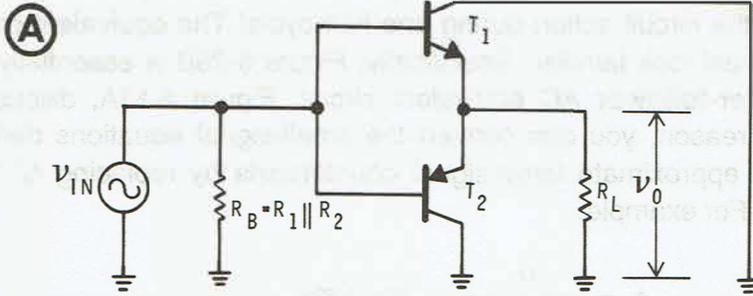
Similarly:

$$|V_{CE1}| = |V_{CE2}| = \frac{V_{CC}}{2} = \frac{20V}{2} = 10V$$

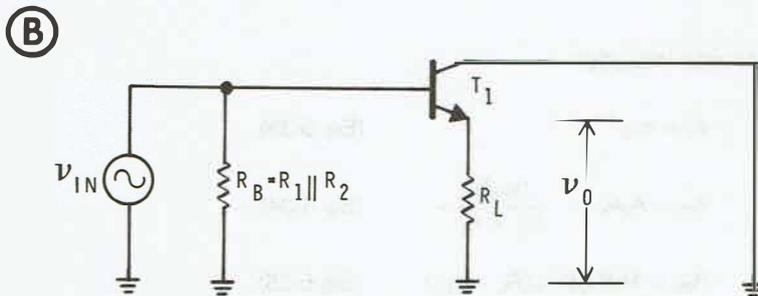
Therefore, the quiescent power dissipated by each transistor is:

$$P_{DQ} = V_{CEQ} I_{CQ}$$

$$P_{DQ} = 10V(50mA) = 0.5W$$



AC EQUIVALENT CIRCUIT



EQUIVALENT CIRCUIT DURING THE POSITIVE HALF-CYCLE OF THE AC INPUT VOLTAGE.

Figure 5-28

Equivalent circuits for the complementary-symmetry amplifier in Figure 5-25.

- A. AC equivalent circuit.
- B. Equivalent circuit during the positive half-cycle of the AC input voltage.

AC Analysis

By reducing the DC source to zero and replacing the coupling capacitors with short circuits, in Figure 5-25, you obtain the AC equivalent circuit in Figure 5-28.

Remember, on the positive half-cycle of the AC input voltage, that T_1 conducts and T_2 is cut off. Therefore, T_2 can be removed from the circuit as shown in Figure 5-28B. Since T_1 is an NPN transistor and T_2 is a PNP transistor, the circuit action is “complementary” during the negative half-cycle of the AC input voltage. Thus, the equivalent circuit during the negative half-cycle appears as shown in Figure 5-28B, with T_1 being replaced by T_2 .

The complementary nature of the circuit simplifies the AC analysis, since you need only analyze the circuit action during one half-cycle! The equivalent circuit in Figure 5-28B should look familiar. Specifically, Figure 5-28B is essentially the same as the **emitter-follower** AC equivalent circuit, Figure 4-15A, discussed in Unit 4! For this reason, you can convert the small-signal equations derived in Unit 4 into their approximate large-signal counterparts by replacing r_e' with $r_{E'}$ and h_{fe} with h_{FE} . For example:

$$A_V = \frac{R_L}{R_L + r_{E'}} \quad (\text{Eq. 5-32})$$

In Figure 5-28, note that the AC load resistance is R_L . This is why we used R_L rather than r_L in Equation 5-32. Also since R_L , typically, is large compared to $r_{E'}$, $A_V \approx 1$.

Additional useful formulas include:

$$A_i = h_{FE} \quad (\text{Eq. 5-33})$$

$$A_P = A_i A_V = \frac{h_{FE} R_L}{R_L + r_{E'}} \quad (\text{Eq. 5-34})$$

$$R_{IN} = R_1 \parallel R_2 \parallel h_{FE}(R_L + r_{E'}) \quad (\text{Eq. 5-35})$$

Class B and Class AB Power Formulas

When we discussed the AC load line of an emitter-follower in Unit 4 we found:

$$i_{C(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{r_L}$$

$$v_{CE(\text{cut})} = V_{CEQ} + I_{CQ}r_L$$

For class B operation, I_{CQ} equals zero. Similarly, for class AB operation, I_{CQ} is small compared to the value of $i_{C(\text{sat})}$. Also recall that each complementary emitter-follower in Figure 5-25 has $V_{CEQ} = \frac{V_{CC}}{2}$ and $r_L = R_L$. For these reasons, the values of $i_{C(\text{sat})}$ and $v_{CE(\text{cut})}$ are:

$$i_{C(\text{sat})} = \frac{V_{CEQ}}{r_L} = \frac{V_{CC}}{2R_L} \quad (\text{Eq. 5-36})$$

$$v_{CE(\text{cut})} = V_{CEQ} = \frac{V_{CC}}{2} \quad (\text{Eq. 5-37})$$

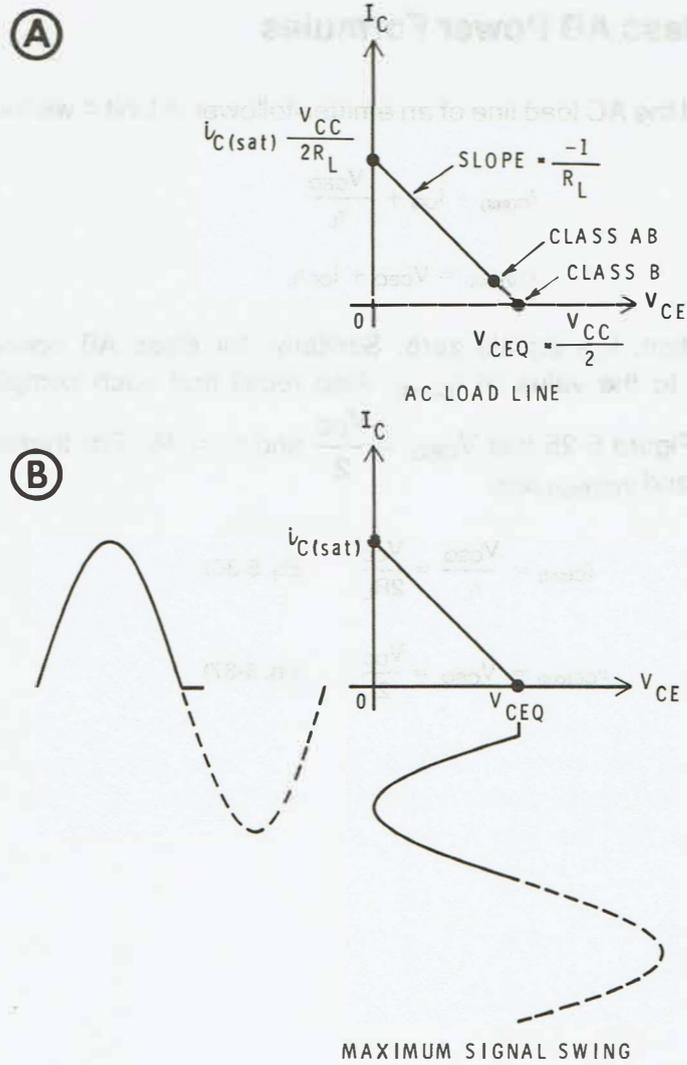


Figure 5-29

AC load lines for a class B and class AB push-pull complementary symmetry amplifier.

- A. AC load line.
- B. Maximum signal swing.

Figure 5-29A illustrates the resulting AC load line. Here, the Q point for class AB operation is very close to the Q point for class B operation. For this reason, the equations that apply to class B operation are reasonable approximations for class AB operation.

Figure 5-29B illustrates the maximum possible signal swings for each transistor in the class B push-pull amplifier. The maximum possible AC output power is:

$$P_{AC} = P_{R_L} = (0.707V_{CEQ})(0.707 \frac{V_{CEQ}}{R_L})$$

$$P_{AC} = \frac{(V_{CEQ})^2}{2R_L} \quad (\text{Eq. 5-38})$$

Substituting $V_{CEQ} = \frac{V_{CC}}{2}$ into Equation 5-38 yields:

$$P_{AC} = \frac{(V_{CC})^2}{8R_L} \quad (\text{Eq. 5-39})$$

In a class B amplifier, the power dissipated by each transistor increases when an AC signal is applied to the input terminals of the amplifier. With calculus, it is possible to prove that the worst case power dissipated by **each** transistor is:

$$P_{D(\text{MAX})} = \frac{(V_{CEQ})^2}{10R_L} = \frac{(V_{CC})^2}{40R_L} \quad (\text{Eq. 5-40})$$

The ratio of the maximum power dissipated by each transistor to the maximum possible AC load power is obtained by dividing Equation 5-40 by Equation 5-39. Thus:

$$\frac{P_{D(\text{MAX})}}{P_{AC}} = \frac{\frac{(V_{CC})^2}{40R_L}}{\frac{(V_{CC})^2}{8R_L}} = \frac{1}{5}$$

Therefore:

$$P_{D(\text{MAX})} = \frac{P_{AC}}{5} \quad (\text{Eq. 5-41})$$

The significance of Equation 5-41 is best illustrated by an example.

Example 5-11

What power ratings are required for the transistor in a push-pull class B amplifier in order to supply 10W of AC output power? What power rating would be required for a comparable class A amplifier?

For the class B push-pull amplifier, **each** transistor must be able to dissipate one fifth of the AC output power. Thus:

$$P_{D(\text{MAX})} \geq \frac{P_{\text{AC}}}{5} \geq \frac{10\text{W}}{5} \geq 2\text{W}$$

Recall that in a class A amplifier the worst case power dissipation occurs under quiescent conditions. In addition, P_{DQ} is double the maximum possible AC output power. Thus:

$$P_{D(\text{MAX})} \geq 2P_{\text{AC}} \geq 2(10\text{W}) \geq 20\text{W}$$

Obviously, lower power transistors can be employed in the class B design as opposed to the class A design!

Example 5-12

The circuit in Figure 5-27 was partially analyzed in Example 5-10. Work out values for:

- A. $i_{C(sat)}$
- B. The maximum possible AC output power.
- C. The required power ratings for T_1 and T_2 .
- D. The voltage gain.
- E. The input resistance as seen by the signal source.

Assume $h_{FE} = 20$ and $r_{E'} = 0.4\Omega$.

$$A. \quad i_{C(sat)} = \frac{V_{CC}}{2R_L} = \frac{20V}{2(10\Omega)} = 1A$$

$$B. \quad P_{AC} = \frac{(V_{CC})^2}{8R_L} = \frac{(20V)^2}{8(10\Omega)} = 5W$$

$$C. \quad P_{D(MAX)} = \frac{(V_{CC})^2}{40R_L} = \frac{(20V)^2}{40(10\Omega)} = 1W$$

Note that $P_{D(MAX)}$ equals one-fifth the maximum possible AC output power. Each transistor should have a $P_{D(MAX)}$ rating of at least 1W.

$$D. \quad A_V = \frac{R_L}{R_L + r_{E'}} = \frac{10\Omega}{10\Omega + 0.4\Omega} = 0.961$$

$$E. \quad R_{IN} = R_1 \parallel R_2 \parallel h_{FE}(R_L + r_{E'})$$

$$R_{IN} = 186\Omega \parallel 186\Omega \parallel 20(10\Omega + 0.4\Omega)$$

$$R_{IN} = 93\Omega \parallel 208\Omega = 64.3\Omega$$

Dual Supply Circuit

In those systems where both positive and negative supply voltages are employed, the circuit shown in Figure 5-30A is commonly used. Notice that the circuit **does not** require an output coupling capacitor. This is because the DC emitter-to-ground voltages in Figure 5-30A, ideally, equal zero.

The AC load line for the dual supply circuit is provided in Figure 5-30B. You will notice that V_{CEQ} equals V_{CC} , not $V_{CC}/2$. For this reason, you have to modify some of the equations derived for the single supply circuit in order to apply them to the dual supply circuit.

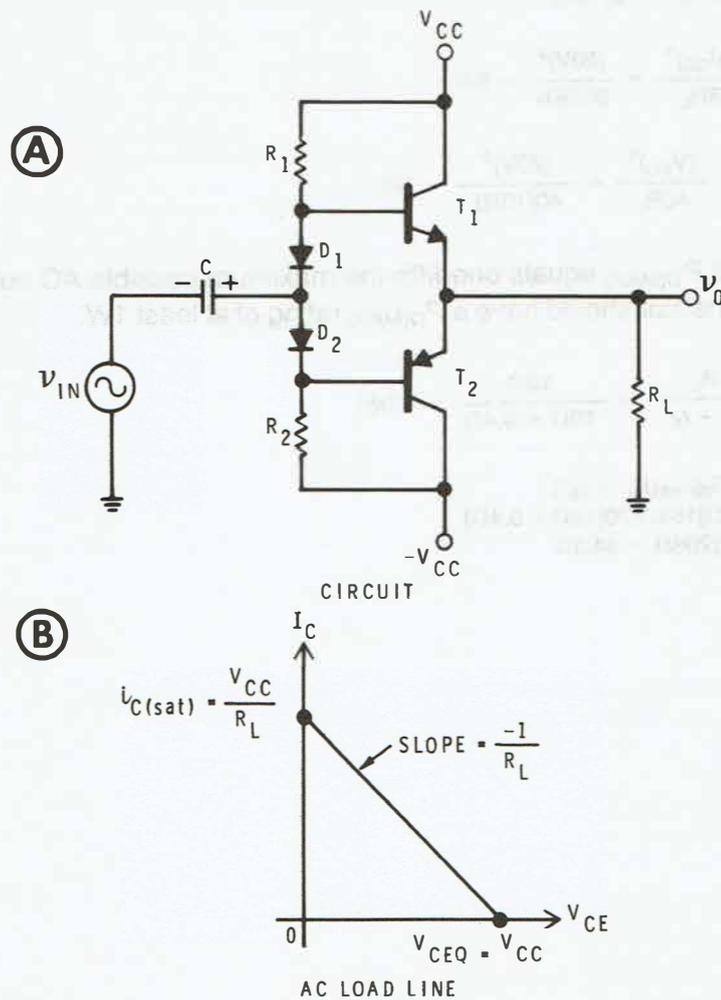


Figure 5-30

A dual-supply class AB complementary-symmetry amplifier.

- A. Circuit.
- B. AC load line.

Appropriate formulas for both the single supply and dual supply circuits are provided in Table 5-2.

Parameter	Single Supply	Dual Supply
I	$\frac{V_{CC} - 1.4V}{R_1 + R_2}$	$\frac{2V_{CC} - 1.4V}{R_1 + R_2}$
V_{CE}	$V_{CE_1} = \frac{V_{CC}}{2}, V_{CE_2} = -\frac{V_{CC}}{2}$	$V_{CE_1} = V_{CC}, V_{CE_2} = -V_{CC}$
V_B	$V_{B_1} = V_{CC} - IR_1$ $V_{B_1} = V_{CC} - 0.7V$ $V_{B_2} = IR_2$	$V_{B_1} = V_{CC} - IR_1$ $V_{B_1} = V_{CC} - 0.7V$ $V_{B_2} = IR_2 - V_{CC}$
V_E	$V_{E_1} = V_{E_2} = \frac{V_{CC}}{2}$	$V_{E_1} = V_{E_2} = 0V$
V_C	$V_{C_1} = V_{CC}, V_{C_2} = 0V$	$V_{C_1} = V_{CC}, V_{C_2} = -V_{CC}$
A_V	$A_V = \frac{R_L}{R_L + r_{e'}} \approx 1$	$A_V = \frac{R_L}{R_L + r_{e'}} \approx 1$
A_i, A_p	$A_i = h_{FE}, A_p = A_i A_V$	$A_i = h_{FE}, A_p = A_i A_V$
R_{IN}	$R_{IN} = R_1 \parallel R_2 \parallel h_{FE}(R_L + r_{e'})$	$R_{IN} = R_1 \parallel R_2 \parallel h_{FE}(R_L + r_{e'})$
P_{AC}	$\frac{(V_{CC})^2}{8R_L}$	$\frac{(V_{CC})^2}{2R_L}$
$P_{D_{MAX}}$	$\frac{(V_{CC})^2}{40R_L} = \frac{P_{AC}}{5}$	$\frac{(V_{CC})^2}{10R_L} = \frac{P_{AC}}{5}$

TABLE 5-2

Summary of approximate formulas for the single and dual supply, complementary-symmetry push-pull class AB amplifiers.

Darlington Pairs

The class AB amplifiers discussed previously consisted of two complementary emitter-followers. In order to increase the amplifier's input resistance and decrease the amplifier's output resistance, Darlington pair packages can be employed as shown in Figure 5-31.

Counting the base-emitter junctions in Figure 5-31 between point 1 and point 2, you find there are four; the junctions in T_1 , T_2 , T_3 , and T_4 . For this reason, four diodes must be connected between points 1 and 2 in order to properly bias the transistors.

The $P_{D(MAX)}$ ratings of T_2 and T_3 should at least equal one-fifth the maximum possible AC output power. Since T_1 and T_4 provide the input signals for T_2 and T_3 , the power ratings required for T_1 and T_4 are considerably lower than those required for T_2 and T_3 . As a guide, T_1 and T_4 should have a $P_{D(MAX)}$ rating at least equal to:

$$P_{D(MAX)} = \frac{P_{AC}}{5h_{FE}} \quad (\text{Eq. 5-42})$$

Where h_{FE} is the large-signal current gain of T_2 and T_3 .

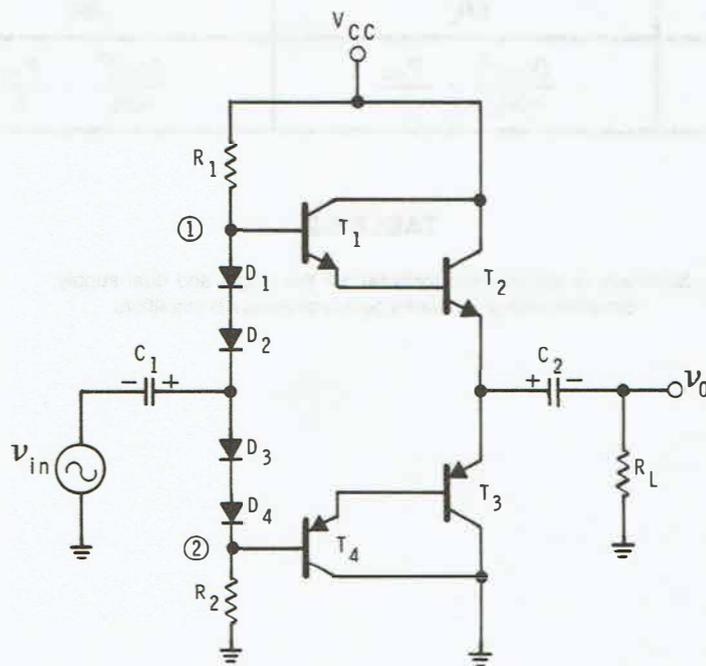


Figure 5-31

Complementary-symmetry amplifier with Darlington-pair packages T_1 , T_2 and T_3 , T_4 .

Quasi-Complementary Amplifiers

For power dissipations greater than approximately 10W, the availability of suitable complementary transistors is quite limited. Moreover, high power PNP transistors generally cost more than their NPN counterparts.

In an attempt to manufacture inexpensive high power PNP transistors, the compound configuration illustrated in Figure 5-32A was developed. Here, a negative-going signal on the base of T_1 produces a positive going signal at the collector of T_1 . Since the collector of T_1 is connected to the base of T_2 , the signal at the collector of T_2 swings negative. The action just described indicates that the compound configuration in Figure 5-32A acts like a single PNP transistor. As was the case with the Darlington packages discussed earlier, the effective h_{FE} of the compound package approximately equals $h_{FE_1}h_{FE_2}$.

Figure 5-32B illustrates how an equivalent NPN transistor can be obtained with a suitable compound package. In practice, this configuration is rarely used due to the fact that a high power PNP transistor, T_4 , is required in the output stage.

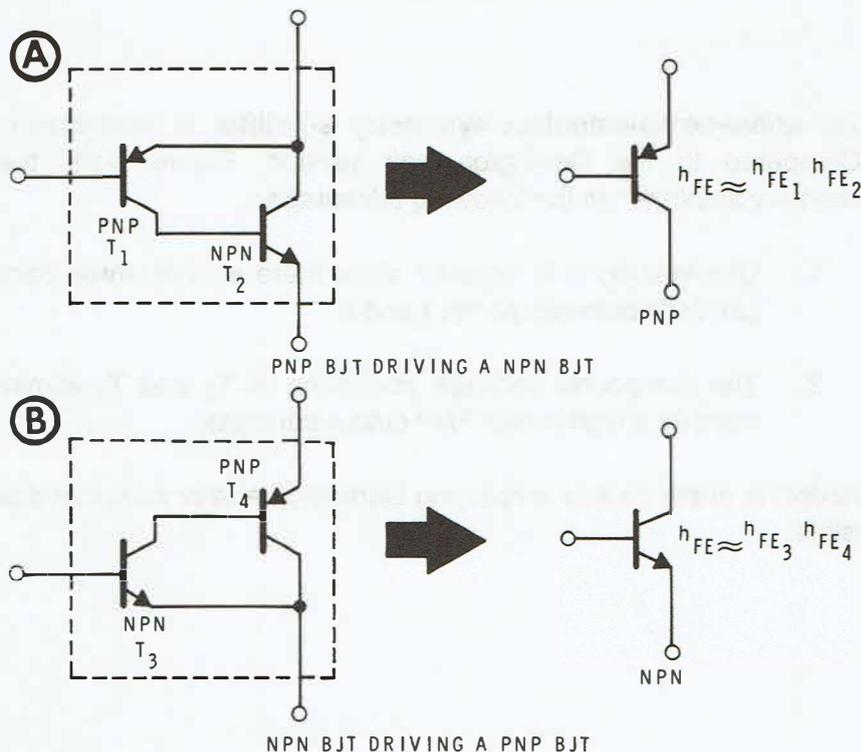


Figure 5-32

- Compound BJT configurations.
- PNP BJT driving an NPN BJT.
 - NPN BJT driving a PNP BJT.

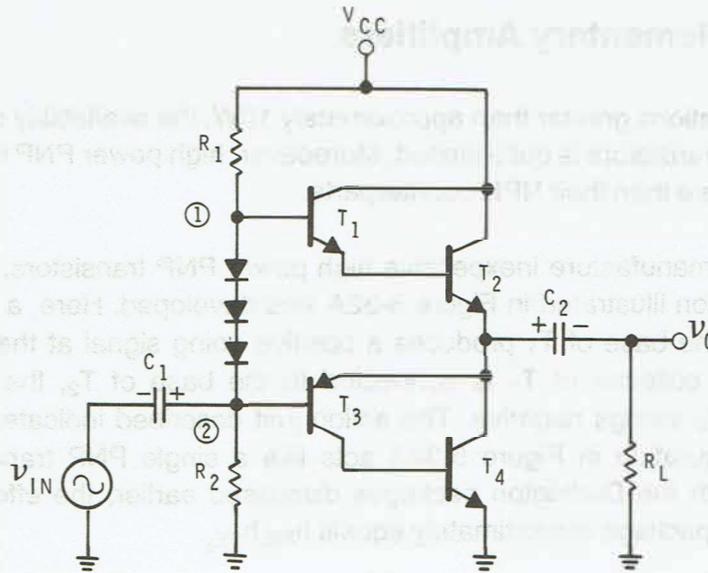


Figure 5-33

An example of a quasi-complementary-symmetry amplifier. Here, T_1, T_2 form an NPN Darlington package while T_3, T_4 constitute a PNP compound package.

A popular **quasi-complementary-symmetry amplifier** is illustrated in Figure 5-33. Compared to the Darlington pair version, Figure 5-31, the quasi-complementary amplifier has the following advantages:

1. One less diode is required, since there are only three base-emitter junctions between points 1 and 2.
2. The compound package consisting of T_3 and T_4 eliminates the need for a high power PNP output transistor.

Many variations of the circuits employing Darlington and/or compound packages are possible.

Designing Class AB Power Amplifiers

Due to nonideal component characteristics, the actual clipping levels in class AB amplifiers that utilize a **single input coupling capacitor** can be significantly less than $\pm V_{CEQ}$.

A simple solution to this potential problem is illustrated in Figure 5-34. The input AC waveform is coupled to the bases of T_1 and T_2 simultaneously. The positive peak forward biases the p-type base of T_1 , causing current to flow through T_1 . At the same time, the positive peak applied to the base of T_2 is reverse bias and ensures that T_2 does NOT conduct. On the negative half cycle, the transistor's status is reversed, with T_2 forward biased and conducting, and T_1 cut off. Depending upon the nature of the signal source and the actual component characteristics, either one or two input coupling capacitors may be required for satisfactory circuit operation.

The following design guides for both single and dual supply circuits should help you design basic class AB power amplifiers.

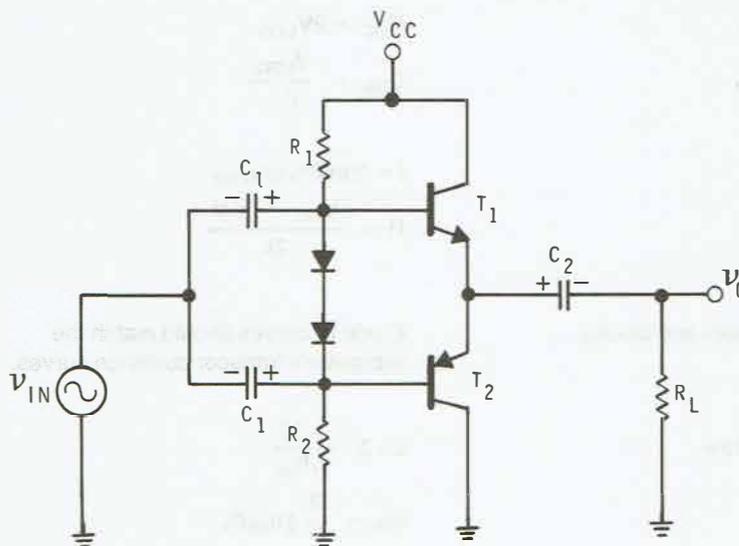
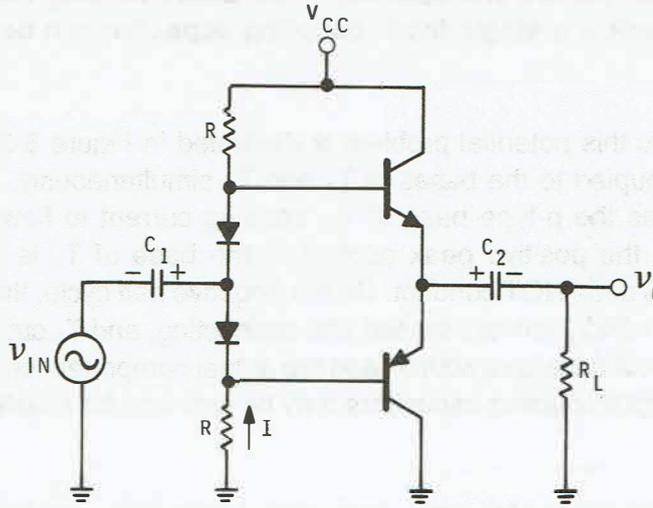


Figure 5-34

A coupling arrangement that employs two input capacitors.

SINGLE SUPPLY CLASS AB PUSH-PULL POWER AMPLIFIER



1. Calculate V_{CEQ}

$$V_{CEQ} = \sqrt{2P_{AC}R_L}$$

2. Calculate V_{CC}

$$V_{CC} = 2V_{CEQ}$$

3. Calculate i_{Csat}

$$i_{Csat} = \frac{V_{CEQ}}{R_L}$$

4. Select I

$$I \approx 2 \text{ to } 6\% \text{ of } i_{Csat}$$

5. Calculate R

$$R = \frac{V_{CC} - 1.4V}{2I}$$

6. Select transistors and diodes.

Diode IV curves should match the transistor's transconductance curves.

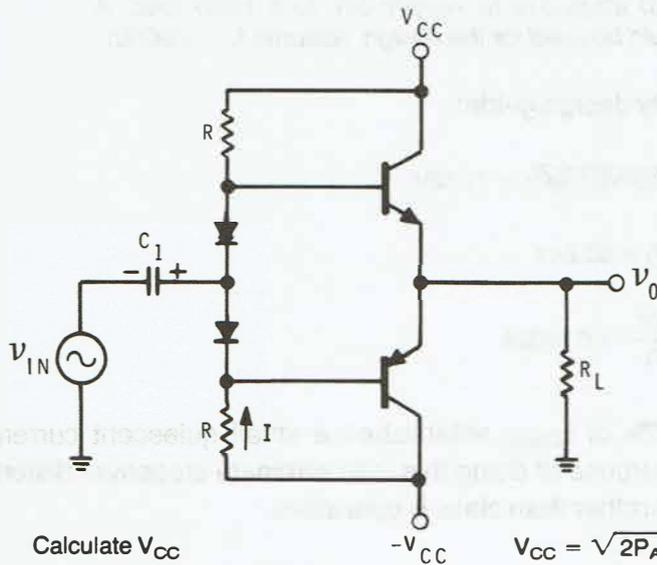
7. Select capacitors

$$C_1 \geq \frac{3.18}{f_1 R_{IN}}$$

$$R_{IN} \approx \frac{R}{2} \parallel h_{FE} R_L$$

$$C_2 \geq \frac{3.18}{f_1 R_L}$$

DUAL SUPPLY CLASS AB PUSH-PULL POWER AMPLIFIER



1. Calculate V_{CC}

$$V_{CC} = \sqrt{2P_{AC}R_L}$$

2. Calculate i_{Csat}

$$i_{Csat} = \frac{V_{CC}}{R_L}$$

3. Select I

$$I \approx 2 \text{ to } 6\% \text{ of } i_{Csat}$$

4. Calculate R

$$R = \frac{2V_{CC} - 1.4V}{2I}$$

5. Select transistors and diodes.

Diode IV curves should match the transistor's transconductance curves.

6. Select C

$$C_1 \geq \frac{3.18}{f_1 R_{IN}}$$

$$R_{IN} \approx \frac{R}{2} \parallel h_{FE} R_L$$

Example 5-13

Design a class AB amplifier to supply 5W to a 100Ω load. A single supply should be used for the design. Assume $f_1 = 500\text{Hz}$.

Referring to the single supply design guide:

1. $V_{CEQ} = \sqrt{2P_{AC}R_L} = \sqrt{2(5W)(100\Omega)} = 31.62V$
2. $V_{CC} = 2V_{CEQ} = 2(31.62V) = 63.24V$
3. $i_{C(sat)} = \frac{V_{CEQ}}{R_L} = \frac{31.62V}{100\Omega} = 0.3162A$
4. Selecting $I = 2$ to 6% of $i_{C(sat)}$ establishes a small quiescent current in the transistors. The purpose of doing this is to eliminate crossover distortion by providing class AB rather than class B operation.

Ideally, $I_{CQ} = I$. In practice however, I_{CQ} is usually different from the value of I , since the diode IV curves and transistor transconductance curves rarely match exactly. The exact value of I_{CQ} is not important as long as it is sufficient to provide class AB operation. Thus, selecting I equal to 5% of $i_{C(sat)}$ we have:

$$I = 5\%(0.3162A) = 15.81\text{mA}$$

5. You can simplify the design process by choosing $R_1 = R_2 = R$. Thus:

$$R = \frac{V_{CC} - 1.4V}{2I} = \frac{63.24V - 1.4V}{2(15.81\text{mA})} = 1.95\text{k}\Omega$$

6. The required transistor ratings are:

$$P_{D(\text{MAX})} \geq \frac{P_{\text{AC}}}{5} \geq \frac{5\text{W}}{5} \geq 1\text{W}$$

$$V_{\text{CE}(\text{MAX})} \geq V_{\text{CEQ}} \geq 31.62\text{V}$$

$$I_{\text{C}(\text{MAX})} \geq i_{\text{C}(\text{sat})} \geq 0.3162\text{A}$$

Naturally, the transistors selected from the design should have maximum ratings somewhat larger than the values just calculated.

In addition, it is desirable to select transistors whose h_{FE} values, at $1.8I_{\text{CQ}}$, are such that:

$$h_{\text{FE}}R_{\text{L}} \geq 5R$$

Such a choice helps to ensure adequate base drive on the maximum peaks of the AC input signal.

Ideally, the diode IV curves should match the transistor transconductance curves. If suitable diodes are not found, you can use transistors connected to act like diodes, as shown in Figure 5-35.

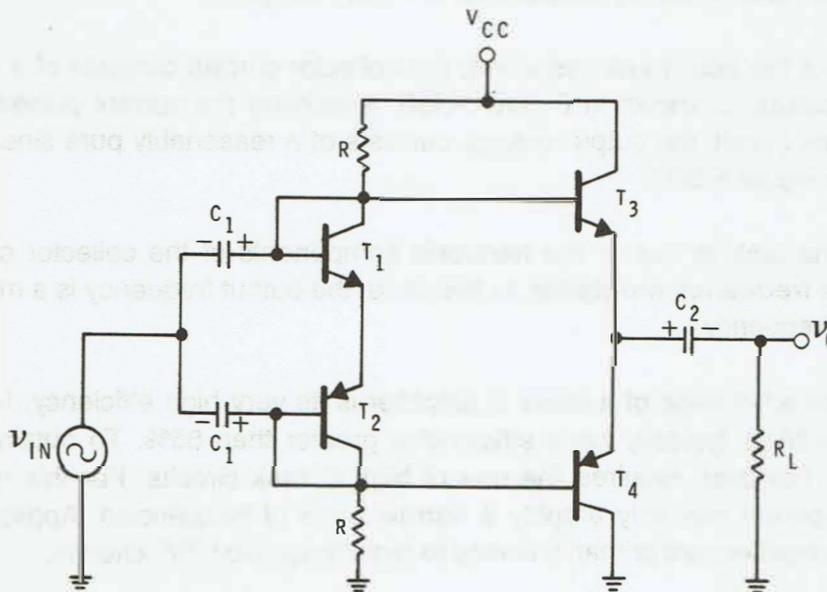


Figure 5-35

T_1 , T_3 and T_2 , T_4 are the same type transistors. By shorting the base-collector terminals of T_1 and T_2 the input transistors act like diodes. In this way, a "reasonable match" between the diode, T_1 , T_2 IV curves and transistor, T_3 , T_4 transconductance curves is obtained.

7. Assuming $h_{FE} = 100$:

$$R_{IN} = \frac{R}{2} \parallel h_{FE} R_L$$

$$R_{IN} = \frac{1.95\text{k}\Omega}{2} \parallel 100(100\Omega)$$

$$R_{IN} = 0.975\text{k}\Omega \parallel 10\text{k}\Omega = 888.4\Omega$$

$$C_1 = \frac{3.18}{f_1 R_{IN}} = \frac{3.18}{500\text{Hz}(888.4\Omega)} = 7.2\mu\text{F}$$

$$C_2 = \frac{3.18}{f_1 R_L} = \frac{3.18}{500\text{Hz}(100\Omega)} = 63.6\mu\text{F}$$

Class C Amplifiers

A class C amplifier is illustrated by the circuit in Figure 5-36A. Here, the $R_B C_1$ time constant is made large compared to the period of the AC input signal. The combination of C_1 and the base-emitter diode of the transistor results in a negative clamping action at the base of the transistor. For this reason, conduction only occurs on the most positive peaks of the AC input voltage.

As a result of the action just described, the collector current consists of a series of current pulses as shown in Figure 5-36B. Assuming the current pulses drive a high Q tank circuit, the output voltage consists of a reasonably pure sine wave as shown in Figure 5-30C.

By tuning the tank to one of the harmonic components of the collector current you obtain a **frequency multiplier**. In this case, the output frequency is a multiple of the input frequency.

The principle advantage of a class C amplifier is its very high efficiency. In fact, class C amplifiers typically have efficiencies greater than 85%. To obtain such efficiencies, however, requires the use of high Q tank circuits. For this reason class C amplifiers can only amplify a narrow band of frequencies. Applications for class C amplifiers are primarily limited to radio frequency, RF, circuits.

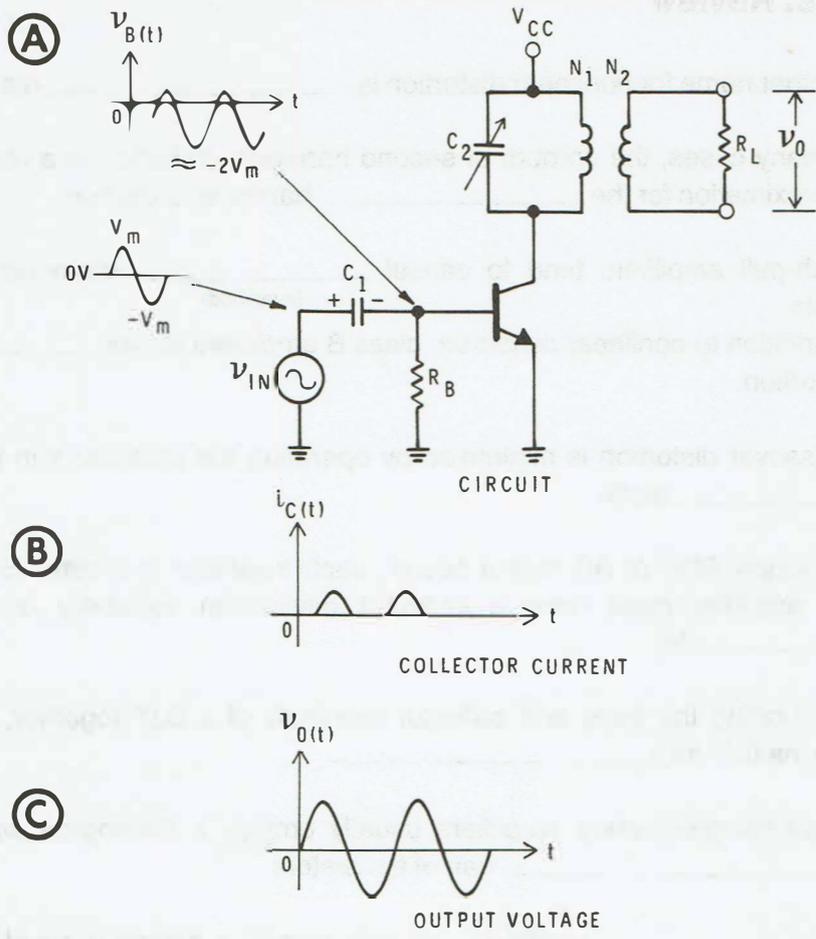


Figure 5-36

- A class C amplifier.
- A. Circuit.
- B. Collector current.
- C. Output voltage.

Self-Test Review

16. Another name for nonlinear distortion is _____ distortion.
17. In many cases, the amount of second harmonic distortion is a reasonable approximation for the _____ harmonic distortion.
18. Push-pull amplifiers tend to cancel _____ harmonic components.
(even/odd)
19. In addition to nonlinear distortion, class B amplifiers exhibit _____ distortion.
20. Crossover distortion is minimized by operating the transistors in the class _____ mode.
21. To supply 20W of AC output power, each transistor in a class B or class AB amplifier must have a collector dissipation capability of at least _____W.
22. By shorting the base and collector terminals of a BJT together, you can use the BJT as a _____.
23. Quasi-complementary amplifiers usually employ a Darlington pair and a _____ pair of transistors.
24. Class _____ amplifiers can only amplify a narrow band of frequencies.
25. Class _____ amplifiers typically have efficiencies in excess of 85 percent.

Answers

- | | |
|---------------|---|
| 16. harmonic | 21. $P_{D(MAX)} = \frac{P_{AC}}{5}$ or 4W |
| 17. total | 22. diode |
| 18. even | 23. compound |
| 19. crossover | 24. C |
| 20. AB | 25. C |

SUMMARY

Power amplifiers are classified according to their mode of operation. Descriptions of the four fundamental modes — class A, class AB, class B, and class C — serve as an introduction to this unit.

In power amplifiers, the signal swings in collector current and collector-to-emitter voltage represent the largest possible changes. Hence, several large-signal parameters were introduced so that the small-signal formulas derived in Units 3 and 4 could be converted into their approximate large-signal counterparts.

Several examples illustrating the analysis and design of class A power amplifiers were provided in the unit. Since class A amplifiers are the least efficient, they are only used for low power applications.

The nonlinear characteristics of transistors change the shape of the signal waveform. This type of distortion is called harmonic distortion. By measuring the output signal at three points, it is possible to estimate the amount of second harmonic distortion using the equations provided in this unit. Frequently, the amount of second harmonic distortion is a reasonable approximation of the total harmonic distortion.

Class B amplifiers can have conversion efficiencies as high as 78.5%. However, class B amplifiers introduce crossover distortion into the output waveform. To minimize crossover distortion the amplifier is designed to operate in the class AB mode rather than the class B mode.

The analysis and design of push-pull, complementary-symmetry amplifiers were discussed in some detail. By referring to the examples and appropriate design guides, you should be able to design useful power amplifiers. Dual supply circuits are especially useful in portable equipment, where a battery power source is used.

Although class C amplifiers have very high efficiencies, applications for these circuits are limited. This is because class C circuits require a resonant tank in the collector. Consequently, only a limited range of signal frequencies can be amplified in a class C amplifier.

UNIT EXAMINATION

The following multiple choice examination is designed to test your understanding of the material presented in this unit. Place a check beside the multiple choice answer (A, B, C, or D) that you feel is most correct. When you have completed the examination, compare your answers with the correct ones that appear after the exam.

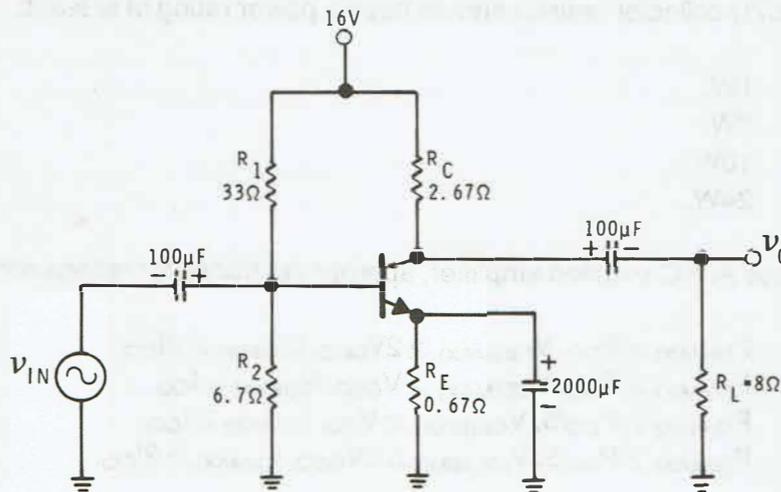


Figure 5-37

Circuit for questions 1 to 5.

Refer to Figure 5-37 for questions 1 through 5.

- The quiescent power dissipated by the transistor is:
 - 0.45W.
 - 5W.
 - 18W.
 - 11.25W.
- The maximum possible power dissipated by the 8Ω load device is:
 - 2.25W.
 - 5W.
 - 11.25W.
 - 18W.
- The total DC input power, including the power dissipated by the biasing resistors, is:
 - 18W.
 - 24.03W.
 - 54.45W.
 - 48W.

4. The conversion efficiency of the circuit is:
- A. 25%.
 - B. 16.5%.
 - C. 4.13%.
 - D. 0%.
5. The 2.67Ω collector resistor should have a power rating of at least:
- A. 1W.
 - B. 2W.
 - C. 10W.
 - D. 24W.
6. In a class A, RC-coupled amplifier, appropriate transistor ratings are:
- A. $P_{D(MAX)} \geq P_{DQ}$, $V_{CE(MAX)} \geq 2V_{CEQ}$, $I_{C(MAX)} \geq 2I_{CQ}$.
 - B. $P_{D(MAX)} \geq P_{DQ}$, $V_{CE(MAX)} \geq V_{CEQ}$, $I_{C(MAX)} \geq I_{CQ}$.
 - C. $P_{D(MAX)} \geq P_{DQ}/5$, $V_{CE(MAX)} \geq V_{CC}$, $I_{C(MAX)} \geq I_{CQ}$.
 - D. $P_{D(MAX)} \geq P_{AC}/5$, $V_{CE(MAX)} \geq 2V_{CEQ}$, $I_{C(MAX)} \geq 2I_{CQ}$.

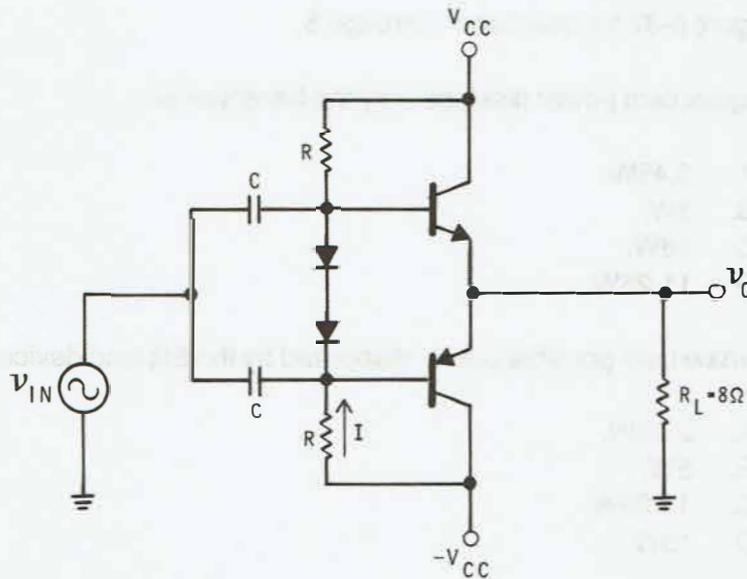


Figure 5-38

Circuit for questions 7 to 11.

Refer to Figure 5-38 for questions 7 through 11. Here, the maximum possible AC load power is assumed to be 2.25W.

7. The supply voltage should equal:
- A. $\pm 12\text{V}$.
 - B. $\pm 6\text{V}$.
 - C. $\pm 3\text{V}$.
 - D. $+6\text{V}, -3\text{V}$.
8. The transistors should have an $I_{C(\text{MAX})}$ rating at least equal to:
- A. 0.75A.
 - B. 1.5A.
 - C. I_{CQ} .
 - D. $2I_{CQ}$.
9. Assuming $I = 4\% i_{C(\text{sat})}R$ should equal, approximately:
- A. 353.34Ω .
 - B. 176.67Ω .
 - C. 88.33Ω .
 - D. 44.16Ω .
10. The transistors should have a $P_{D(\text{MAX})}$ rating at least equal to:
- A. 4.5W.
 - B. 2.25W.
 - C. 1.12W.
 - D. 0.45W.
11. Assuming $f_1 = 1\text{kHz}$, the required value for C_2 is:
- A. C_2 not required.
 - B. $397.5\mu\text{F}$.
 - C. $39.75\mu\text{F}$.
 - D. $3.975\mu\text{F}$.

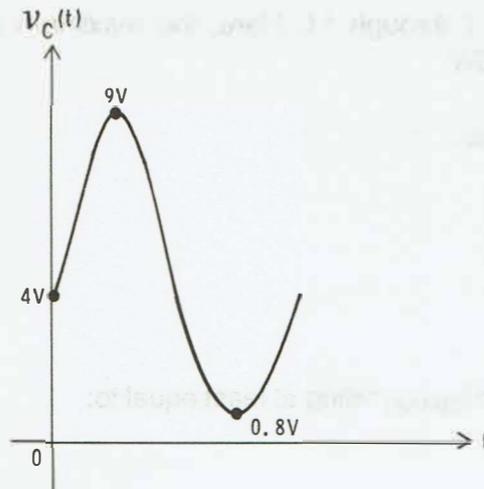


Figure 5-39

Waveform for questions 12 to 14.

Refer to Figure 5-39 for questions 12 through 14.

12. The peak value of the fundamental component of the voltage is approximately:
- 9V.
 - $9V - 0.8V$.
 - $9V - 4V$.
 - 4.1V.
13. The peak value of the second harmonic component of the voltage is approximately:
- 0.45V.
 - $9V - 0.8V/2$.
 - 0V.
 - Depends on frequency.
14. The percent second harmonic distortion approximately equals:
- 0%.
 - 10.9%.
 - 7.3%.
 - 3.70%.
15. The most efficient type of amplifier discussed in this unit is:
- Class A.
 - Class B.
 - Class AB.
 - Class C.

EXAMINATION ANSWERS

1. C — To calculate P_{DQ} you must first calculate the values of I_{CQ} and V_{CEQ} .
Thus:

$$V_B = \frac{16V(6.7\Omega)}{33\Omega + 6.7\Omega} = 2.7V$$

$$V_E = 2.7V - 0.7V = 2V$$

$$I_E = \frac{V_E}{R_E} = \frac{2V}{0.67\Omega} = 2.99A \approx 3A \approx I_{CQ}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$V_{CE} = 16V - 3A(2.67\Omega + 0.67\Omega)$$

$$V_{CE} = 16V - 10.02V \approx 6V = V_{CEQ}$$

Thus:

$$P_{DQ} = V_{CEQ}I_{CQ}$$

$$P_{DQ} = 6V(3A) = 18W$$

2. A — The maximum possible power dissipated by R_L is:

$$P_{R_L} = \frac{(V_{CEQ})^2}{2R_L} = \frac{(6V)^2}{2(8\Omega)} = 2.25W$$

3. C — The total DC input power, including the power dissipated by the biasing resistors, is calculated using Equation 5-1. Here:

$$P_{DC} = V_{CC}[I_{CQ} + I_{R_1}]$$

Since $V_B = 2.7V$ and $R_2 = 6.7\Omega$, I_{R_2} equals $2.7V/6.7\Omega$ or $0.403A$ (neglecting the small base current, $I_{R_1} = I_{R_2}$). Therefore:

$$P_{DC} = 16V[3A + 0.403A] = 54.45W$$

4. C — Conversion efficiency is a ratio of the maximum possible AC load power to the DC input power. Thus:

$$\eta' = \frac{P_{AC}}{P_{DC}} \times 100$$

$$\eta' = \frac{2.25W}{54.45W} \times 100 = 4.13\%$$

5. D — Since $I_{CQ} = 3A$:

$$P_{R_C} = (I_{CQ})^2 R_C$$

$$P_{R_C} = (3A)^2 (2.67\Omega) = 24W$$

6. A — In a class A, RC coupled amplifier, the approximate transistor ratings are:

$$P_{D(MAX)} \geq P_{DQ}, V_{CE(MAX)} \geq 2V_{CEQ}, I_{C(MAX)} \geq 2I_{CQ}$$

7. B — Referring to the dual supply design guide:

$$V_{CC} = \sqrt{2P_{AC}R_L} = \sqrt{2(2.25W)(8\Omega)} = 6V$$

8. A — $I_{C(MAX)} \geq i_{C(sat)}$. For the dual supply circuit:

$$i_{C(sat)} = \frac{V_{CC}}{R_L} = \frac{6V}{8\Omega} = 0.75A$$

9. B — $4\% i_{C(sat)} = 4\% (0.75A) = 30mA$.

$$R = \frac{2V_{CC} - 1.4V}{2I} = \frac{2(6V) - 1.4V}{2(30mA)} = 176.67\Omega$$

10. D — In the push-pull amplifier, $P_{D(MAX)} = P_{AC}/5$. Thus:

$$P_{D(MAX)} = \frac{2.25W}{5} = 0.45W$$

11. A — The dual supply circuit does **not** require an output coupling capacitor!

12. D — In Figure 5-39, $V_{\text{MAX}} = 9\text{V}$, $V_{\text{MIN}} = 0.8\text{V}$, and $V_{\text{Q}} = 4\text{V}$. Thus:

$$V_1 = \frac{V_{\text{MAX}} - V_{\text{MIN}}}{2} = \frac{9\text{V} - 0.8\text{V}}{2} = 4.1\text{V peak}$$

13. A — $V_2 = \frac{V_{\text{MAX}} + V_{\text{MIN}} - 2V_{\text{Q}}}{4} = \frac{9\text{V} + 0.8\text{V} - 2(4\text{V})}{4}$

$$V_2 = 0.45\text{V peak}$$

14. B — The percent second harmonic distortion is:

$$D_2 = \left| \frac{V_2}{V_1} \right| \times 100$$

$$D_2 = \left| \frac{0.45\text{V}}{4.1\text{V}} \right| \times 100 = 10.9\%$$

15. D — The class C amplifier has the highest efficiency.

11. The first part of the report is devoted to a description of the

12. The second part of the report is devoted to a description of the

13. The third part of the report is devoted to a description of the

14. The fourth part of the report is devoted to a description of the

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19. The ninth part of the report is devoted to a description of the

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UNIT 6

**MULTIPLE-TRANSISTOR
CIRCUITS**

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INTRODUCTION

With the exception of push-pull amplifiers, and single stage amplifiers employing Darlington and/or compound packages, the circuits examined previously were single transistor circuits. In this unit, some of the more frequently encountered multiple-transistor circuits will be examined.

Generally speaking, amplifiers may be classified as being either direct-coupled or AC coupled. The differential amplifier is a good example of the direct-coupled concept. Due to its versatility, the differential amplifier is employed extensively in both feedback systems and linear integrated circuits. Consequently, the operation of this important circuit will be discussed in detail.

Multistage amplifiers are necessary when gain, power, and/or impedance requirements cannot adequately be met by a single stage of amplification. For this reason, examples illustrating the analysis and design of two-stage AC coupled amplifiers will also be provided in this unit.

UNIT OBJECTIVES

When you have completed this unit, you should be able to:

1. Analyze and design a differential amplifier utilizing an R_E , V_{EE} current source.
2. Analyze and design a differential amplifier that utilizes one of three BJT constant current sources.
3. Analyze and design a two stage, common-emitter, RC coupled voltage amplifier.
4. Select component values for a voltage divider feedback network.
5. State how voltage series negative feedback affects R_{IN} , R_O , and A_V in a two-stage, common-emitter voltage amplifier.

UNIT ACTIVITY GUIDE

- Read section on "Differential Amplifiers".
- Answer Self-Test Review Questions 1-14.
- Perform Experiment 10 in Unit 9.
- Read section on "Cascaded Stages".
- Answer Self-Test Review Questions 15-24.
- Perform Experiment 11 in Unit 9.
- Study the Summary.
- Complete Unit Examination.
- Check Examination Answers.



DIFFERENTIAL AMPLIFIERS

Differential amplifiers are frequently used to obtain an output voltage that is directly proportional to the difference between two input voltages. For this reason, differential amplifiers are also referred to as **difference amplifiers**.

The input stage of many linear integrated circuits is a differential amplifier. Thus, the knowledge you acquire by examining a basic BJT differential amplifier will help you understand the terminology and operation of numerous linear IC's.

Basic Circuit

An elementary BJT differential amplifier is shown in Figure 6-1. Ideally, transistors T_1 and T_2 have identical characteristics. In addition, component values are selected so that $R_{C1} = R_{C2} = R_C$ and $R_{B1} = R_{B2} = R_B$.

In Figure 6-1, note that the circuit has two input terminals and two output terminals. An input can be applied to either or both bases. Similarly, outputs are available between either collector and ground. In addition, an output can also be taken **between** the two collector terminals. These various options make the differential amplifier a very versatile circuit.

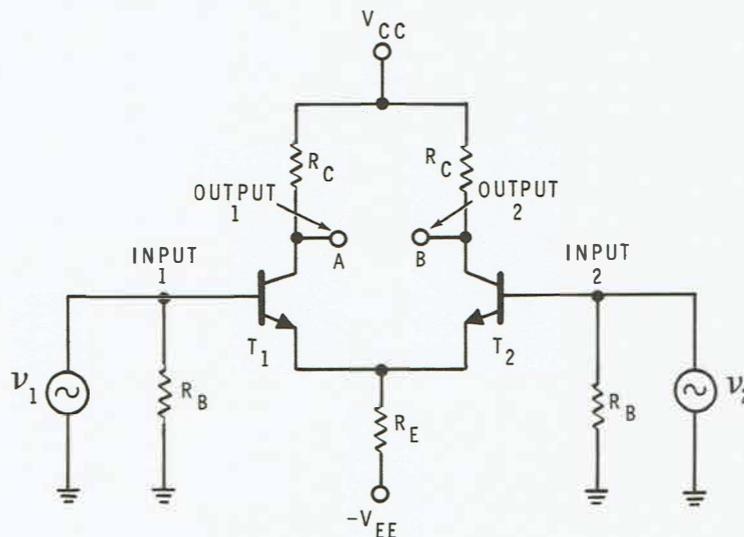


Figure 6-1

Basic differential amplifier.

DC Analysis

By removing the two signal sources, v_1 and v_2 , you obtain the DC equivalent circuit shown in Figure 6-2A. To emphasize the symmetrical nature of the circuit, R_E can be split into two components as shown in Figure 6-2B. Since $2R_E \parallel 2R_E = R_E$, it should be apparent that the circuit in Figure 6-2A is equivalent to the circuit in Figure 6-2B.

The symmetry of the differential amplifier can be employed to simplify the analysis process. The results obtained by analyzing one-half of the circuit are directly applicable to the remaining half.

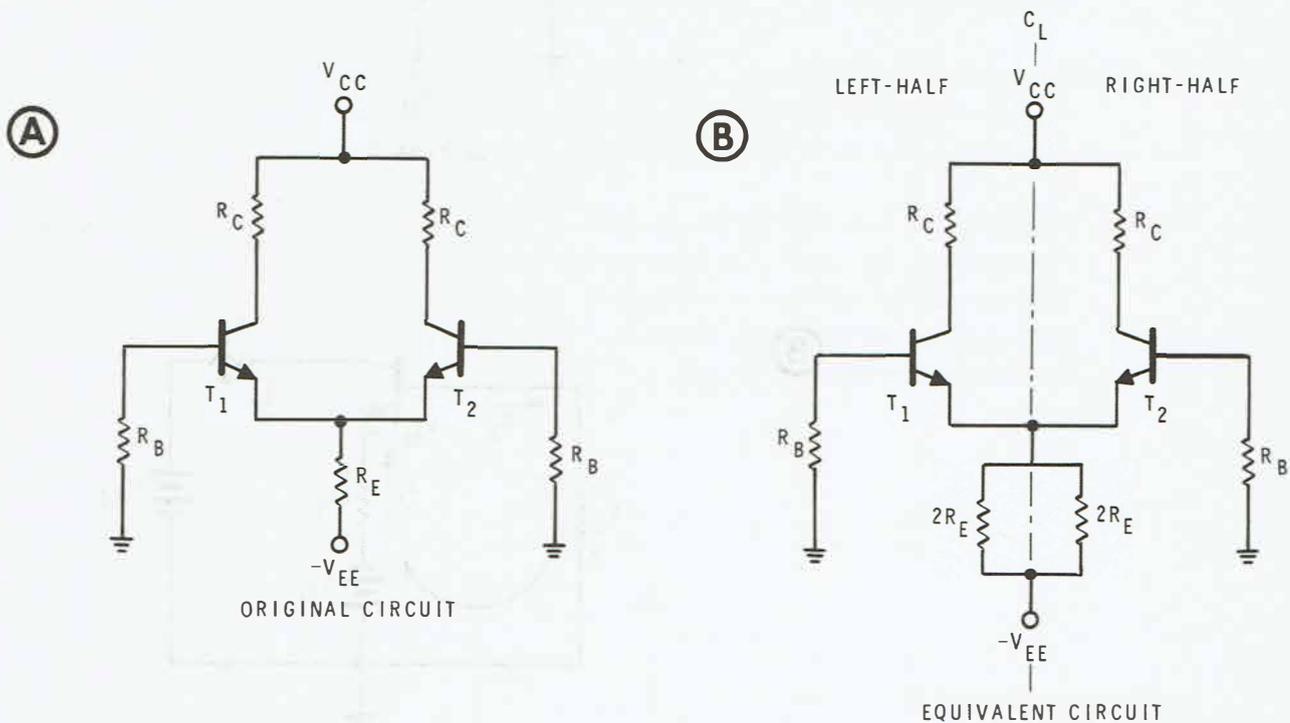
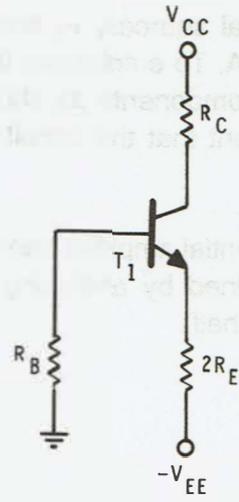


Figure 6-2

DC equivalent circuits for the BJT differential amplifier in Figure 6-1.

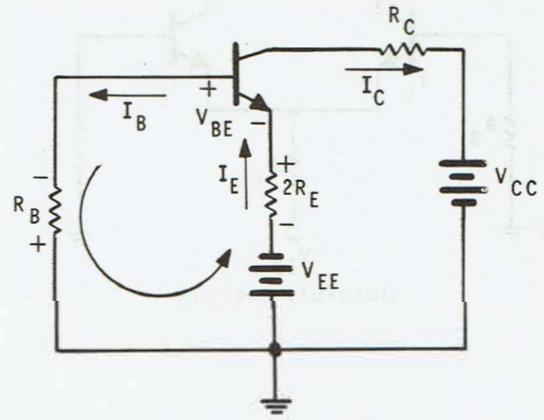
- A. Original circuit.
- B. Equivalent circuit.

(A)



LEFT-HALF

(B)



REDRAWN FOR CLARITY

Figure 6-3

DC equivalent circuits for one-half of the differential amplifier in Figure 6-2B.

- A. Left-half.
- B. Redrawn for clarity.

The DC equivalent circuit for the left half of the differential amplifier is provided in Figure 6-3A. By redrawing the circuit, you obtain the circuit shown in Figure 6-3B. Here, the loop equation for the base-emitter portion of the circuit is:

$$-I_B R_B + V_{EE} - 2I_E R_E - V_{BE} = 0$$

Substituting I_E/h_{fe} for I_B and solving for I_E yields:

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E + \frac{R_B}{h_{fe}}}$$

Assuming component values are chosen so that $2R_E \gg \frac{R_B}{h_{fe}}$, the value of I_E is approximated by:

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E} \quad (\text{Eq. 6-1})$$

Due to the circuit's symmetry, $I_E = I_{E_1} = I_{E_2}$. Since the current in the emitter resistor, R_E , equals $I_{E_1} + I_{E_2}$, we have:

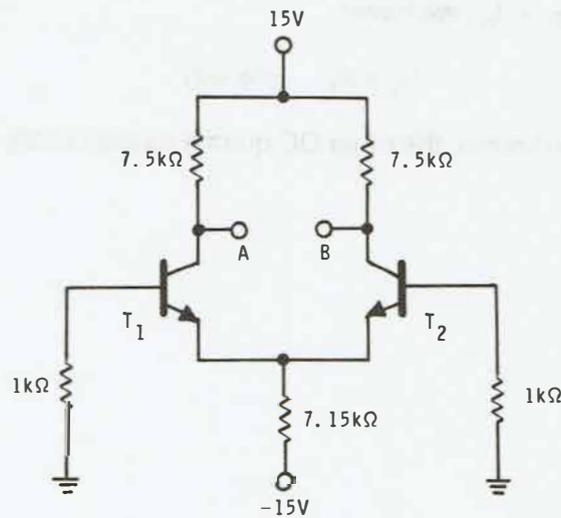
$$I_{R_E} = 2I_E \quad (\text{Eq. 6-2})$$

Once the value of I_E is known, the other DC quantities are readily determined.

Example 6-1

For the circuit shown in Figure 6-4, work out values for the following DC quantities:

- The emitter currents.
- The current flowing through R_E .
- The collector-to-ground voltages.
- The emitter-to-ground voltages.
- The collector-to-emitter voltages.
- The collector-to-collector voltage, V_{AB} .

**Figure 6-4**

Circuit for Example 6-1.

$$(a) \quad I_{E_1} = I_{E_2} = I_E = \frac{V_{EE} - V_{BE}}{2R_E} = \frac{15V - 0.7V}{2(7.15k\Omega)} = 1mA$$

$$(b) \quad I_{R_E} = 2I_E = 2(1mA) = 2mA$$

$$(c) \quad V_{C_1} = V_{C_2} = V_{CC} - I_C R_C = 15V - 1mA(7.5k\Omega) = 7.5V$$

(d) Since $I_{R_E} = 2I_E$, the emitter-to-ground voltage, V_E , is:

$$V_E = 2I_E R_E - V_{EE}$$

$$V_E = 2mA(7.15k\Omega) - 15V$$

$$V_E \approx -0.7V$$

Note that the DC emitter voltage is only slightly below ground potential. This is similar to the situation encountered in a single transistor emitter bias circuit, where V_E is typically $-0.7V$.

$$(e) \quad V_{CE} = V_C - V_E$$
$$V_{CE} = 7.5V - (-0.7V)$$
$$V_{CE} = 8.2V$$

(f) Since V_{C_1} equals V_{C_2} , the collector-to-collector voltage, $V_{C_1} - V_{C_2}$, is zero. Specifically:

$$V_{AB} = V_{C_1} - V_{C_2} = 7.5V - 7.5V = 0V$$

Current Source Model

The function of R_E and V_{EE} in the basic differential amplifier is to provide a constant current flow through R_E . Ideally, the value of this current should not change when v_1 and/or v_2 are applied to the input terminals of the amplifier. As you will see, it is important to maintain a constant value of I_{R_E} in spite of variations in v_1 , v_2 , or both v_1 and v_2 .

Since R_E and V_{EE} function as a crude "constant current source," you can visualize the basic differential amplifier as shown in Figure 6-5.

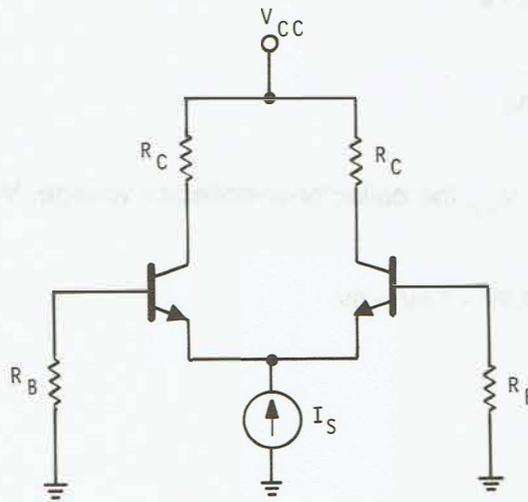


Figure 6-5

Current source representation of a differential amplifier.

Example 6-2

Show how the circuit of Example 6-1, Figure 6-4, can be analyzed using the concept of a current source model.

The original circuit is reproduced in Figure 6-6A. The value of the current flowing through R_E equals the value of I_S in the current source model. Since, I_{R_E} equals $2I_E$:

$$I_S = \frac{V_{EE} - V_{BE}}{R_E} \quad (\text{Eq. 6-3})$$

Thus:

$$I_S = \frac{15V - 0.7V}{7.15k\Omega} = 2mA$$

In this case, the current source model appears as shown in Figure 6-6B. Therefore,

$$I_E = \frac{I_S}{2} = \frac{2mA}{2} = 1mA$$

Once you know the value of I_E , you can calculate the remaining DC currents and voltages as in Example 6-1.

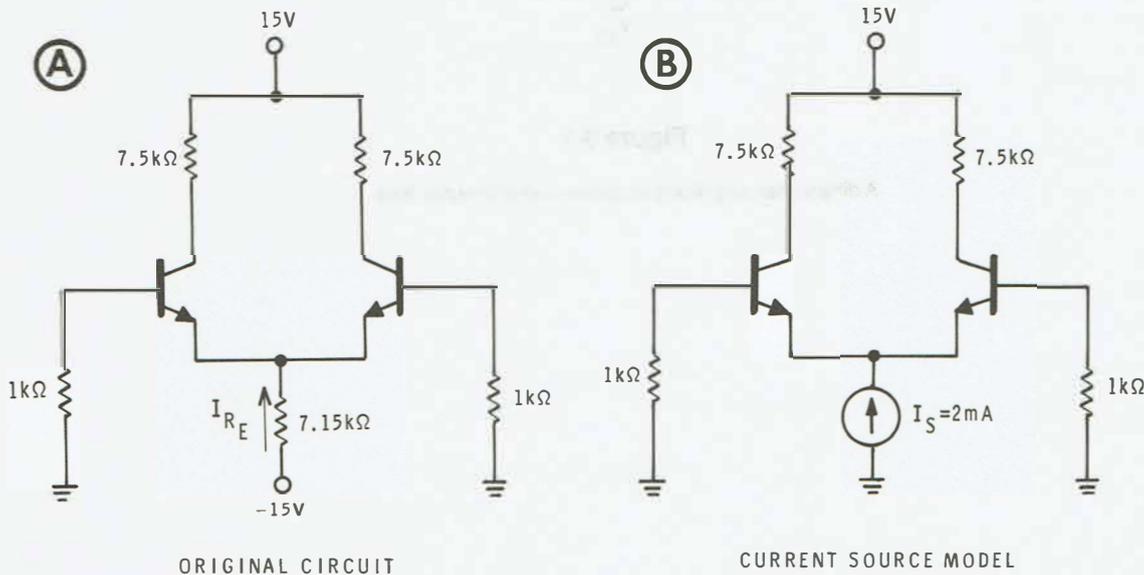


Figure 6-6

- Circuits for Example 6-2.
 A. Original circuit.
 B. Current source model.

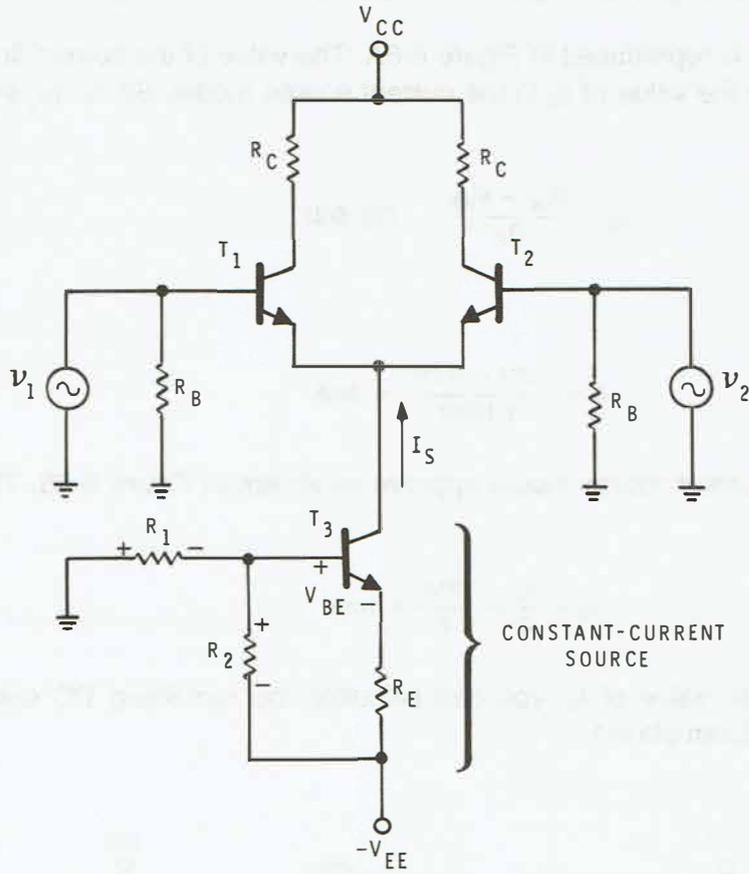


Figure 6-7

A differential amplifier that utilizes current source bias.

Current Source Bias

If you analyze the differential amplifier from an AC point of view, you will find that large values of R_E are desirable. Unfortunately, large values of R_E also require relatively large supply voltages. In addition, for a given value of I_S , large R_E values dissipate more power than do small R_E values.

A circuit that overcomes the limitations of the R_E , V_{EE} biasing scheme is illustrated in Figure 6-7. Here, transistor T_3 , resistors R_1 , R_2 , and R_E , and the voltage source, V_{EE} , function as a much improved constant current source for the differential amplifier.

The current source portion of the circuit in Figure 6-7 can be analyzed in this way:

Using voltage division:

$$V_{R_2} = \frac{V_{EE}R_2}{R_1 + R_2}$$

By inspection, the voltage across R_E equals the voltage across R_2 minus the transistor base-to-emitter voltage. Thus:

$$V_{R_E} = V_{R_2} - V_{BE}$$

Since I_{R_E} equals I_S , we have, using Ohm's law:

$$I_S = \frac{V_{R_2} - V_{BE}}{R_E}$$

Example 6-3

For the circuit shown in Figure 6-8 calculate the values of:

- (a) The source current, I_S .
- (b) The emitter current of T_1 .
- (c) The base voltage of T_3 .

$$(a) \quad V_{R_2} = \frac{V_{EE}R_2}{R_1 + R_2} = \frac{15V(10k\Omega)}{10k\Omega + 10k\Omega} = 7.5V$$

$$I_S = \frac{V_{R_2} - V_{BE}}{R_E} = \frac{7.5V - 0.7V}{3.4k\Omega} = 2mA$$

$$(b) \quad I_{E_1} = \frac{I_S}{2} = \frac{2mA}{2} = 1mA$$

Thus, both I_{E_1} and I_{E_2} equal 1mA.

- (c) The base voltage of T_3 equals the voltage across R_1 . In Figure 6-8, note that the base voltage is negative with respect to ground. Thus:

$$V_B = V_{R_1} = -7.5V$$

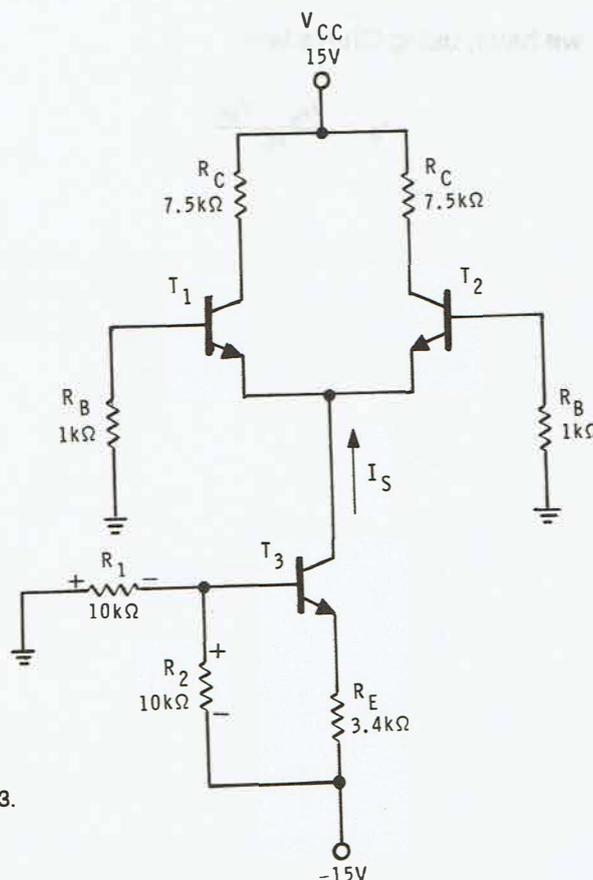


Figure 6-8

Circuit for Example 6-3.

Additional Constant Current Sources

Two popular variations of the constant-current source, in Figure 6-7, are illustrated in Figure 6-9.

In the zener diode circuit shown in Figure 6-9A:

$$V_{R_E} = V_Z - V_{BE}$$

Since $I_S \approx I_{R_E}$, we have:

$$I_S = \frac{V_Z - V_{BE}}{R_E} \quad (\text{Eq. 6-5}) \quad \text{Zener diode circuit}$$

Similarly, for the diode circuit in Figure 6-9B:

$$V_{R_2} = \frac{(V_{EE} - V_D)R_2}{R_1 + R_2} \quad (\text{Eq. 6-6})$$

$$V_{R_E} = -V_{BE} + V_D + V_{R_2}$$

Since the diode voltage, V_D , and the transistor's base-to-emitter voltage, V_{BE} , are approximately equal, the voltage across R_E essentially equals the voltage across R_2 . Thus:

$$V_{R_E} \approx V_{R_2}$$

Therefore, the current produced by the constant-current source is:

$$I_S = I_{R_E} = \frac{V_{R_2}}{R_E} \quad (\text{Eq. 6-7})$$

The zener diode circuit stabilizes I_S against supply voltage and temperature variations by providing a stable reference voltage. Similarly, the diode circuit minimizes the effects of variations in V_{BE} since the voltage drop across the diode, V_D , effectively cancels the transistor's base-to-emitter voltage, V_{BE} .

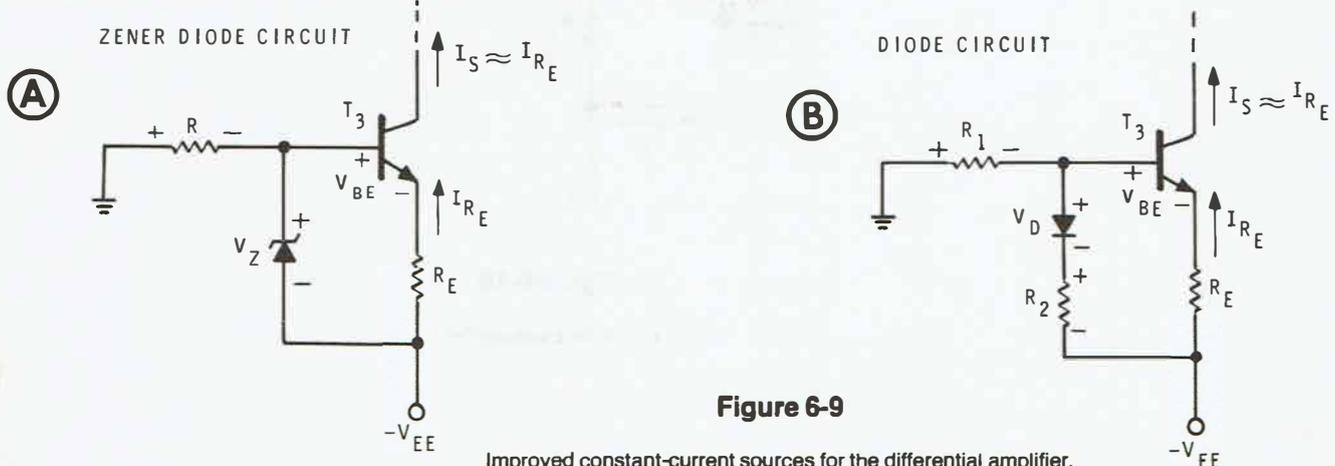


Figure 6-9

Improved constant-current sources for the differential amplifier.

- A. Zener diode circuit.
- B. Diode circuit.

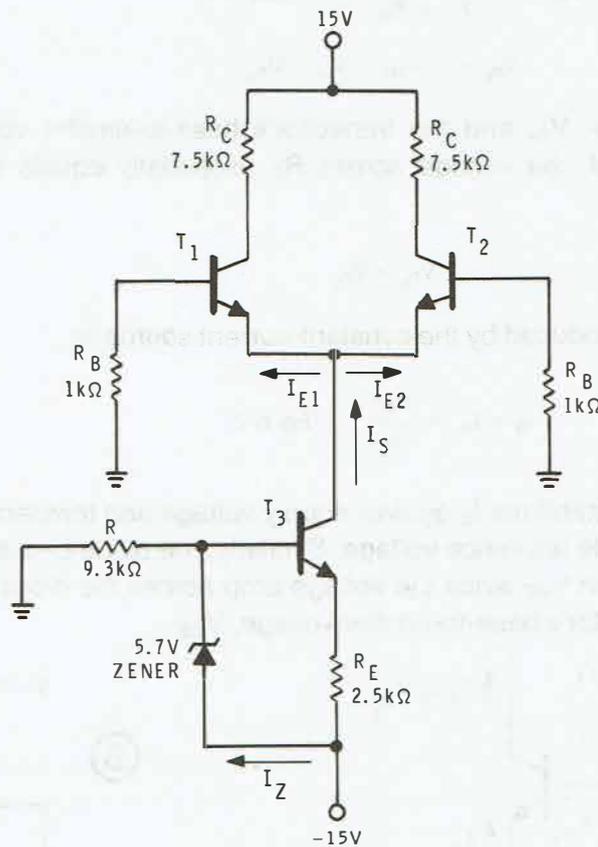
Example 6-4

Calculate the source current, I_S , zener current, I_Z , and emitter currents for the circuit shown in Figure 6-10.

$$I_S = \frac{V_Z - V_{BE}}{R_E} = \frac{5.7V - 0.7V}{2.5k\Omega} = 2mA$$

$$I_Z = I_R = \frac{V_{EE} - V_Z}{R} = \frac{15V - 5.7V}{9.3k\Omega} = 1mA$$

$$I_E = \frac{I_S}{2} = \frac{2mA}{2} = 1mA = I_{E1} = I_{E2}$$

**Figure 6-10**

Circuit for Example 6-4.

Example 6-5

What value of I_S is produced by the constant-current source in Figure 6-11?

$$V_{R_2} = \frac{(V_{EE} - V_D)R_2}{R_1 + R_2}$$

Assuming $V_D = 0.7V$:

$$V_{R_2} = \frac{(10V - 0.7V)6.8k\Omega}{3.3k\Omega + 6.8k\Omega} = \frac{9.3V(6.8k\Omega)}{10.1k\Omega} = 6.26V$$

$$I_S = \frac{V_{R_2}}{R_E} = \frac{6.26V}{2k\Omega} = 3.13mA$$

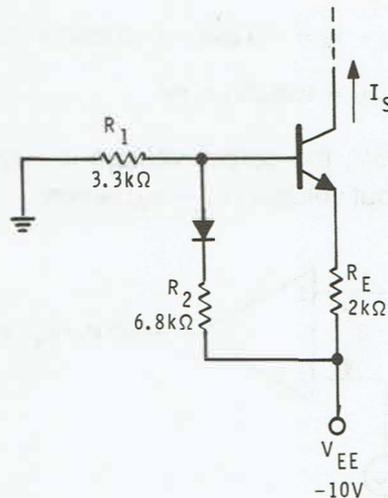


Figure 6-11

Current source for Example 6-5.

AC Analysis

An “exact” AC analysis of the basic differential amplifier in Figure 6-1 is surprisingly complex. However, by employing a few new concepts and considering the symmetrical nature of the circuit, it is possible to derive a number of approximate, but useful, formulas.

DIFFERENTIAL-MODE VOLTAGE

The output voltage taken between the two collectors in Figure 6-1 ideally depends upon the product of the amplifier's voltage gain, A_d , and the difference between the two input voltages ($V_1 - V_2$). This concept is illustrated in Figure 6-12, where the triangular symbol is used to represent the differential amplifier. Here, the difference voltage ($V_1 - V_2$) is referred to as the **differential input voltage**, v_d . Stated mathematically:

$$\left. \begin{aligned} v_d &= v_1 - v_2 && \text{(Eq. 6-8)} \\ v_o &= A_d v_d && \text{(Eq. 6-9)} \end{aligned} \right\} \text{Ideal differential amplifier.}$$

For example, if $v_1 = +0.25\text{V}$, $v_2 = -0.25\text{V}$, and $A_d = 10$, the output voltage in Figure 6-12 would be calculated as follows:

$$\begin{aligned} v_d &= v_1 - v_2 = +0.25\text{V} - (-0.25\text{V}) = 0.5\text{V} \\ v_o &= A_d v_d = 10(0.5\text{V}) = 5\text{V} \end{aligned}$$

Similarly, if $v_1 = v_2 = 0.25\text{V}$, the output voltage in Figure 6-12 would be zero volts since the differential input voltage ($v_1 - v_2$) is zero.

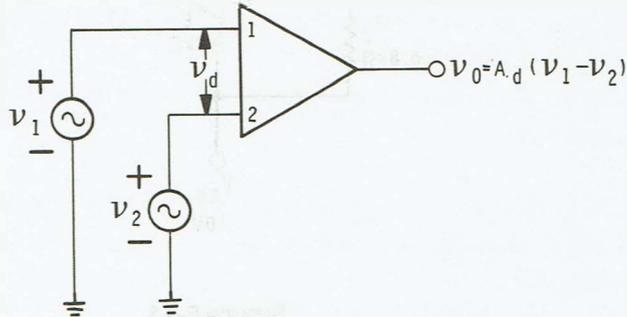


Figure 6-12

The ideal differential amplifier.

Example 6-6

In Figure 6-12, $v_1 = 1.25\text{V}$, $v_2 = 0.75\text{V}$, and $A_d = 10$. Calculate the output voltage, v_o , assuming the amplifier is ideal.

$$\begin{aligned} v_d &= v_1 - v_2 = 1.25\text{V} - 0.75\text{V} = 0.5\text{V} \\ v_o &= A_d v_d = 10(0.5\text{V}) = 5\text{V} \end{aligned}$$

Since the differential input voltage was the same as the previous example, the output voltage is also the same, 5V.

COMMON-MODE VOLTAGES

By definition, the **common-mode voltage**, v_{CM} , is the **average value** of the two input voltages to a differential amplifier. Stated mathematically:

$$v_{CM} = \frac{v_1 + v_2}{2} \quad (\text{Eq. 6-10})$$

By solving Equation 6-8 and Equation 6-10 for v_1 and v_2 in terms of v_d and v_{CM} , you obtain:

$$v_1 = v_{CM} + \frac{v_d}{2} \quad (\text{Eq. 6-11})$$

$$v_2 = v_{CM} - \frac{v_d}{2} \quad (\text{Eq. 6-12})$$

You can appreciate the significance of these equations by referring to Figure 6-13. In Figure 6-13A, v_1 and v_2 are applied to the input terminals of the differential amplifier. Here:

1. The voltage from terminal A to ground equals v_1 .
2. The voltage from terminal B to ground equals v_2 .
3. The voltage between terminals A and B, the differential input voltage, equals $v_1 - v_2$.

Equation 6-11 and Equation 6-12 suggest the equivalent circuit shown in Figure 6-13B. Here, each input voltage is thought of as containing both a differential-mode, $v_{d/2}$, and common-mode, v_{CM} , component. The following example verifies the equivalence of the circuit in Figure 6-13A and Figure 6-13B.

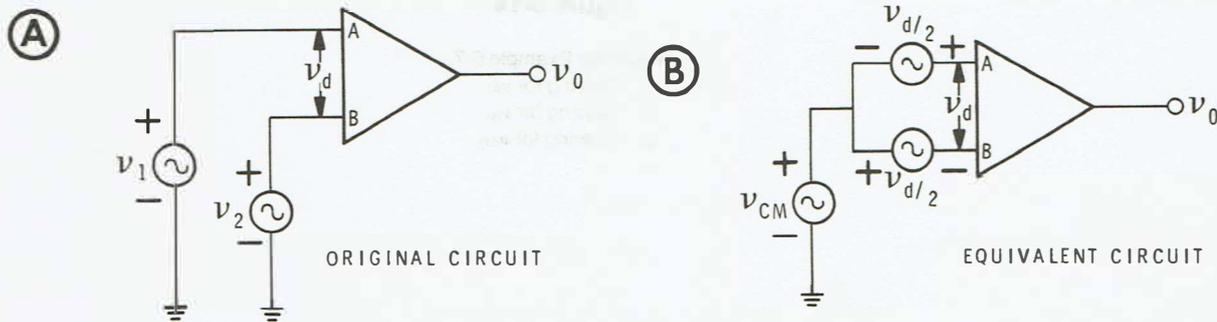
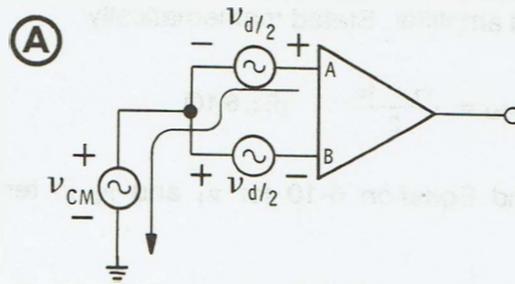
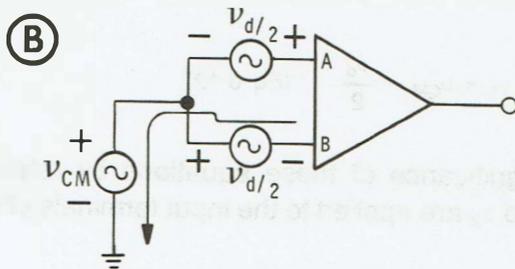
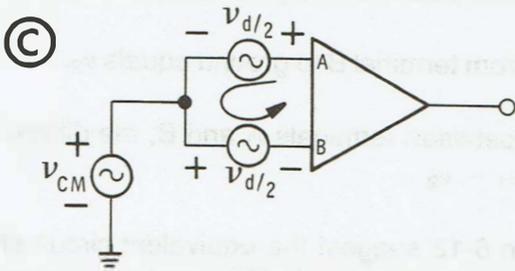


Figure 6-13

The input voltages, v_1 and v_2 , in A can be represented by differential and common-mode components as shown in B.
 A. Original circuit.
 B. Equivalent circuit.

SOLVING FOR v_A SOLVING FOR v_B SOLVING FOR v_{AB} **Figure 6-14**

Circuits for Example 6-7.

- A. Solving for v_A .
- B. Solving for v_B .
- C. Solving for v_{AB} .

Example 6-7

In Figure 6-13A $v_A = v_1$, $v_B = v_2$, and $v_{AB} = v_1 - v_2$. Show that the same values are obtained for the circuit in Figure 6-13B.

The circuit in Figure 6-13B is redrawn in Figure 6-14. By following the path indicated from terminal A to ground in Figure 6-14A, you obtain:

$$v_A = \frac{v_d}{2} + v_{CM}$$

Substituting $v_1 - v_2$ for v_d and $\frac{v_1 + v_2}{2}$ for v_{CM} yields:

$$v_A = \frac{v_1 - v_2}{2} + \frac{v_1 + v_2}{2} = \frac{2v_1}{2} = v_1$$

Similarly, through the path shown in Figure 6-14B:

$$v_B = \frac{-v_d}{2} + v_{CM}$$

$$v_B = \frac{-v_1 + v_2}{2} + \frac{v_1 + v_2}{2} = \frac{2v_2}{2} = v_2$$

Finally, referring to Figure 6-14C:

$$v_{AB} = \frac{v_d}{2} + \frac{v_d}{2} = v_d = v_1 - v_2$$

Since the terminal-to-ground and terminal-to-terminal voltages in Figure 6-13A and Figure 6-13B are identical, we conclude that the voltage sources in Figure 6-13A can be represented as shown in Figure 6-13B.

Practical Differential Amplifiers

Due to the fact that real components cannot be matched exactly, the two halves of a practical differential amplifier are not exactly the same. For this reason, the output voltage depends upon both the differential and common-mode components of the input voltages. Specifically, the output voltage of a practical differential amplifier is described as follows:

$$v_o = A_d v_d + A_{CM} v_{CM} \quad (\text{Eq. 6-13})$$

Where: v_d = differential input voltage = $v_1 - v_2$

$$v_{CM} = \text{common-mode input voltage} = \frac{v_1 + v_2}{2}$$

A_d = differential voltage gain.

A_{CM} = common-mode voltage gain.

It is important to remember that, in real differential amplifiers, equal differential input voltages do not necessarily result in equal output voltages.

The following example illustrates this concept.

Example 6-8

A differential amplifier has a differential voltage gain, A_d , of 10 and a common-mode voltage gain, A_{CM} , of 0.1. Estimate the output voltage for the following input voltages:

$$(a) \quad v_1 = +0.25V, v_2 = -0.25V$$

$$(b) \quad v_1 = v_2 = 0.25V$$

$$(c) \quad v_1 = 1.25V, v_2 = 0.75V$$

$$(a) \quad v_d = v_1 - v_2 = +0.25V - (-0.25V) = 0.5V$$

$$v_{CM} = \frac{v_1 + v_2}{2} = \frac{+0.25V + (-0.25V)}{2} = 0V$$

Note that when $v_1 = -v_2$, the common-mode component of the input voltage is zero.

$$\begin{aligned} v_o &= A_d v_d + A_{CM} v_{CM} \\ v_o &= 10(0.5V) + 0.1(0V) = 5V \end{aligned}$$

In this case, a differential input voltage of 0.5V results in a 5V output voltage.

$$(b) \quad v_d = v_1 - v_2 = 0.25V - 0.25V = 0V$$

$$v_{CM} = \frac{v_1 + v_2}{2} = \frac{0.25V + 0.25V}{2} = 0.25V$$

Note that when $v_1 = v_2$, the differential input voltage is zero. Ideally, the output voltage should also be zero. However, since a real differential amplifier responds to both the differential and common-mode input components, we have:

$$v_o = A_d v_d + A_{CM} v_{CM}$$

$$v_o = 10(0V) + 0.1(0.25V) = 0.025V$$

$$(c) \quad v_d = v_1 - v_2 = 1.25V - 0.75V = 0.5V$$

$$v_{CM} = \frac{v_1 + v_2}{2} = \frac{1.25V + 0.75V}{2} = 1V$$

Note that the differential input voltage, 0.5V, is the same as in (a). In this case, however, the output voltage is:

$$v_o = A_d v_d + A_{CM} v_{CM}$$

$$v_o = 10(0.5V) + 0.1(1V) = 5.1V$$

Common Mode Rejection Ratio

Since the ideal differential amplifier is perfectly balanced, its common-mode voltage gain is zero. Thus, the ideal differential amplifier only responds to differential input signals. Common-mode signals are completely rejected by the amplifier.

Real differential amplifiers respond to both differential- and common-mode signals. Clearly, a practical differential amplifier is one whose differential-mode voltage gain is large compared to its common-mode voltage gain.

A measure of how close the characteristics of a real differential amplifier are to those of the ideal differential amplifier is given by the ratio of the amplifier's differential- and common-mode voltage gains. This ratio is called the **common mode rejection ratio, CMRR**, and is defined as follows:

$$CMRR = \frac{A_d}{A_{CM}} \quad (\text{Eq. 6-14})$$

Obviously, large values of CMRR are desirable. Frequently, the CMRR of a differential amplifier is expressed in decibels rather than as a simple numeric ratio. Specifically:

$$CMRR_{dB} = 20 \log CMRR \quad (\text{Eq. 6-15})$$

Example 6-9

Calculate the CMRR for the amplifier in Example 6-8:

$$\text{CMRR} = \frac{A_d}{A_{CM}} = \frac{10}{0.1} = 100$$

Expressed in decibels:

$$\begin{aligned}\text{CMRR}_{\text{dB}} &= 20 \log \text{CMRR} \\ \text{CMRR}_{\text{dB}} &= 20 \log 100 = 40\text{dB}\end{aligned}$$

Noise

The common-mode component of the input voltages to a differential amplifier is effectively applied to both inputs of the amplifier, as illustrated previously in Figure 6-13B. For this reason, any signal that is simultaneously applied to both inputs will appear as a common-mode signal to the amplifier. As you know, differential amplifiers tend to reject common-mode signals.

Sources of electrical noise are both varied and numerous. Typical noise sources include electric motors, lightning, incandescent light dimmers, fluorescent lights, and power supplies. Frequently, these and other noise sources induce unwanted voltages in leads connected between a signal source and the input terminals of an amplifier.

Noise-induced voltages are amplified along with the signal voltage by most amplifiers. Thus, when the amplitude of the induced noise voltage is on the same order of magnitude or larger than the signal voltage, the output voltage from a conventional amplifier will be a highly distorted waveform.

Differential amplifiers have excellent noise immunity. This is because the noise voltages induced in each of the two amplifier input leads are essentially equal. Consequently, the induced noise voltages appear as a common-mode signal to the differential amplifier and are rejected.

Useful Formulas

The left half of the basic differential amplifier is reproduced in Figure 6-15A. Here, we are assuming that a common-mode voltage is applied to the input of the amplifier. The AC equivalent circuit is shown in Figure 6-15B. By following the path indicated by this dotted line you obtain:

$$v_{CM} - 2i_e R_E - i_e r_{e'} = 0$$

Solving for i_e :

$$i_e = \frac{v_{CM}}{2R_E + r_{e'}} \approx i_C$$

$$v_C = -i_C R_C = \frac{-v_{CM} R_C}{2R_E + r_{e'}}$$

The ratio of v_C to v_{CM} , A_{CM} , is therefore:

$$A_{CM} = - \frac{R_C}{2R_E + r_{e'}} \quad (\text{Eq. 6-16})$$

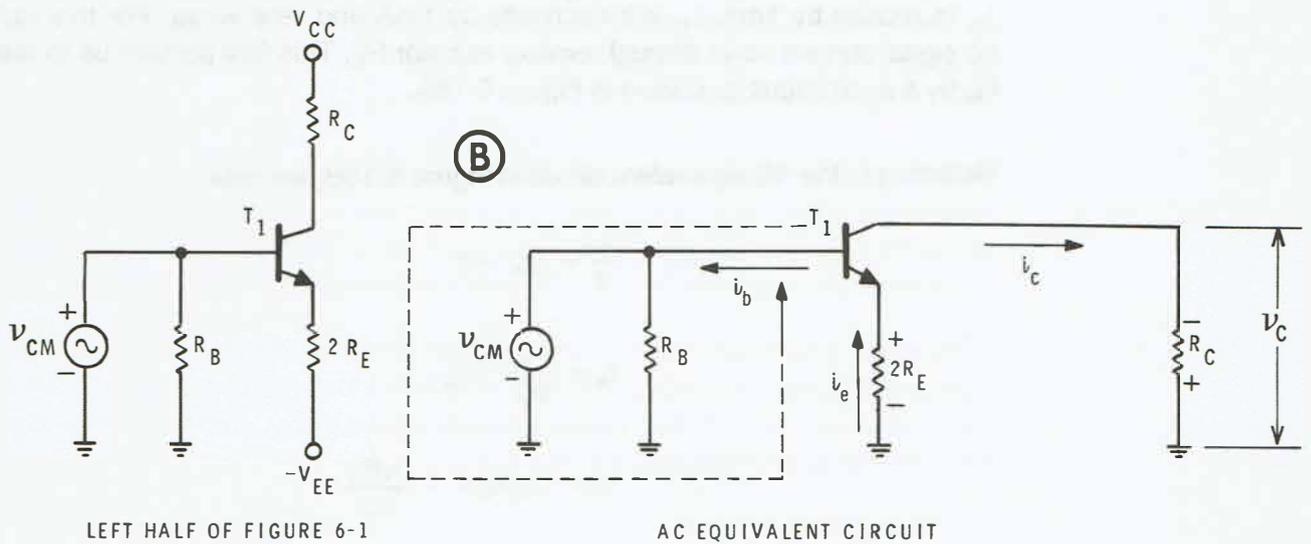


Figure 6-15

Circuits for deriving an expression for A_{CM} .

- A. Left-half of Figure 6-1.
- B. AC equivalent circuit.

Assuming component values are chosen so that $2R_E \gg r_{e'}$, Equation 6-16 is closely approximated by:

$$A_{CM} = -\frac{R_C}{2R_E} \quad (\text{Eq. 6-17})$$

To obtain a small value of A_{CM} , R_E should be large. Increasing the value of R_E , however, requires a larger V_{EE} supply voltage. Thus, the values chosen for V_{EE} and R_E represent a common-mode voltage gain/supply voltage compromise.

If current source bias is employed, the effective value of R_E in Equation 6-17 approximately equals the value of $r_{C'}$. Thus:

$$A_{CM} = -\frac{R_C}{2r_{C'}} \quad (\text{Eq. 6-18}) \quad \text{Current source bias}$$

Since $r_{C'}$ is usually very large compared to R_C , the common-mode voltage gain of a differential amplifier employing current source bias is quite small — which of course is desirable.

To calculate the differential voltage gain, v_{CM} is assumed to be zero. When $v_1 = v_d/2$ and $v_2 = v_d/2$, the changes in i_{e_1} and i_{e_2} are complementary. Thus, if i_{e_1} increases by 1mA, i_{e_2} will decrease by 1mA and vice versa. For this reason, no signal current flows through emitter resistor R_E . This fact permits us to replace R_E by a short circuit as shown in Figure 6-16A.

Referring to the AC equivalent circuit in Figure 6-16B, we note:

$$\frac{v_d}{2} - i_e r_{e'} = 0$$

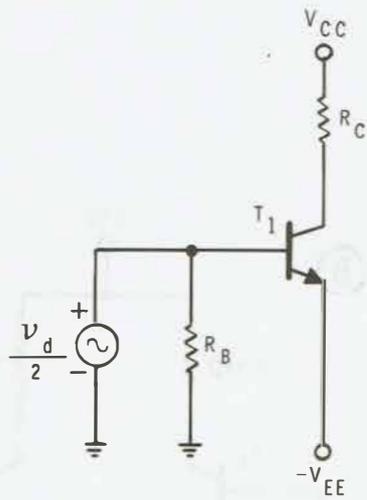
$$i_e = \frac{v_d}{2r_{e'}} \approx i_C$$

$$v_C = -i_C R_C = -\frac{v_d R_C}{2r_{e'}}$$

The differential voltage gain, A_d , is therefore:

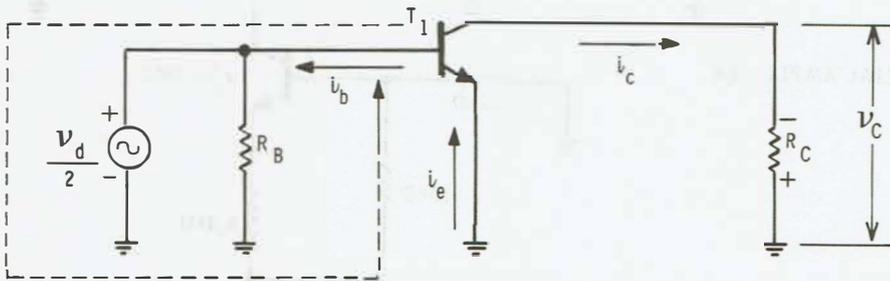
$$A_d = \frac{v_C}{v_d} = -\frac{R_C}{2r_{e'}} \quad (\text{Eq. 6-19})$$

(A)



ORIGINAL CIRCUIT

(B)



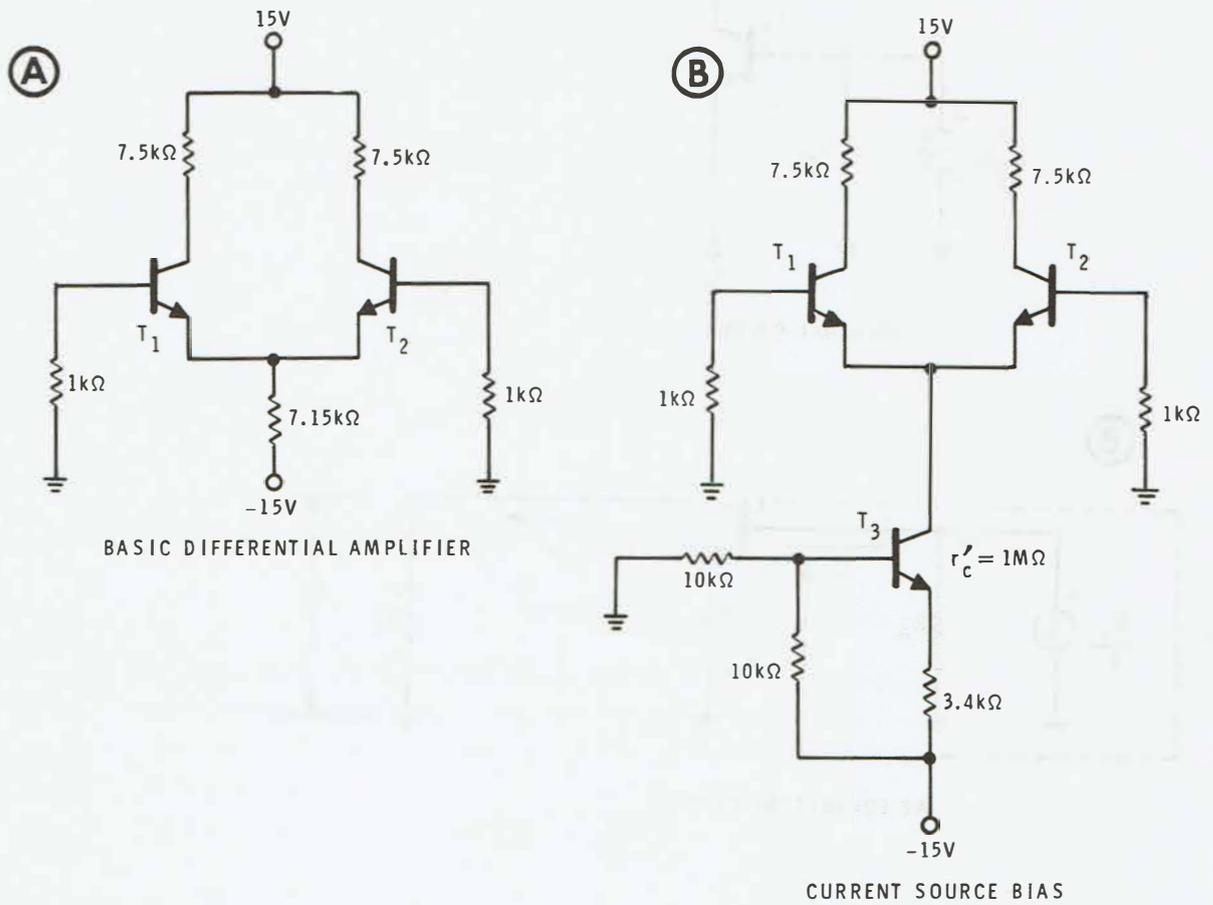
AC EQUIVALENT CIRCUIT

Figure 6-16

Circuits for deriving an expression for A_d .

A. Original circuit.

B. AC equivalent circuit.

**Figure 6-17**

Circuits for Example 6-10.

- A. Basic differential amplifier.
- B. Current source bias.

Example 6-10

The circuits shown in Figure 6-17A and Figure 6-17B were partially analyzed in Example 6-1 and Example 6-3 respectively. Recall that in both circuits $I_{E_1} = I_{E_2} = 1\text{mA}$. Based on this fact, calculate the differential voltage gain, common-mode voltage gain, and the common-mode rejection ratio of each circuit.

For the basic differential amplifier:

$$r_{e'} = \frac{37\text{mV}}{I_E} = \frac{37\text{mV}}{1\text{mA}} = 37\Omega$$

$$A_d = -\frac{R_C}{2r_{e'}} = -\frac{7.5\text{k}\Omega}{2(37\Omega)} = -101.3$$

$$A_{CM} = -\frac{R_C}{2R_E} = -\frac{7.5\text{k}\Omega}{2(7.15\text{k}\Omega)} = -0.524$$

$$\text{CMRR} = \frac{A_d}{A_{CM}} = \frac{101.3}{0.524} = 193.3$$

$$\text{CMRR}_{\text{dB}} = 20 \log 193.3 = 45.7\text{dB}$$

Since the current source bias circuit has the same values of R_C and $r_{e'}$ as the basic circuit, $A_d = -101.3$. Also, since $r_{C'}$ for $T_3 = 1\text{M}\Omega$, the common-mode voltage gain, A_{CM} , is:

$$A_{CM} = \frac{-R_C}{2r_{C'}} = \frac{-7.5\text{k}\Omega}{2(1\text{M}\Omega)} = -0.00375$$

Thus:

$$\text{CMRR} = \frac{A_d}{A_{CM}} = \frac{101.3}{0.00375} = 27013.3$$

$$\text{CMRR}_{\text{dB}} = 20 \log 27013.3 = 86.67\text{dB}$$

Obviously, the use of current source bias provides superior common-mode rejection.

Mode of Operation

Since the differential amplifier has two input and two output terminals, a number of operating modes are possible. The simplest mode is the **single-input, single-output** arrangement. In this mode, a single input voltage, v_1 , or v_2 , is applied to the base of either T_1 or T_2 in the "differential pair." The output voltage is then taken from the collector of either T_1 or T_2 . To illustrate the various operating modes, let's examine the circuit shown in Figure 6-18.

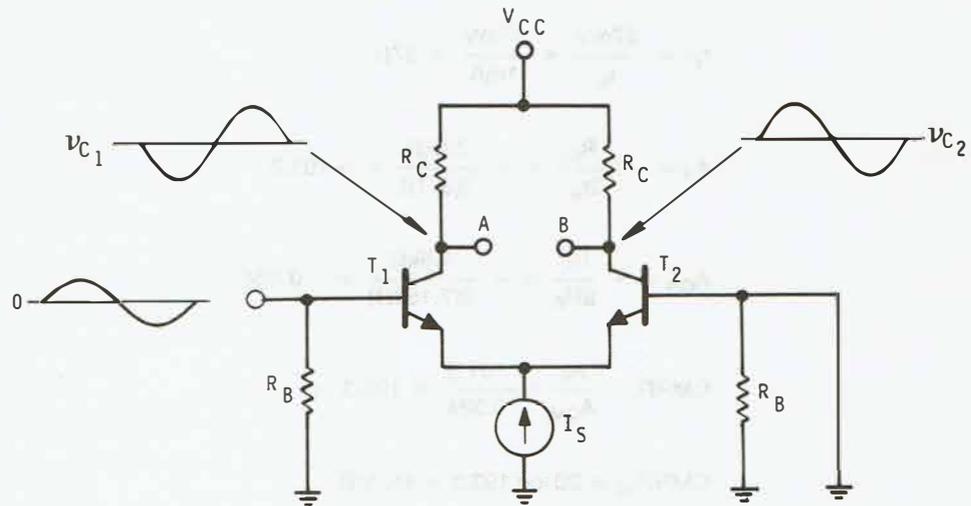


Figure 6-18

Single-input signal waveforms.

SINGLE-INPUT, SINGLE-OUTPUT MODE

In Figure 6-18 a single input voltage, v_1 , is applied to the base of T_1 . Since the base of T_2 is grounded, v_2 equals 0. Therefore, the amplifier sees a differential input voltage of $(v_1 - 0)$, or v_1 .

The signal at the collector of T_1 equals the differential voltage gain, $-R_C/2r_e'$, times the differential input voltage, v_1 . Thus, the voltage appearing at the collector of T_1 is an amplified but **inverted** version of v_1 .

Changes in v_1 produce changes in the emitter current in T_1 . Since the emitter of T_1 is connected directly to the emitter of T_2 and since I_S is constant, the emitter current in T_2 must follow the changes in the emitter current in T_1 . For this reason, T_2 acts like a common-base amplifier. Thus, the voltage appearing at the collector of T_2 is an amplified — **in phase** version of v_1 . The amplitude of v_{C_1} and v_{C_2} are, ideally, equal. Thus, in the single-input, single-output mode, you have a choice of selecting either an in-phase or inverted output voltage. In each case, the output voltage is approximately $R_C/2r_e'$ times larger than the input voltage.

SINGLE-INPUT, DIFFERENTIAL-OUTPUT MODE

In Figure 6-18, the collector voltages are of equal amplitude but opposite phase. For this reason, the signal voltage between the collectors, v_{AB} , will be **double the value** of either collector-to-ground voltage. Specifically:

$$v_{AB} = v_{C_1} - v_{C_2}$$

Substituting $-v_{C_1}$ for v_{C_2} yields:

$$v_{AB} = v_{C_1} - (-v_{C_1}) = 2v_{C_1}$$

Therefore, by taking the output voltage between the two collector terminals, the voltage gain of the circuit is effectively doubled. Thus, for a differential output voltage:

$$A_d = 2 \frac{R_C}{2r_e'} = \frac{R_C}{r_e'}$$

DUAL-INPUT, SINGLE-OUTPUT MODE

When two voltages, v_1 and v_2 , are applied to the inputs of a differential amplifier, the differential input voltage equals $(v_1 - v_2)$. Consequently, the signal appearing at the collector of T_2 equals $R_C/2r_e'$ times $(v_1 - v_2)$.

Thus, as was the case with the single-input, single-output mode, you have a choice of selecting either an in-phase or inverted output voltage. In this case, however, the output voltage is an amplified version of the **difference** between the two input voltages.

DUAL-INPUT, DIFFERENTIAL-OUTPUT MODE

Once again, the effective voltage gain is doubled when the output voltage is taken between the two collector terminals. In this mode:

$$v_{AB} = \frac{R_C}{r_e'} (v_1 - v_2)$$

DIFFERENTIAL-INPUT, SINGLE- AND DIFFERENTIAL-OUTPUT MODES

A **single-ended** voltage is a voltage between an ungrounded point and ground. Both v_1 and v_2 are examples of single-ended voltages. A **differential** voltage is a voltage that exists between two ungrounded points. The difference voltage ($v_1 - v_2$) is an example of a differential voltage.

The output voltage from a Wheatstone bridge is another example of a differential voltage. Since measurement systems frequently employ bridge circuits, differential amplifiers are normally used to amplify the system's differential output voltage. In addition, the large CMRR of the differential amplifier minimizes the problems encountered when the measurement system is in a noisy environment.

A differential amplifier that can be used to directly amplify a differential input voltage is illustrated in Figure 6-19. Here, single-ended output signals are available at either collector. Similarly, a differential output signal results when the output is taken between the two collector terminals. As you might expect, v_{C_1} equals $-R_C/r_e'$ times v_{IN} and v_{C_2} equals $R_C/2r_e'$ times v_{IN} . Consequently, the differential-output voltage equals $(v_{C_1} - v_{C_2})$ or R_C/r_e' times v_{IN} .

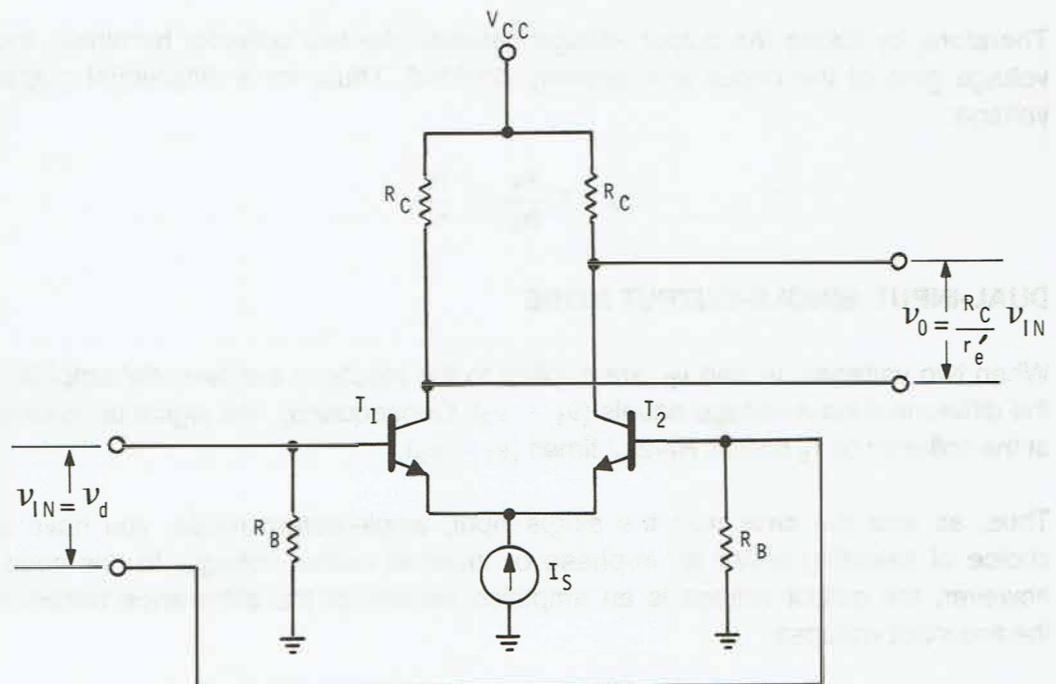


Figure 6-19

Differential-input, differential-output mode. Note that single-output signals are available at each collector.

The various operating modes are summarized in Table 6-1. Here, the **magnitude** of the output voltage(s) are provided in column four. Naturally, the phase of a particular output voltage depends upon the specific input and output terminals employed.

Table 6-1

Differential Amplifier operating modes.

Mode	(v_{IN}) Input Voltage(s)	(v_d) Differential Voltage	(v_o) Output Voltage
Single-Input, Single-Output	v_1 OR v_2	v_1 OR v_2	$\frac{R_C}{2r_{e'}} v_{IN}$
Single-Input, Differential-Output	v_1 OR v_2	v_1 OR v_2	$\frac{R_C}{r_{e'}} v_{IN}$
Dual-Input, Single-Output	v_1 and v_2	$(v_1 - v_2)$	$\frac{R_C}{2r_{e'}} (v_1 - v_2)$
Dual-Input, Differential-Output	v_1 and v_2	$(v_1 - v_2)$	$\frac{R_C}{r_{e'}} (v_1 - v_2)$
Differential-Input, Single-Output	v_{IN}	v_{IN}	$\frac{R_C}{2r_{e'}} v_{IN}$
Differential-Input, Differential-Output	v_{IN}	v_{IN}	$\frac{R_C}{r_{e'}} v_{IN}$

Input and Output Resistances

The derivation of “exact” formulas for the input and output resistances of the differential amplifier is quite complex. In most cases, the following approximate formulas are adequate.

The input resistances seen by v_1 and v_2 are approximately:

$$R_{IN_1} = R_{IN_2} = 2h_{fe}r_e' \parallel R_B \quad (\text{Eq. 6-20})$$

The input resistance seen by a differential input signal, v_d , is approximately:

$$R_{IN_d} = 4h_{fe}r_e' \parallel R_B \quad (\text{Eq. 6-21})$$

The approximate output resistance looking back into the circuit from either collector terminal is:

$$R_{O_1} = R_{O_2} = R_C \quad (\text{Eq. 6-22})$$

Similarly, for a differential output connection, the resistance seen looking back into the two collector terminals is approximately:

$$R_{O_d} = 2R_C \quad (\text{Eq. 6-23})$$

Example 6-11

In many applications, the signals applied to the inputs of a differential amplifier are complementary, as shown in Figure 6-20. For the given input signals, predict:

- (a) *The collector voltage at T_1 .*
- (b) *The collector voltage at T_2 .*
- (c) *The voltage developed between the collectors of T_1 and T_2 .*
- (d) *The input resistance seen by v_1 and v_2 .*
- (e) *The output resistance; assuming the output signal is taken between the two collector terminals.*

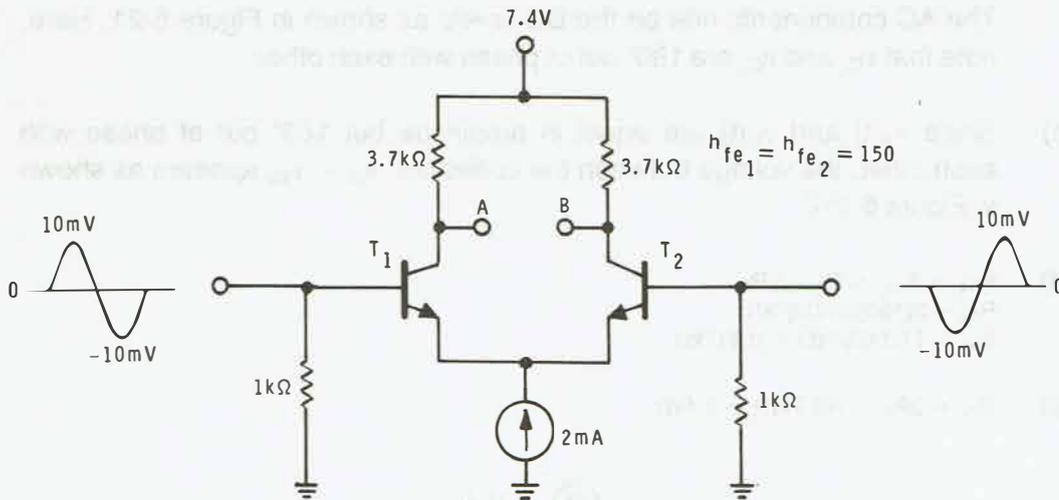


Figure 6-20

Circuit for Example 6-11.

(a,b) Since $I_S = 2\text{mA}$, the DC emitter current in each transistor is $2\text{mA}/2$ or 1mA . The DC collector-to-ground voltages are therefore:

$$V_C = V_{CC} - I_C R_C$$

$$V_C = 7.4\text{V} - 1\text{mA}(3.7\text{k}\Omega) = 3.7\text{V}$$

Table 6-1 indicates that, for dual inputs, v_d equals $(v_1 - v_2)$. In this case, $v_2 = -v_1$. Thus:

$$v_d = (v_1 - v_2) = 10\text{mV} - (-10\text{mV}) = 20\text{mV peak}$$

Since $I_E = 1\text{mA}$, the values of $r_{e'}$ and A_d are calculated as follows:

The **magnitude** of A_d equals $R_C/2r_{e'}$. Thus:

$$A_d = \frac{R_C}{2r_{e'}} = \frac{3.7\text{k}\Omega}{2(37\Omega)} = 50$$

The peak values of the AC collector voltages are therefore:

$$v_C = A_d v_d = 50(20\text{mV}) = 1\text{V peak}$$

The AC components ride on the DC levels as shown in Figure 6-21. Here, note that v_{C_1} and v_{C_2} are 180° out of phase with each other.

- (c) Since $v_A(t)$ and $v_B(t)$ are equal in amplitude but 180° out of phase with each other, the voltage between the collectors, $v_A - v_B$, appears as shown in Figure 6-21C.

(d) $R_{IN_1} = R_{IN_2} = 2h_{fe}r_e' \parallel R_B$
 $R_{IN} = 2(150)(37\Omega) \parallel 1k\Omega$
 $R_{IN} = 11.1k\Omega \parallel 1k\Omega = 0.917k\Omega$

(e) $R_{O_1} = 2R_C = 2(3.7k\Omega) = 7.4k\Omega$

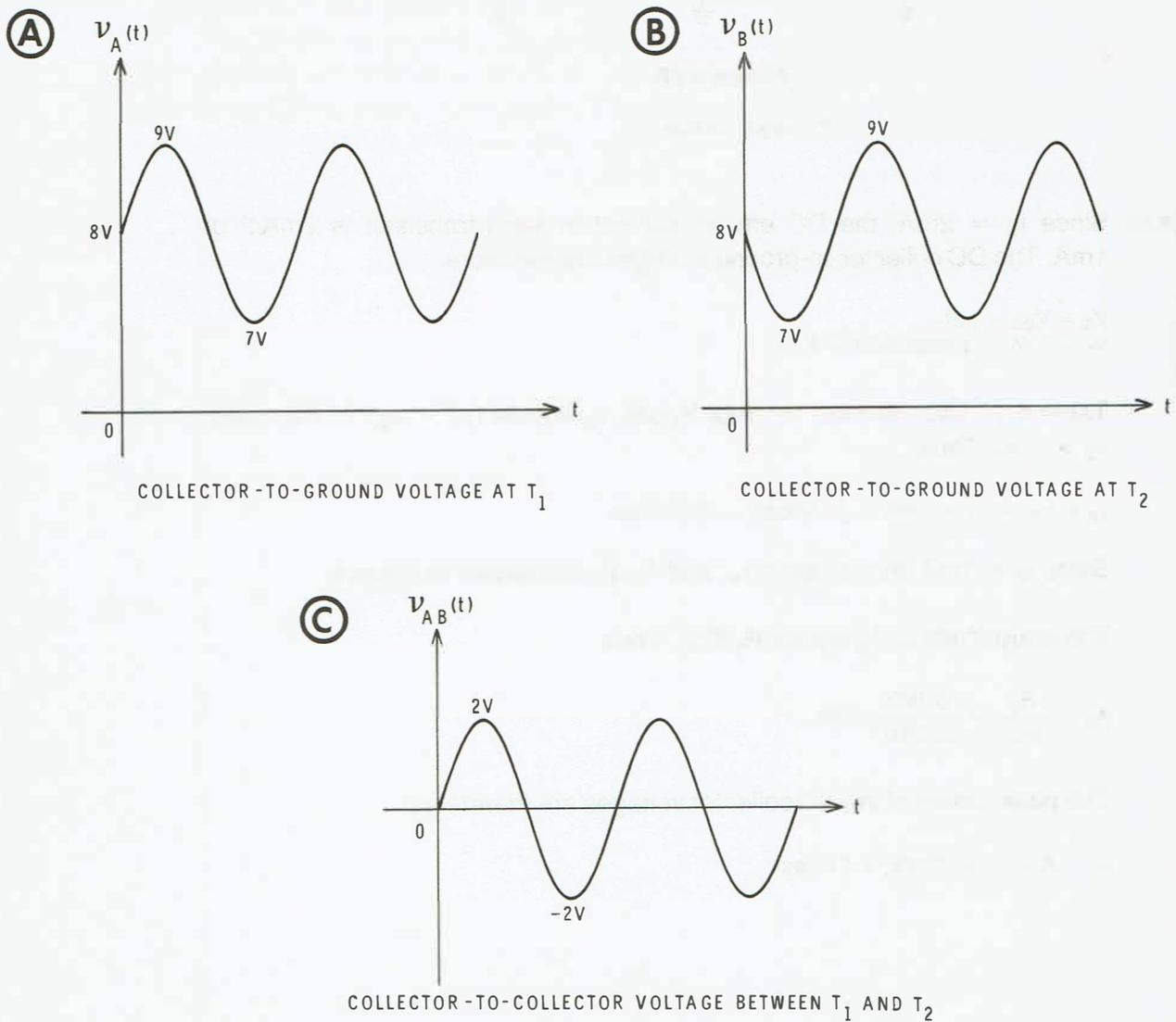


Figure 6-21

Waveforms for Example 6-11.

- A. Collector-to-ground voltage at T_1 .
 B. Collector-to-ground voltage at T_2 .
 C. Collector-to-collector voltage between T_1 and T_2 .

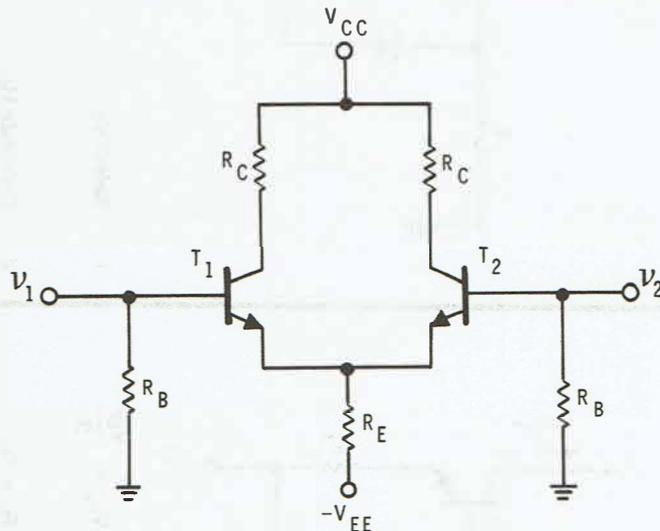
Designing Differential Amplifiers

The design guides that follow, outline the steps necessary to design basic BJT differential amplifiers. The first step is to select a suitable value of I_S . As a guide, choose I_S to be between 2mA and 6mA. The value of R_C is chosen so that V_{CQ} is approximately one-half of V_{CC} . This choice permits reasonable signal swings in the output voltages.

To obtain a large CMRR, it is necessary to utilize one of three BJT constant current sources discussed in this unit. The second design guide outlines the steps necessary to design a suitable constant current source.

A given discrete transistor rarely has characteristics that closely match another discrete transistor. For example, variations in V_{BE} of 0.1V between two transistors is quite common. Unfortunately, the differential amplifier sees any mismatch in V_{BE} as a differential voltage which it amplifies. Consequently, you should expect to find variations in the actual collector voltages and emitter currents in the two halves of the various BJT differential amplifier circuits.

DIFFERENTIAL AMPLIFIER DESIGN GUIDE



1. Select I_S .

2. Calculate R_C .

$$R_C = \frac{V_{CC}}{I_S}$$

3. Calculate R_E .

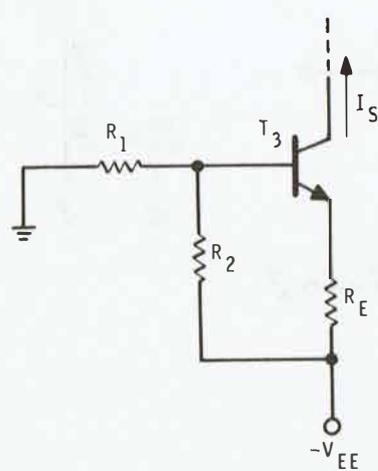
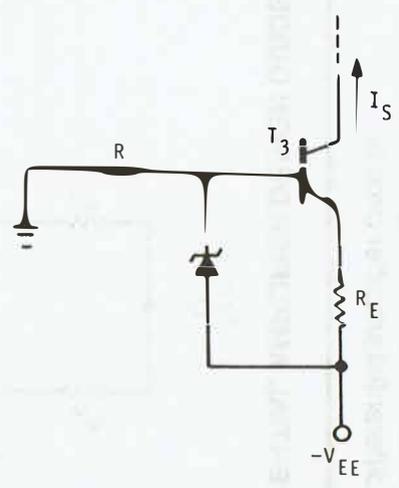
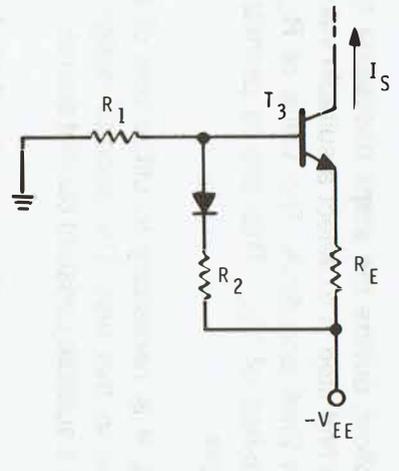
$$R_E = \frac{V_{EE} - V_{BE}}{I_S}$$

4. Select R_B .

$R_B = 1\text{k}\Omega$ to $10\text{k}\Omega$ is typical.

To obtain a large CMRR, use a BJT constant current source in place of R_E . In this case, step 3 is replaced by steps 1 through 3 in the constant current source design guide.

CONSTANT CURRENT SOURCE DESIGN GUIDE

1	2	3
		
<ol style="list-style-type: none"> 1. Calculate V_{R_2}. $V_{R_2} = \frac{V_{EE}}{2}$ 2. Select R_1 & R_2. $R_1 = R_2$ ($10k\Omega$ to $47k\Omega$ is typical.) 3. Calculate R_E. $R_E = \frac{V_{R_2} - V_{BE}}{I_S}$ 	<ol style="list-style-type: none"> 1. Select V_Z. $V_Z \approx 1/3$ to $1/2$ V_{EE} 2. Calculate R_E. $R_E = \frac{V_Z - V_{BE}}{I_S}$ 3. Calculate R. $R = \frac{V_{EE} - V_Z}{I_Z}$ 	<ol style="list-style-type: none"> 1. Calculate V_{R_2}. $V_{R_2} = \frac{V_{EE} - V_{BE}}{2}$ 2. Calculate R_E. $R_E = \frac{V_{R_2}}{I_S}$ 3. Select R_1 & R_2. $R_1 = R_2$ ($10k\Omega$ to $47k\Omega$ is typical.)

For those applications requiring “near ideal” differential amplifiers, you will find numerous integrated circuit, IC, units available from various manufacturers. Most of the problems you would encounter with discrete differential amplifiers are greatly minimized in the IC versions.

Example 6-12

Design a basic BJT differential amplifier assuming $I_S = 3\text{mA}$, $V_{CC} = 15\text{V}$, and $V_{EE} = -15\text{V}$.

Referring to the steps in the design guide:

1. $I_S = 3\text{mA}$
2. $R_C = \frac{V_{CC}}{I_S} = \frac{15\text{V}}{3\text{mA}} = 5\text{k}\Omega$
3. $R_E = \frac{V_{EE} - V_{BE}}{I_S} = \frac{15\text{V} - 0.7\text{V}}{3\text{mA}} = 4.76\text{k}\Omega$
4. Select $R_B = 1\text{k}\Omega$

Example 6-13

Redesign the amplifier in Example 6-12 to include a BJT constant current source that utilizes a zener diode. Assume a zener current of 2.5mA is adequate to keep the diode operating in the zener region.

1. Since $V_{EE} = -15\text{V}$ a 5.6V zener diode is a good choice.

$$2. R_E = \frac{V_Z - V_{BE}}{I_S} = \frac{5.6\text{V} - 0.7\text{V}}{3\text{mA}} = 1.63\text{k}\Omega$$

$$3. R = \frac{V_{EE} - V_Z}{I_Z} = \frac{15\text{V} - 5.6\text{V}}{2.5\text{mA}} = 3.76\text{k}\Omega$$

Self-Test Review

1. The differential amplifier is sometimes called a difference amplifier since it amplifies the _____ between the two input voltages.
2. In a well-designed differential amplifier, the differential-mode voltage gain is _____ and the common-mode voltage gain is _____.
3. For a differential output voltage, the effective differential voltage gain equals R_C divided by _____.
4. For a single-ended output voltage, the differential voltage gain equals R_C divided by _____.
5. The ratio of the differential- and common-mode voltage gain is called the _____.
6. $v_1 = 10\text{mV}$ peak, and $v_2 = 5\text{mV}$ peak. Assuming v_1 and v_2 are in phase with each other, the differential input voltage is _____mV peak.
7. The common-mode component of the input voltages in question 6 is _____mV peak.
8. If v_1 and v_2 in question 6 are 180° out of phase with each other, the differential input voltage equals _____mV peak.

Refer to Figure 6-22 for questions 9 through 14.

9. R_E should equal approximately, _____ $k\Omega$.
10. R_C should equal approximately, _____ $k\Omega$.
11. The peak value, of the AC component, of the voltage between point A and ground is _____ V.
12. The peak value of the voltage between points A and B is _____ V.
13. The circuit's common-mode rejection ratio is approximately, _____ dB.
14. The DC voltage between points A and B, ideally, equals _____ V.

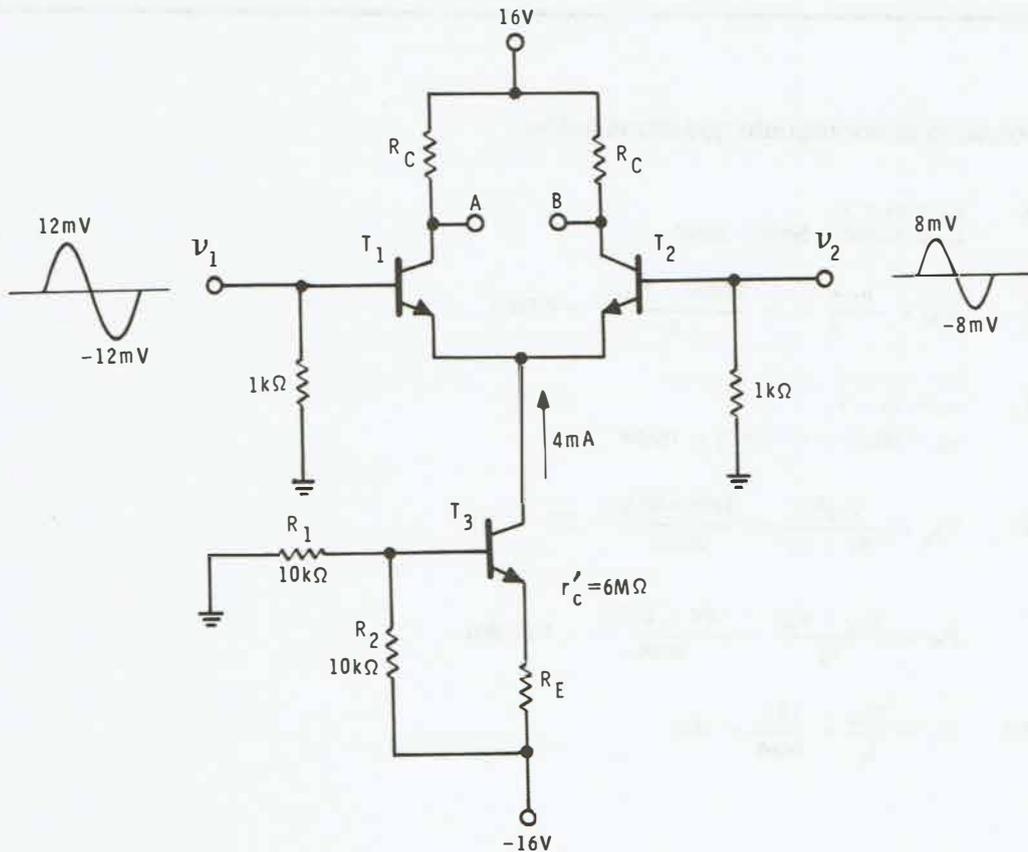


Figure 6-22

Circuit for Self-Test Review questions 9-14.

Answers

- | | |
|--------------------------------|--------------------|
| 1. difference | 8. 15mV |
| 2. large, small | 9. 1.825k Ω |
| 3. r_e' | 10. 4k Ω |
| 4. $2r_e'$ | 11. 0.432V |
| 5. common-mode rejection ratio | 12. 0.864V |
| 6. 5mV | 13. 110.2dB |
| 7. 7.5mV | 14. zero V |

Solutions to appropriate questions follow:

$$6. \quad \begin{aligned} v_d &= v_1 - v_2 \\ v_d &= 10\text{mV} - 5\text{mV} = 5\text{mV} \end{aligned}$$

$$7. \quad v_{\text{CM}} = \frac{v_1 + v_2}{2} = \frac{10\text{mV} + 5\text{mV}}{2} = 7.5\text{mV}$$

$$8. \quad \begin{aligned} v_d &= v_1 - v_2 \\ v_d &= 10\text{mV} - (-5\text{mV}) = 15\text{mV} \end{aligned}$$

$$9. \quad V_{R_2} = \frac{V_{EE}R_2}{R_1 + R_2} = \frac{16\text{V}(10\text{k}\Omega)}{20\text{k}\Omega} = 8\text{V}$$

$$R_E = \frac{V_{R_2} - V_{BE}}{I_S} = \frac{8\text{V} - 0.7\text{V}}{4\text{mA}} = 1.825\text{k}\Omega$$

$$10. \quad R_C = \frac{V_{CC}}{I_S} = \frac{16\text{V}}{4\text{mA}} = 4\text{k}\Omega$$

11. The differential voltage gain has a magnitude of $R_C/2r_{e'}$. Since $I_S = 4\text{mA}$, I_E equals 2mA . Thus:

$$r_{e'} = \frac{37\text{mV}}{I_E} = \frac{37\text{mV}}{2\text{mA}} = 18.5\Omega$$

$$A_d = \frac{R_C}{2r_{e'}} = \frac{4\text{k}\Omega}{2(18.5\Omega)} = 108$$

$$v_d = v_1 - v_2 = 12\text{mV} - 8\text{mV} = 4\text{mV peak}$$

The peak value of the AC component of **each** collector voltage is therefore:

$$v_C = A_d v_d = 108(4\text{mV}) = 0.432\text{V peak}$$

Naturally, v_{C_1} and v_{C_2} are 180° out of phase with each other.

12. $v_{C_1} = v_{C_2} = 0.432\text{V}$. However, v_{C_1} and v_{C_2} are 180° out of phase with each other. Thus:

$$v_{C_1} - v_{C_2} = 0.432\text{V} - (-0.432\text{V}) = 0.864\text{V}. \text{ Note that, by taking the output between the collectors, the effective voltage gain is doubled.}$$

13. $\text{CMRR} = A_d/A_{\text{CM}}$

Since a BJT constant source is employed, the magnitude of A_{CM} equals $R_C/2r_{c'}$. Thus:

$$A_{\text{CM}} = \frac{R_C}{2r_{c'}} = \frac{4\text{k}\Omega}{2(6\text{M}\Omega)} = 3.33 \times 10^{-4}$$

Since the magnitude of A_d is 108:

$$\text{CMRR} = \frac{A_d}{A_{\text{CM}}} = \frac{108}{3.33 \times 10^{-4}} = 324,000$$

In decibel notation:

$$\text{CMRR}_{\text{dB}} = 20 \log \text{CMRR}$$

$$\text{CMRR}_{\text{dB}} = 20 \log 324,000 = 110.2\text{dB}$$

14. Ideally, $V_{C_1} = V_{C_2}$. Thus the DC voltage between the two collectors ideally, equals zero.

MULTISTAGE AMPLIFIERS

When the requirements for a particular application cannot be satisfied by a single stage of amplification, several stages can be cascaded together to form a multistage amplifier. In this section, we will discuss the analysis and design of selected multistage RC-coupled amplifiers.

Analysis By Blocks

Before attempting to analyze an actual multistage amplifier, let's consider the general block diagram shown in Figure 6-23. Here, a number of single stage amplifiers have been cascaded together to form the multistage amplifier enclosed by the dashed lines.

From your study of single stage amplifiers, you know that the voltage gain of a given stage depends upon the value of load resistance, R_L , connected across the output terminals of the amplifier. In Figure 6-23 it is important to note that:

The effective load resistance of each stage, except the last stage, is the input resistance of the following stage.

Thus, in Figure 6-23, the effective load resistance of the first stage is R_{IN_2} . Similarly, the effective load resistance of the second stage is R_{IN_3} , and so forth. For this reason, when you analyze a multistage amplifier, you should begin with the last stage and work backwards until you reach the first stage. Naturally, the load resistance of the last stage is the resistance of the actual load device.

Obviously, the overall characteristics of a multistage amplifier depend upon the characteristics of the individual stages. Referring to Figure 6-23, let's examine how the characteristics of the individual stages effect the input resistance, output resistance, and various gains of the multistage amplifier.

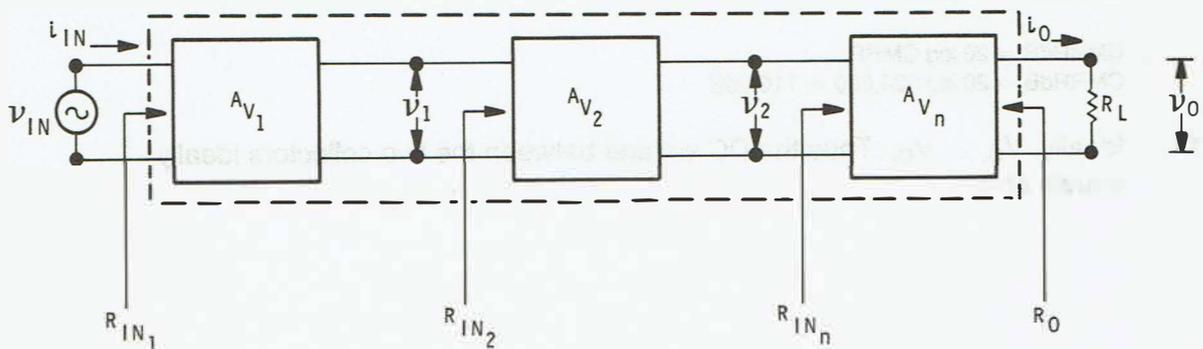


Figure 6-23

Block diagram of n cascaded amplifier stages.

INPUT AND OUTPUT RESISTANCE

The input resistance seen by the signal source is, by inspection, the input resistance of the first amplifier stage. Similarly, the output resistance seen by the actual load device is the output resistance of the last amplifier stage. Thus:

$$R_{IN} = R_{IN_1} \quad (\text{Eq. 6-24})$$

$$R_O = R_{O_n} \quad (\text{Eq. 6-25})$$

VOLTAGE GAIN

The total voltage gain of n cascaded stages equals the product of the individual stage gains. Thus:

$$A_{V_T} = A_{V_1} \cdot A_{V_2} \cdots A_{V_n} \quad (\text{Eq. 6-26})$$

Naturally, if the individual stage gains are given in decibels, the total dB gain of the system equals the sum of the individual stage gains.

CURRENT GAIN

As was the case with voltage gain, the total current gain equals the product of the individual stage gains. Thus:

$$A_{i_T} = A_{i_1} \cdot A_{i_2} \cdots A_{i_n} \quad (\text{Eq. 6-27})$$

A more useful expression for the total current gain is obtained as follows:

$$A_{V_T} = \frac{v_O}{v_{IN}} = \frac{i_O R_L}{i_{IN} R_{IN}}$$

Since the ratio $\frac{i_O}{i_{IN}}$ is the total current gain of the multistage amplifier, we have:

$$A_{V_T} = \frac{A_{i_T} R_L}{R_{IN_1}}$$

Solving for A_{i_T} yields:

$$A_{i_T} = \frac{A_{V_T} R_{IN_1}}{R_L} \quad (\text{Eq. 6-28})$$

POWER GAIN

Once again, the total gain equals the product of the individual stage gains:

$$A_{P_T} = A_{P_1} \cdot A_{P_2} \dots A_{P_n} \quad (\text{Eq. 6-29})$$

As was the case with current gain, it is desirable to express the power gain in terms of the voltage gain. Thus:

$$A_{P_T} = \frac{(v_O)^2/R_L}{(v_{IN})^2/R_{IN}}$$

Substituting A_{V_T} for v_O/v_{IN} , we have:

$$A_{P_T} = \frac{(A_{V_T})^2 R_{IN}}{R_L} \quad (\text{Eq. 6-30})$$

Example 6-14

For the multistage amplifier in Figure 6-24, determine:

- The voltage, current, and power gains.
- The input and output resistance.
- The power supplied to R_L , assuming $v_{IN} = 10\text{mV rms}$.

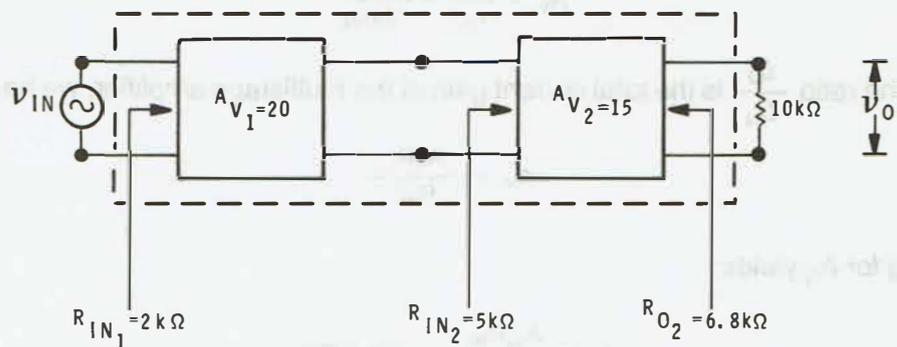


Figure 6-24

Circuit for Example 6-14.

(a) $A_{V_T} = A_{V_1}A_{V_2} = 20(15) = 300$

$$A_{i_T} = \frac{A_{V_T}R_{IN}}{R_L} = \frac{300(2k\Omega)}{10k\Omega} = 60$$

$$A_{P_T} = \frac{(A_{V_T})^2R_{IN}}{R_L} = \frac{(300)^2(2k\Omega)}{10k\Omega} = 18,000$$

Note that the product of the voltage and current gains equal the power gain. If you prefer, you can calculate the power gain as follows:

$$A_{P_T} = A_{V_T}A_{i_T} = 300(60) = 18,000$$

(b) $R_{IN} = R_{IN_1} = 2k\Omega$

$$R_O = R_{O_2} = 6.8k\Omega$$

(c) Since A_{P_T} equals 18,000, the AC power supplied to the $10k\Omega$ load will be 18,000 times greater than the AC input power. Thus:

$$P_{IN} = \frac{(v_{IN})^2}{R_{IN}} = \frac{(10mV)^2}{2k\Omega} = .05\mu W$$

$$P_O = A_{P_T}P_{IN} = 18,000(.05\mu W) = .9mW$$

Two-Stage Voltage Amplifiers

The simplest multistage amplifiers consist of two stages of amplification. Since the common-emitter configuration provides relatively large voltage, current, and power gains, it is often the preferred configuration for two-stage voltage amplifiers.



A typical two-stage, RC coupled, voltage amplifier is illustrated in Figure 6-25. Note that the input resistance of the second stage, R_{IN_2} , is the effective load resistance of the first stage. This point is emphasized by the equivalent circuit in Figure 6-25B.

You analyze a two-stage amplifier by combining the results of the "block analysis" and the methods used to analyze single stage circuits. The following example illustrates this process.

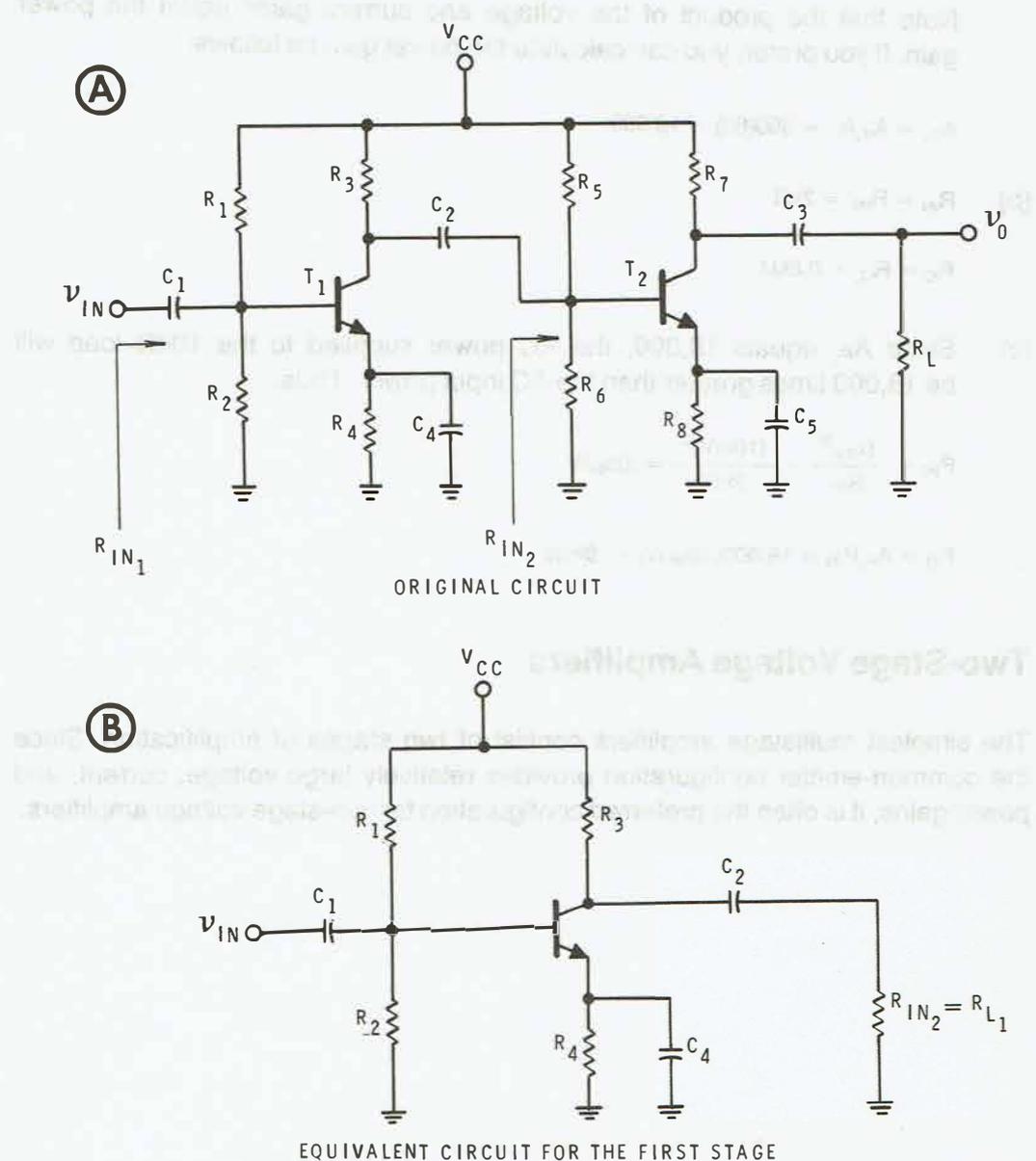


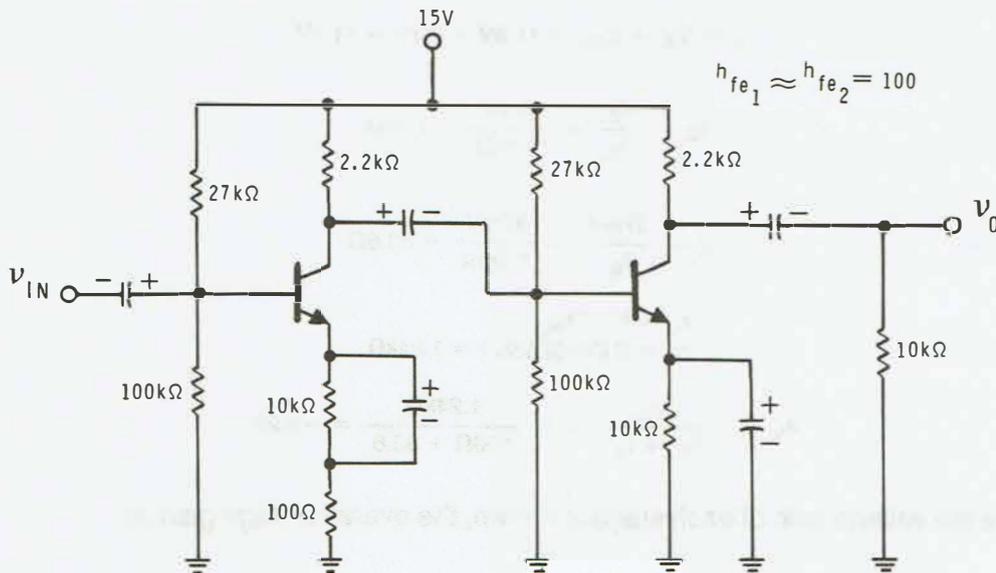
Figure 6-25

A multistage amplifier, composed of two common-emitter stages.

- A. Original circuit.
- B. Equivalent circuit for the first stage.

Example 6-15

For the circuit shown in Figure 6-26, calculate the voltage gain, current gain, power gain, input resistance, and output resistance.

**Figure 6-26**

Circuit for Example 6-15.

You begin by analyzing the last stage. Thus:

$$V_{B_2} = \frac{15V(100k\Omega)}{27k\Omega + 100k\Omega} = 11.8V$$

$$V_{E_2} = V_{B_2} - V_{BE_2} = 11.8V - 0.7V = 11.1V$$

$$I_{E_2} = \frac{V_{E_2}}{R_{E_2}} = \frac{11.1V}{10k\Omega} = 1.11mA$$

$$r_{e_2}' = \frac{37mV}{I_{E_2}} = \frac{37mV}{1.11mA} = 33.3\Omega$$

$$r_{L_2} = 2.2k\Omega \parallel 10k\Omega = 1.8k\Omega$$

$$A_{v_2} = - \frac{r_{L_2}}{r_{e_2}'} = - \frac{1.8k\Omega}{33.3\Omega} = -54.05$$

$$R_{IN(BASE\ 2)} = h_{fe_2}(r_{e_2}') \\ R_{IN(BASE\ 2)} = 100(33.3\Omega) = 3.3k\Omega$$

$$R_{IN_2} = 27k\Omega \parallel 100k\Omega \parallel 3.3k\Omega \\ R_{IN_2} = 21.2k\Omega \parallel 3.3k\Omega = 2.85k\Omega$$

Since R_{IN_2} is the effective load resistance of the first stage, $R_{L_1} = 2.85\text{k}\Omega$. Thus, the analysis of the first stage proceeds as follows:

$$V_{B_1} = \frac{15\text{V}(100\text{k}\Omega)}{27\text{k}\Omega + 100\text{k}\Omega} = 11.8\text{V}$$

$$V_{E_1} = V_{B_1} - V_{BE_1} = 11.8\text{V} - 0.7\text{V} = 11.1\text{V}$$

$$I_{E_1} = \frac{V_{E_1}}{R_{E_1}} = \frac{11.1\text{V}}{10.1\text{k}\Omega} = 1.1\text{mA}$$

$$r_{e_1}' = \frac{37\text{mV}}{I_{E_1}} = \frac{37\text{mV}}{1.1\text{mA}} = 33.6\Omega$$

$$r_{L_1} = R_C \parallel R_{IN_2}$$

$$r_{L_1} = 2.2\text{k}\Omega \parallel 2.85\text{k}\Omega = 1.24\text{k}\Omega$$

$$A_{V_1} = \frac{-r_{L_1}}{R_{E_1} + r_{e_1}'} = -\frac{1.24\text{k}\Omega}{100\Omega + 33.6} = -9.28$$

Since the voltage gain of each stage is known, the overall voltage gain is:

$$A_{V_T} = A_{V_1} A_{V_2}$$

$$A_{V_T} = (-9.28)(-54.05) = 501.6$$

Since each common emitter stage provides a 180° phase shift, the input and output voltages are in phase with each other. Consequently, the sign preceding A_{V_T} is positive.

The input resistance of the amplifier is the input resistance of the first stage. Thus:

$$R_{IN(\text{BASE } 1)} = h_{ie_1}(R_{E_1} + r_{e_1}')$$

$$R_{IN(\text{BASE } 1)} = 100(100\Omega + 33.6\Omega) = 13.36\text{k}\Omega$$

$$R_{IN_1} = 27\text{k}\Omega \parallel 100\text{k}\Omega \parallel 13.36\text{k}\Omega$$

$$R_{IN_1} = 21.2\text{k}\Omega \parallel 13.36\text{k}\Omega = 8.19\text{k}\Omega$$

The output resistance of a common-emitter amplifier is approximately equal to the collector resistance, R_C . Thus:

$$R_O \approx R_{C_2} = 2.2\text{k}\Omega$$

Since R_{IN} , R_L , and A_{V_T} are known, the current and power gains can be obtained as follows:

$$A_{i_T} = \frac{A_{V_T} R_{IN_1}}{R_L} = \frac{501.6(8.19\text{k}\Omega)}{10\text{k}\Omega} = 410.8$$

$$A_{P_T} = \frac{(A_{V_T})^2 R_{IN_1}}{R_L} = \frac{(501.6)^2(8.19\text{k}\Omega)}{10\text{k}\Omega} = 206,062$$

Example 6-16

Estimate the clipping levels for the second stage in Figure 6-26. Based upon these estimates, what is the largest value of v_{IN} that produces an unclipped output voltage?

Recall from Unit 3 that the clipping levels of a common-emitter amplifier are approximated by:

$$V^+ = I_{CQ}(R_{E_1} + r_L)$$

$$V^- = V_{CEQ}$$

Thus:

$$V^+ = 1.11\text{mA}(0 + 1.8\text{k}\Omega) = 2\text{V peak}$$

$$V_{C_2} = V_{CC} - I_{C_2} R_{C_2}$$

$$V_{C_2} = 15\text{V} - 1.11\text{mA}(2.2\text{k}\Omega) = 12.56\text{V}$$

Since $V_{E_2} = 11.1\text{V}$

$$V^- = V_{CEQ} = 12.56\text{V} - 11.1\text{V} = 1.46\text{V peak}$$

Thus, the maximum possible unclipped output voltage from the amplifier is approximately 1.46V peak.

Since the total voltage gain, A_{V_T} , is approximately 501.6, the value of v_{IN} that produces a 4V peak output voltage is:

$$v_{IN(\text{MAX})} = \frac{v_{O(\text{MAX})}}{A_{V_T}}$$

$$v_{IN(\text{MAX})} = \frac{1.46\text{V}}{501.6} = 2.91\text{mV peak}$$

Noise

The largest input voltage that produces an unclipped output voltage, in Figure 6-26, was estimated to be 2.91 mV peak. Obviously, this is a small input signal.

Since the amplifier in Figure 6-26 is single ended, any noise present at the input will be amplified along with the signal voltages. Thus, if the noise voltage is in the mV range, or larger, the output voltage in Figure 6-26 will be distorted.

For these reasons, induced noise voltages are especially bothersome in amplifiers that have large voltage gains. Some of the steps you can take to minimize the amplification of noise voltage include:

1. Keep the lead lengths of components as short as possible.
2. Connect components that go to ground to a single point.
3. Use coaxial cable for the input and output leads.
4. Enclose the entire circuit in a metal box. This helps to shield the circuit from potential noise sources.

If the previous steps do not solve the problem, you should consider employing differential stages before the single-ended voltage amplifier. For example, by cascading a differential-input, differential-output stage with a differential-input, single-output stage, you obtain a single-ended output voltage that contains very little noise.

Design Considerations

Clearly, it is not possible to provide a concise series of design steps that apply equally well to virtually any set of specifications. Above a certain order of complexity, the persistence, experience, and creativity of the circuit designer become major components of the actual design process.

Nevertheless, by employing the various design guides, in conjunction with the block approach, it is possible to design numerous useful multistage amplifiers. To illustrate some of the steps in an elementary multistage design problem, let's assume we are to design a voltage amplifier according to the following specifications:

1. $V_{CC} = 15V$
2. $R_L = 10k\Omega$
3. A_v should have a typical value of approximately 500.

To begin, the relatively large voltage gain suggests two stages of amplification. As mentioned previously, common-emitter stages are a reasonable choice for multistage amplifiers. Therefore, the common-emitter configuration will be used for each stage.

The design of a multistage amplifier may be reduced to the design of two or more compatible stages. Since a total voltage gain of 500 is desired, the product of the individual stage gains should equal 500. Somewhat arbitrarily then, we select $A_{v_1} = 10$ and $A_{v_2} = 50$, as shown in Figure 6-27.

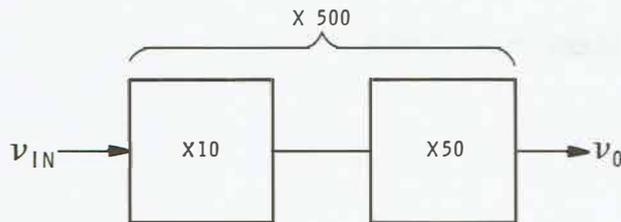


Figure 6-27

Block diagram for the design problem discussed in the text.

Due to its inherent stability, voltage divider bias will be used for both stages. Thus, referring to the common-emitter, voltage divider design guide in Unit 3, you proceed as follows:

2ND STAGE

1. $I_{CQ} = 1\text{mA}$
2. $r_e' = 37\text{mV}/1\text{mA} = 37\Omega$
3. $R_{E_1} = 0$
4. $r_L = A_V(r_e' + R_{E_1}) = 50(37\Omega) = 1.85\text{k}\Omega$
5. $R_C = \frac{R_L r_L}{R_L - r_L} = \frac{10\text{k}\Omega(1.85\text{k}\Omega)}{10\text{k}\Omega - 1.85\text{k}\Omega} = 2.27\text{k}\Omega$
6. $V_{CEQ} = I_{CQ}(R_{E_1} + r_L) = 1\text{mA}(0 + 1.85\text{k}\Omega) = 1.85\text{V}$
7. $V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CEQ}]$
 $V_{EQ} = 15\text{V} - [1\text{mA}(2.27\text{k}\Omega) + 1.85\text{V}] = 10.88\text{V}$
8. $R_E = V_{EQ}/I_{CQ} = 10.88\text{V}/1\text{mA} = 10.88\text{k}\Omega$
9. $R_{E_2} = 10.88\text{k}\Omega$
10. $R_2 = 100\text{k}\Omega$
11. $R_1 = \frac{R_2(V_{CC} - V_{BQ})}{V_{BQ}} = \frac{100\text{k}\Omega(15\text{V} - 11.58\text{V})}{11.58\text{V}} = 29.5\text{k}\Omega$
12. $R_{IN(\text{BASE})} = h_{fe}(R_{E_1} + r_e')$
 $R_{IN(\text{BASE})} = 100(0 + 37\Omega) = 3.7\text{k}\Omega$
 $R_{IN} = 29.5\text{k}\Omega \parallel 100\text{k}\Omega \parallel 3.7\text{k}\Omega$
 $R_{IN} = 22.8\text{k}\Omega \parallel 3.7\text{k}\Omega = 3.18\text{k}\Omega$

The minimum capacitor values are:

$$C_1 = \frac{3.18}{f_1 R_{IN}} = \frac{3.18}{500(3.18\text{k}\Omega)} = 2\mu\text{F}$$

$$C_2 = \frac{3.18}{f_1 R_L} = \frac{3.18}{500(10\text{k}\Omega)} = 0.636\mu\text{F}$$

$$C_3 = \frac{3.18}{f_1 R_{E_2}} = \frac{3.18}{500(10.88\text{k}\Omega)} = 0.585\mu\text{F}$$

In order to provide a reasonable input resistance for the first stage, we opt for a partially bypassed emitter resistor. Thus:

1ST STAGE

1. $I_{CQ} = 1\text{mA}$
2. $r_e' = 37\text{mV}/1\text{mA} = 37\Omega$
3. Initially, you might select $R_{E_1} = 5r_e' = 185\Omega$. In this case, however, you will find in step 7 that such a choice requires a larger supply voltage than 15V. For this reason, we choose $R_{E_1} = 100\Omega$.
4. $r_L = A_V(r_e' + R_{E_1}) = 10(37\Omega + 100\Omega) = 1.37\text{k}\Omega$
5. $R_C = \frac{R_L r_L}{R_L - r_L} = \frac{3.18\text{k}\Omega(1.37\text{k}\Omega)}{3.18\text{k}\Omega - 1.37\text{k}\Omega} = 2.4\text{k}\Omega$
6. $V_{CEQ} = I_{CQ}(R_{E_1} + r_L) = 1\text{mA}(100\Omega + 1.37\text{k}\Omega) = 1.47\text{V}$
7. $V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CEQ}]$
 $V_{EQ} = 15\text{V} - [1\text{mA}(2.4\text{k}\Omega + 1.47\text{V})] = 11.13\text{V}$
8. $R_E = V_{EQ}/I_{CQ} = 11.13\text{V}/1\text{mA} = 11.13\text{k}\Omega$
9. $R_{E_2} = R_E - R_{E_1} = 11.13\text{k}\Omega - 100\Omega = 11.03\text{k}\Omega$
10. Select $R_2 = 100\text{k}\Omega$
11. $R_1 = \frac{R_2(V_{CC} - V_{BQ})}{V_{BQ}} = \frac{100\text{k}\Omega(15\text{V} - 11.83\text{V})}{11.83\text{V}} = 26.8\text{k}\Omega$
12. $R_{IN(\text{BASE})} = h_{ie}(R_{E_1} + r_e') = 100(100\Omega + 37\Omega) = 13.7\text{k}\Omega$
 $R_{IN} = 26.8\text{k}\Omega \parallel 100\text{k}\Omega \parallel 13.7\text{k}\Omega$
 $R_{IN} = 21.1\text{k}\Omega \parallel 13.7\text{k}\Omega = 8.31\text{k}\Omega$

The minimum capacitor values are:

$$C_1 = \frac{3.18}{f_1 R_{IN}} = \frac{3.18}{500(8.31\text{k}\Omega)} = 0.765\mu\text{F}$$

C_2 for the first stage is C_1 of the second stage, or $2.13\mu\text{F}$

$$C_3 = \frac{3.18}{f_1 R_{E_2}} = \frac{3.18}{500(11.03\text{k}\Omega)} = 0.576\mu\text{F}$$

Employing standard value components, you obtain the circuit shown in Figure 6-26.

Negative Feedback

The term **feedback** refers to the process of obtaining a portion of a system's output, and literally feeding back the sampled signal to the system's input. In a negative feedback system, the **difference** between the input and feedback signals are amplified by the feedback amplifier.

In a system composed of amplifier blocks, both voltage and current can be fed back to the input. In addition, the feedback signal can be connected in either series or parallel with the signal source. For these reasons, there are four fundamental feedback configurations.

VOLTAGE-SERIES NEGATIVE FEEDBACK

Figure 6-28A illustrates a non-inverting amplifier block. Typically, this block would consist of two cascaded common-emitter stages. The voltage gain of the basic amplifier block is referred to as the **open loop gain**, A_{OL} . Thus, in Figure 6-28A:

$$A_{OL} = \frac{v_O}{v_{IN}} \quad (\text{Eq. 6-31})$$

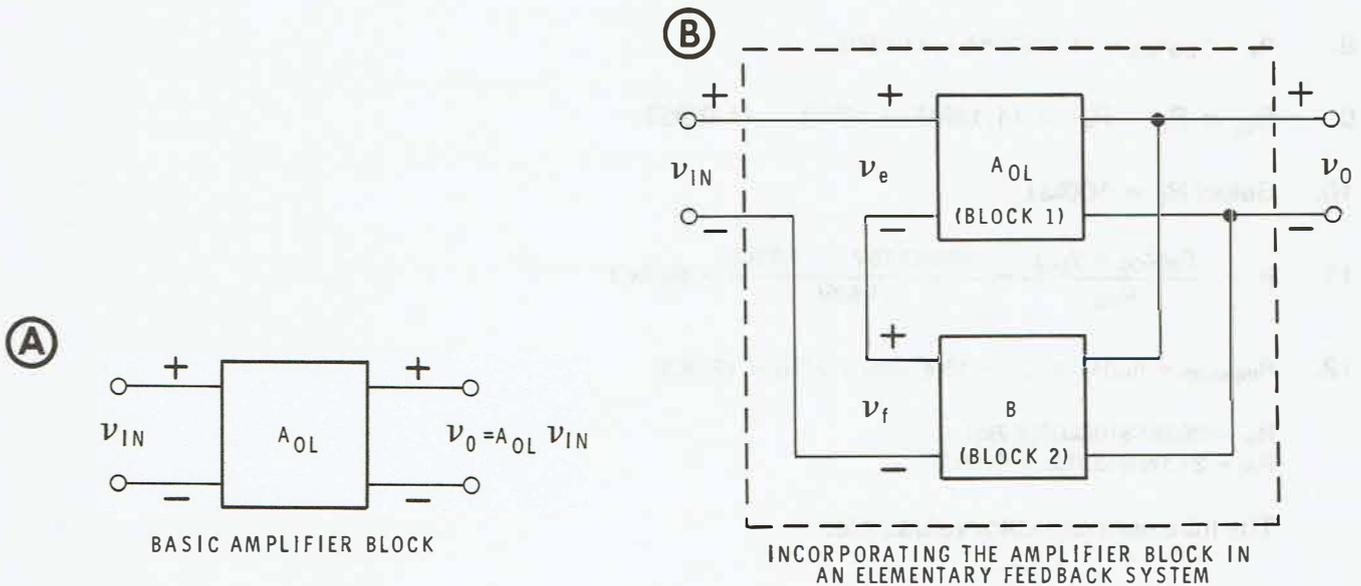


Figure 6-28

Constructing a voltage-series, negative feedback amplifier.

- A. Basic amplifier block.
- B. Incorporating the amplifier block in an elementary feedback system.

The system illustrated in Figure 6-28B is an example of a **voltage - series negative feedback** system. Here, the voltage gain of the system enclosed by the dotted lines is referred to as the **closed loop gain**, A_{CL} . Therefore, in Figure 6-28B:

$$A_{CL} = \frac{v_O}{v_{IN}} \quad (\text{Eq. 6-32})$$

In Figure 6-28B, note that the feedback amplifier basically consists of two parts. These are:

1. Block number 1, which represents the noninverting amplifier shown in Figure 6-28A.
2. Block number 2, which represents the **feedback network**. The purpose of the feedback network is to sample the output voltage in order to produce the desired feedback signal, v_f . The actual network in block number 2 is often nothing more than a simple voltage divider. Since the input to the feedback network is v_O , the voltage gain, B' , of the feedback network is:

$$B' = \frac{v_f}{v_O} \quad (\text{Eq. 6-33})$$

Typically, the value of B' is less than unity since it is only a sample of the output.

Referring to Figure 6-28B, you can obtain an expression for the system's closed loop voltage gain as follows:

Looking at block number 1 we note: v_e is the effective input voltage with feedback.

$$v_O = A_{OL}v_e$$

Writing a loop equation at the input to block number 1 yields:

$$v_e = v_{IN} - v_f$$

Since $v_f = B'v_O$:

$$v_e = v_{IN} - B'v_O$$

Substituting $(v_{IN} - B'v_O)$ for v_e in the expression $v_O = A_{OL}v_e$, we obtain:

$$\begin{aligned} v_O &= A_{OL}(v_{IN} - B'v_O) \\ v_O &= A_{OL}v_{IN} - A_{OL}B'v_O \\ v_O + A_{OL}B'v_O &= A_{OL}v_{IN} \\ v_O(1 + A_{OL}B') &= A_{OL}v_{IN} \end{aligned}$$

Finally, since the ratio of v_O to v_{IN} is the closed loop voltage gain, we have:

$$A_{CL} = \frac{v_O}{v_{IN}} = \frac{A_{OL}}{1 + A_{OL}B'} \quad (\text{Eq. 6-34})$$

Incidentally, the term $A_{OL}B'$ appearing in the denominator of Equation 6-34 is called the **loop gain**.

You can appreciate the significance of Equation 6-34 by considering how the gain of the feedback amplifier is affected by changes in the gain of the noninverting amplifier block.

Example 6-17

A noninverting amplifier has an open loop voltage gain of 1000. This amplifier is employed as one block of a voltage-series feedback amplifier as shown in Figure 6-29. Here, note that the details of the feedback network contained in block 2 are provided.

- (a) Calculate the gain of the feedback network.
- (b) Calculate the voltage gain of the feedback amplifier.
- (c) Due to temperature changes, component aging, etc., the voltage gain of the noninverting amplifier increases from 1000 to 2000. What is the new value for the voltage gain of the feedback amplifier?

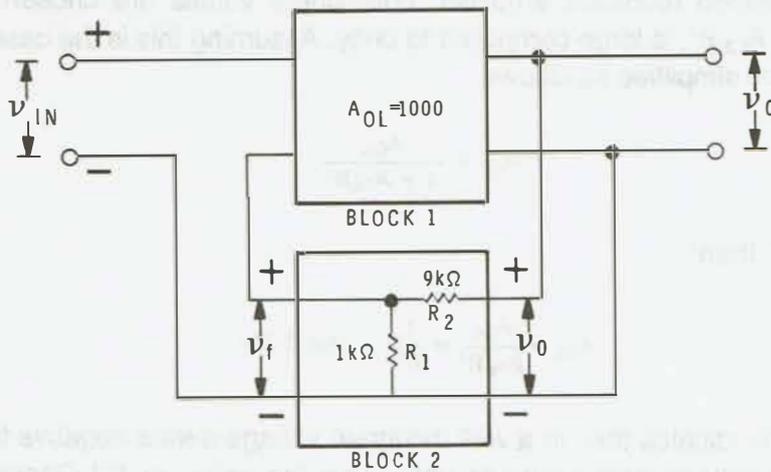


Figure 6-29

Circuit for Example 6-17.

- (a) In Figure 6-29, v_f as determined using voltage division, is:

$$v_f = v_O \left(\frac{R_1}{R_1 + R_2} \right)$$

Thus:

$$B' = \frac{v_f}{v_O} = \frac{R_1}{R_1 + R_2} = \frac{1\text{ k}\Omega}{1\text{ k}\Omega + 9\text{ k}\Omega} = 0.1$$

- (b) Since the gain of the noninverting amplifier and feedback network are known, you can calculate the gain of the feedback amplifier as follows:

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}B'} = \frac{1000}{1 + 1000(0.1)} = 9.9$$

- (c) In this case, $A_{OL} = 2000$. Thus:

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}B'} = \frac{2000}{1 + 2000(0.1)} = 9.95$$

Note that a 100% change in the gain of the amplifier block produces very little change in the gain of the feedback amplifier.

In a well designed feedback amplifier, component values are chosen so that the loop gain, $A_{OL}B'$, is large compared to unity. Assuming this is the case, Equation 6-34 can be simplified as follows:

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}B'}$$

If $A_{OL}B' \gg 1$, then:

$$A_{CL} \approx \frac{A_{OL}}{A_{OL}B'} = \frac{1}{B'} \quad (\text{Eq. 6-35})$$

Equation 6-35 indicates that, in a well designed voltage-series negative feedback amplifier, the voltage gain depends only upon the value of B' ! Consequently, variations in the gain of the noninverting amplifier block have little effect on the actual voltage gain of the feedback amplifier.

By employing a voltage divider that utilizes precision resistors, the value of B' is fixed. Since $A_{CL} \approx 1/B'$, the resulting closed loop gain is largely independent of both individual unit and unit-to-unit parameter variations.

Input and Output Resistances

The introduction of voltage-series feedback to an amplifier produces a higher input resistance and a lower output resistance. An analysis of the feedback system indicates that the change in resistance-levels equals $(1 + A_{OL}B')$. Specifically:

$$R_{IN}' = R_{IN}(1 + A_{OL}B') \quad (\text{Eq. 6-36})$$

$$R_{O}' = \frac{R_O}{1 + A_{OL}B'} \quad (\text{Eq. 6-37})$$

Where: R_{IN} and R_O are the input resistance and output resistance of the noninverting amplifier.

R_{IN}' and R_{O}' are the input resistance and output resistance of the feedback amplifier.

Example 6-18

The noninverting amplifier in Figure 6-29 has an input resistance of $2\text{k}\Omega$ and output resistance of $5\text{k}\Omega$. Calculate the input resistance and output resistance of the feedback amplifier.

Since $A_{OL} = 1000$ and $B' = 0.1$:

$$1 + A_{OL}B' = 1 + 1000(0.1) = 101$$

Thus:

$$\begin{aligned} R_{IN}' &= R_{IN}(1 + A_{OL}B') \\ R_{IN}' &= 2\text{k}\Omega(101) = 202\text{k}\Omega \end{aligned}$$

$$R_O = \frac{R_O}{1 + A_{OL}B'} = \frac{5\text{k}\Omega}{101} = 49.5\Omega$$

Distortion

Nonlinear distortion is evident in an amplifier when the changes in collector current and collector-to-emitter voltage are large. As the instantaneous operating point approaches the saturation and cutoff regions, the current gain of the transistor decreases. A large decrease in the transistor's current gain produces a corresponding decrease in the voltage gain of the amplifier. This results in nonlinear distortion.

With sufficient negative feedback, the closed loop gain of the feedback amplifier is largely immune to variations in the open loop gain of the noninverting amplifier. Hence, the nonlinear distortion is greatly reduced. As was the case with resistance-levels, the factor by which the distortion is changed, ideally, equals $(1 + A_{OL}B')$. Thus:

$$D' = \frac{D}{1 + A_{OL}B'} \quad (\text{Eq. 6-38})$$

Where: D = amount of nonlinear distortion without negative feedback.
 D' = amount of nonlinear distortion with negative feedback.

For example, if 10% nonlinear distortion is present without feedback and $(1 + A_{OL}B') = 99$, the nonlinear distortion with negative feedback is only 1%.

Practical Voltage-Series, Negative Feedback Amplifier

An example of a popular voltage-series, negative feedback circuit is provided in Figure 6-30. Here, the common-emitter stages composed of T_1 and T_2 provide a reasonably large open loop voltage gain. As you can see, the feedback network consists of the voltage divider formed by R_1 and R_2 .

In Figure 6-30, note that the feedback voltage, v_f , is fed back from the output of the second stage to the emitter of the first stage. For this reason, the AC base-to-emitter voltage of T_1 equals the difference between v_{IN} and v_f .

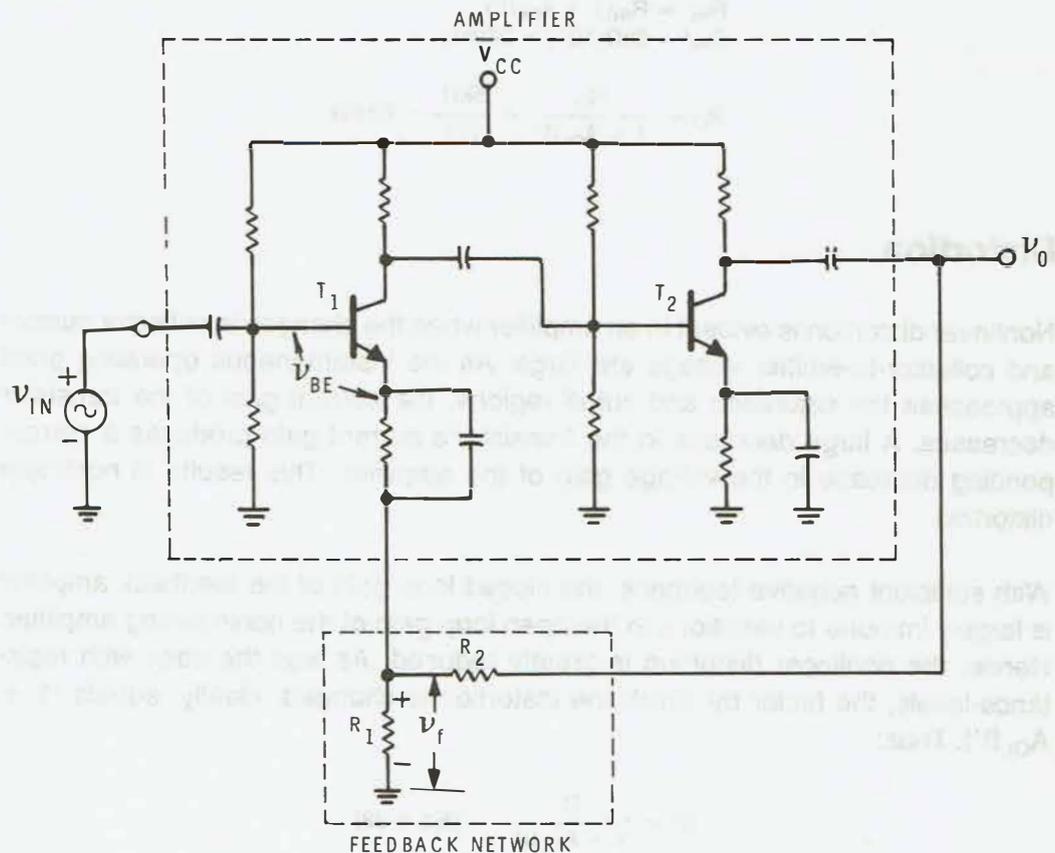


Figure 6-30

A practical voltage-series negative feedback amplifier.

In example 6-17, the voltage gain of the voltage divider feedback network was shown to be:

$$B' = \frac{R_1}{R_1 + R_2}$$

If the loop gain, $A_{OL}B'$, is large compared to unity, the closed loop gain approximately equals $1/B'$. Assuming this is the case:

$$A_{CL} \approx \frac{1}{B'} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1} \quad (\text{Eq. 6-39})$$

Example 6-19

The amplifier in Figure 6-30 has an open loop gain of 1000. In addition, $R_1 = 150\Omega$ and $R_2 = 4.5k\Omega$. What is the value of the closed loop gain predicted by Equation 6-34? Equation 6-39?

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}B'} \quad (\text{Eq. 6-34})$$

$$B' = \frac{R_1}{R_1 + R_2} = \frac{150\Omega}{150\Omega + 4.5k\Omega} = 0.0322$$

Thus:

$$A_{CL} = \frac{1000}{1 + 32.2} = 30.12$$

$$A_{CL} = 1 + \frac{R_2}{R_1} \quad (\text{Eq. 6-39})$$

$$A_{CL} = 1 + \frac{4.5k\Omega}{150\Omega} = 31$$

Self-Test Review

Refer to Figure 6-31 for questions 15 through 19.

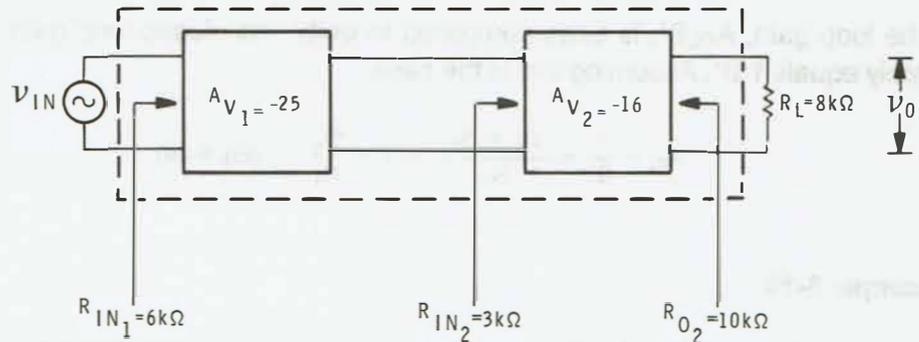


Figure 6-31

Circuit for Self-Test Review questions 15-19.

15. The total voltage gain is _____ dB.
16. The total current gain is _____.
17. The total power gain is _____.
18. Assuming both stages are common-emitter amplifiers, v_O and v_{IN} will be _____ degrees out of phase with each other.
19. The effective load resistance of the first stage is approximately _____ $\text{k}\Omega$.

Refer to Figure 6-32 for questions 20 through 24. Assume the loop gain, $A_{OL}B'$, is large compared to unity.

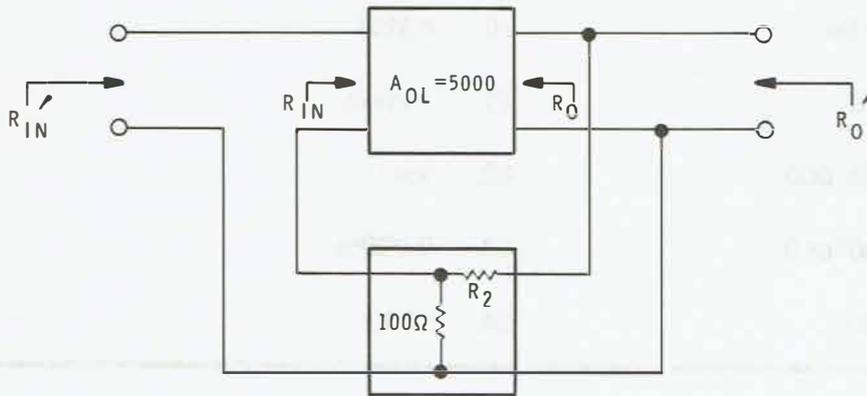


Figure 6-32

Circuit for Self-Test Review questions 20-24.

20. The value of R_2 required to obtain a closed loop gain of 50 is _____ $k\Omega$.
21. Assuming $R_{IN} = 1k\Omega$, the value of R_{IN}' is approximately _____ $k\Omega$.
22. Assuming $R_O = 10k\Omega$, the value of R_O' is approximately _____.
23. Without feedback, the output voltage contains 10% harmonic distortion. With feedback, the harmonic distortion is reduced to approximately _____%.
24. If R_2 is changed to $124.9k\Omega$, $A_{OL}B'$ is no longer large compared to unity. In this case, the closed loop gain equals _____.

Answers

- | | |
|-----------------|-------------------|
| 15. 52.04 | 20. 4.9k Ω |
| 16. 300 | 21. 101k Ω |
| 17. 120 000 | 22. 99 Ω |
| 18. 360° or 0° | 23. 0.099% |
| 19. 3k Ω | 24. 1000 |

Solutions to questions 15 through 24 follow.

$$15. A_{V_T} = A_{V_1} A_{V_2}$$

$$A_{V_T} = (-25)(-16) = 400$$

Converting to decibels:

$$A_{V_{TdB}} = 20 \log A_{V_T} = 20 \log 400 = 52.04\text{dB}$$

$$16. A_{z_T} = \frac{A_{V_T} R_{IN_1}}{R_L} = \frac{400(6\text{k}\Omega)}{8\text{k}\Omega} = 300$$

$$17. A_{P_T} = \frac{(A_{V_T})^2 R_{IN_1}}{R_L} = \frac{(400)^2(6\text{k}\Omega)}{8\text{k}\Omega} = 120,000$$

18. Since each common-emitter stage provides a 180° phase shift, the total phase shift is 360°. This is equivalent to a 0° phase shift. Thus, the input and output signals are in phase with each other.

19. The effective load resistance of the first stage is the input resistance of the second stage, or 3k Ω in this case.

$$20. \text{ If } A_{OL}B' \gg 1, A_{CL} \approx \frac{1}{B'} = 1 + \frac{R_2}{R_1}$$

Thus:

$$1 + \frac{R_2}{R_1} = 50$$

$$\frac{R_2}{R_1} = 50 - 1 = 49$$

$$R_2 = 49R_1$$

Since $R_1 = 100\Omega$:

$$R_2 = 49(100\Omega) = 4.9\text{k}\Omega$$

$$21. \quad B' = \frac{R_1}{R_1 + R_2} = \frac{100\Omega}{100\Omega + 4.9\text{k}\Omega} = 0.02$$

$$R_{IN}' = R_{IN}(1 + A_{OL}B')$$

$$R_{IN}' = 1\text{k}\Omega[1 + 5000(0.02)] = 101\text{k}\Omega$$

$$22. \quad R_{O}' = \frac{R_O}{1 + A_{OL}B'} = \frac{10\text{k}\Omega}{1 + 5000(0.02)} = 99\Omega$$

$$23. \quad D' = \frac{D}{1 + A_{OL}B'} = \frac{10\%}{1 + 5000(0.02)} = 0.099\%$$

$$24. \quad A_{CL} = \frac{A_{OL}}{1 + A_{OL}B'}$$

$$B' = \frac{R_1}{R_1 + R_2} = \frac{100\Omega}{100\Omega + 124.9\text{k}\Omega} = 0.0008$$

Thus:

$$A_{CL} = \frac{5000}{1 + 5000(0.0008)} = \frac{5000}{5} = 1000$$

SUMMARY

Differential amplifiers have two input leads and two output leads. Therefore, numerous operating modes are possible. This makes the differential amplifier a very versatile circuit which is suitable for a wide range of applications. A summary of the most frequently encountered operating modes is provided in Table 6-1.

Differential amplifiers are also referred to as difference amplifiers because they are often used to obtain an output voltage that is directly proportional to the difference between two input voltages. It is useful to think of each input voltage as containing a differential-mode and a common-mode component.

A well designed differential amplifier has a large differential-mode gain and a small common-mode gain. The ratio of the differential- and common-mode gains is called the common-mode rejection ratio, CMRR. The larger the CMRR, the more ideal the amplifier.

The value of the CMRR is largely determined by the quality of the constant current source used to bias the transistors in the differential amplifier. To obtain large CMRRs, it is necessary to utilize a BJT constant current source. Examples illustrating the analysis and design of three typical constant current sources were provided in this unit.

Differential amplifiers exhibit outstanding noise immunity. This is because most noise appears as a common-mode signal and is therefore rejected by the amplifier.

Multistage amplifiers frequently consist of two or more RC coupled common-emitter stages. When you are analyzing or designing multistage amplifiers, it is important to realize that the input resistance of the following stage is the effective load resistance of the previous stage.

By employing a block approach, formulas for the various gains and resistance levels were obtained. In addition, examples illustrating the analysis and design of a two-stage circuit were provided in the unit.

Many practical amplifiers utilize some form of negative feedback to obtain stable voltage gains. In this unit, the voltage-series negative feedback configuration was discussed in some detail.

The addition of voltage-series, negative feedback to a two-stage common-emitter amplifier results in increased input resistance, decreased output resistance, less distortion, and a voltage gain that is largely independent of parameter variations. The price paid for these improvements is a lower value of voltage gain.

UNIT EXAMINATION

The following multiple choice examination is designed to test your understanding of the material presented in this unit. Place a check beside the multiple choice answer (A, B, C, or D) that you feel is most correct. When you have completed the examination, compare your answers with the correct ones that appear after the exam.

Refer to Figure 6-33 for questions 1 through 6.

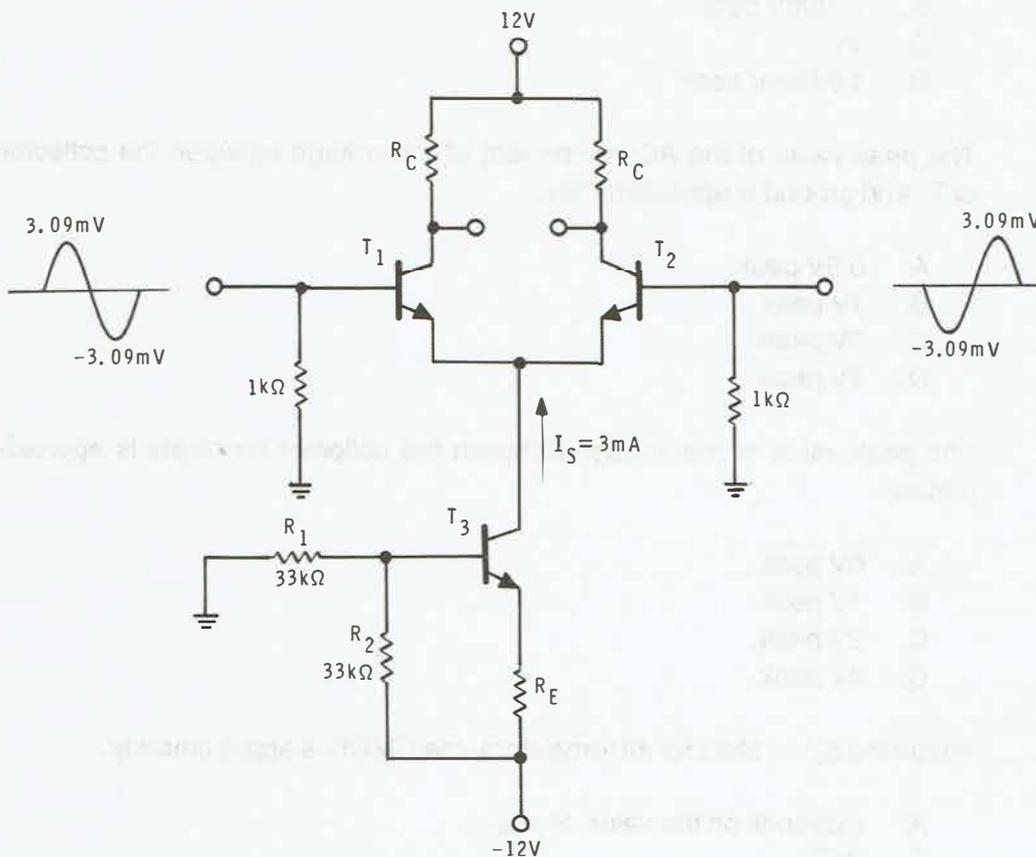


Figure 6-33

Circuit for questions 1 to 6.

1. R_C should equal approximately:

- A. $8\text{k}\Omega$.
- B. $4\text{k}\Omega$.
- C. $33\text{k}\Omega$.
- D. R_E .

2. R_E should equal approximately:
- A. $3.53k\Omega$.
 - B. R_C .
 - C. $1.77k\Omega$.
 - D. $10k\Omega$.
3. The differential input voltage is:
- A. $3.09mV$ peak.
 - B. $6.18mV$ peak.
 - C. $0V$.
 - D. $1.545mV$ peak.
4. The peak value of the AC component of the voltage between the collector of T_1 and ground is approximately:
- A. $0.5V$ peak.
 - B. $1V$ peak.
 - C. $0V$ peak.
 - D. $2V$ peak.
5. The peak value of the voltage between the collector terminals is approximately:
- A. $0V$ peak.
 - B. $1V$ peak.
 - C. $2V$ peak.
 - D. $4V$ peak.
6. Assuming $r_C' = 2M\Omega$ for all transistors, the CMRR is approximately:
- A. Depends on the value of v_{CM} .
 - B. $0dB$.
 - C. $60dB$.
 - D. $98.2dB$.

Refer to Figure 6-34 for questions 7 through 11.

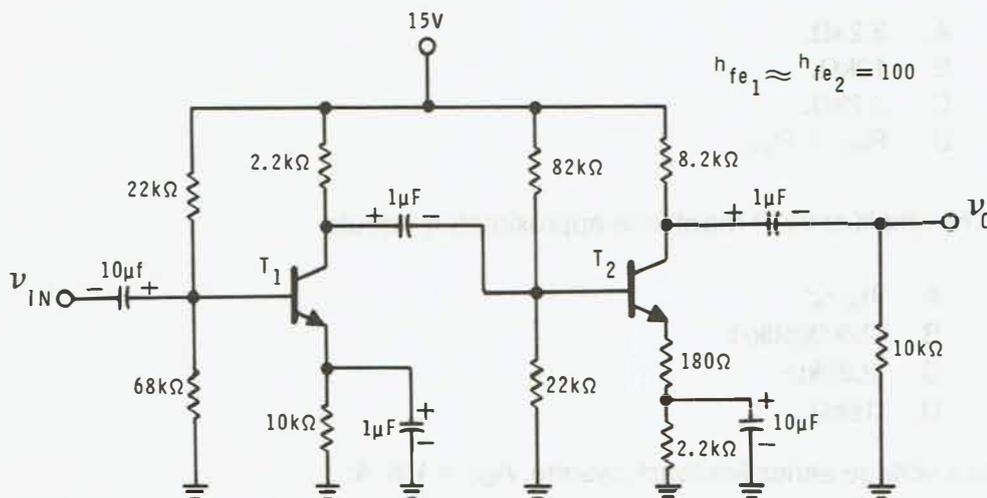


Figure 6-34

Circuit for questions 7 to 11.

7. The voltage gain of the second stage is approximately:
 - A. -20.9.
 - B. -126.4.
 - C. +126.4.
 - D. -210.

8. The voltage gain of the first stage is approximately:
 - A. -22.
 - B. -124.6.
 - C. -60.
 - D. -51.3.

9. The total current gain provided by both stages is approximately:
 - A. 276.
 - B. -276.
 - C. 308.8.
 - D. α .

10. The amplifier's output resistance approximately equals:

- A. $8.2\text{k}\Omega$.
- B. $10\text{k}\Omega$.
- C. $2.2\text{k}\Omega$.
- D. $R_{IN_1} + R_{IN_2}$.

11. The amplifier input resistance approximately equals:

- A. $h_{fe_1}r_{e_1}$.
- B. $22\text{k}\Omega \parallel 68\text{k}\Omega$.
- C. $2.88\text{k}\Omega$.
- D. $16\text{k}\Omega$.

12. In a voltage-series feedback system, $A_{CL} \approx 1/B'$ if:

- A. A_{OL} is large.
- B. B' is large.
- C. $A_{OL}B' \ll 1$.
- D. $A_{OL}B' \gg 1$.

13. Negative voltage-series feedback:

- A. Increases R_{IN} .
- B. Decreases R_{IN} .
- C. Increases R_O .
- D. Increases the amount of harmonic distortion.

14. The term loop gain refers to:

- A. $A_{OL}/(1 + A_{OL}B')$.
- B. v_f .
- C. $1 + A_{OL}B'$.
- D. $A_{OL}B'$.

EXAMINATION ANSWERS

1. B — $R_C = \frac{V_{CC}}{I_S} = \frac{12V}{3mA} = 4k\Omega$

2. C — Using the constant current source design guide number 1:

$$V_{R_2} = \frac{V_{EE}}{2} = \frac{12V}{2} = 6V$$

$$R_E = \frac{V_{R_2} - V_{BE}}{I_S} = \frac{6V - 0.7V}{3mA} = 1.77k\Omega$$

3. B — $v_d = (v_1 - v_2)$
 $v_d = 3.09mV - (-3.09mV)$
 $v_d = 6.18mV$ peak

4. A — Referring to Table 6-1 for dual-input single-output operation, we find:

$$v_O = \frac{R_C}{2r_{e'}} (v_1 - v_2)$$

Since $I_E = I_S/2$ or 1.5mA:

$$r_{e'} = \frac{37mV}{I_E} = \frac{37mV}{1.5mA} = 24.7\Omega$$

Thus:

$$v_O = \frac{4k\Omega}{2(24.7\Omega)} (6.18mV) = 0.5V$$
 peak

5. B — The output obtained between the collectors is double the output obtained from either collector to ground. Thus, $v_O = 2(0.5V)$ or 1V peak.

6. D — First calculate the values of the differential- and common-mode voltage gains.

$$A_d = \frac{-R_C}{2r_{e'}} = \frac{4\text{k}\Omega}{2(24.7\Omega)} = -81$$

$$A_{CM} = \frac{-R_C}{2r_{C'}} = \frac{-4\text{k}\Omega}{2(2\text{M}\Omega)} = -0.001$$

Now:

$$\text{CMRR} = \frac{A_d}{A_{CM}} = \frac{-81}{-0.001} = 81,000$$

Finally, converting to dB notation:

$$\text{CMRR}_{\text{dB}} = 20 \log 81,000 = 98.2$$

7. A — First calculate the values of r_{e_2}' and r_{L_2} :

$$V_{B_2} = \frac{15\text{V}(22\text{k}\Omega)}{82\text{k}\Omega + 22\text{k}\Omega} = 3.17\text{V}$$

$$V_E = V_{B_2} - V_{BE} = 3.17\text{V} - 0.7\text{V} = 2.47\text{V}$$

$$I_{E_2} = \frac{V_{E_2}}{180\Omega + 2.2\text{k}\Omega} = \frac{2.47\text{V}}{2.38\text{k}\Omega} = 1.04\text{mA}$$

$$r_{e_2}' = \frac{37\text{mV}}{I_{E_2}} = \frac{37\text{mV}}{1.04\text{mA}} = 35.6\Omega$$

$$r_{L_2} = R_{C_2} \parallel R_L = 8.2\text{k}\Omega \parallel 10\text{k}\Omega = 4.5\text{k}\Omega$$

Thus:

$$A_{v_2} = \frac{-r_{L_2}}{180\Omega + 35.6\Omega} = -\frac{4.5\text{k}\Omega}{215.6\Omega} = -20.9$$

8. D — Since $R_{L1} = R_{IN2}$, you begin by calculating R_{IN2} .

$$R_{IN(BASE\ 2)} = h_{fe2}(180\Omega + 35.6\Omega)$$

$$R_{IN(BASE\ 2)} = 100(215.6\Omega) = 21.6k\Omega$$

$$R_{IN2} = 82k\Omega \parallel 22k\Omega \parallel 21.6k\Omega$$

$$R_{IN2} = 17.3k\Omega \parallel 21.6k\Omega = 9.6k\Omega$$

$$r_{L1} = R_{C1} \parallel R_{IN2}$$

$$r_{L1} = 2.2k\Omega \parallel 9.6k\Omega = 1.79k\Omega$$

Now:

$$V_{B1} = \frac{15V(68k\Omega)}{22k\Omega + 68k\Omega} = 11.3V$$

$$V_{E1} = V_{B1} - V_{BE} = 11.3V - 0.7V = 10.6V$$

$$I_{E1} = \frac{V_{E1}}{10k\Omega} = \frac{10.6V}{10k\Omega} = 1.06mA$$

$$r_{e1}' = \frac{37mV}{I_{E1}} = \frac{37mV}{1.06mA} = 34.9\Omega$$

Thus:

$$A_{V1} = -\frac{r_{L1}}{r_{e1}'} = -\frac{1.79k\Omega}{34.9\Omega} = -51.3$$

9. C — First calculate R_{IN1} and A_{V1} .

$$R_{IN(BASE\ 1)} = h_{fe1}r_{e1}'$$

$$R_{IN(BASE\ 1)} = 100(34.9\Omega) = 3.49k\Omega$$

$$R_{IN1} = 22k\Omega \parallel 68k\Omega \parallel 3.49k\Omega$$

$$R_{IN1} = 16.6k\Omega \parallel 3.49k\Omega = 2.88k\Omega$$

$$A_{V1} = A_{V1}A_{V2}$$

$$A_{V1} = (-51.3)(-20.9) = 1,072.17$$

Thus:

$$A_{V1} = \frac{A_{V1}R_{IN1}}{R_L} = \frac{(1,072.17)(2.88k\Omega)}{10k\Omega} = 308.8$$

10. A — $R_O \approx R_{C_2} = 8.2\text{k}\Omega$
11. C — $R_{IN} = R_{IN_1} = 2.88\text{k}\Omega$
12. D — Since $A_{CL} = \frac{A_{OL}}{1 + A_{OL}B'}$, A_{CL} will approximately equal $1/B'$ when $A_{OL}B' \gg 1$.
13. A — Negative voltage-series feedback, ideally, increases R_{IN} by $(1 + A_{OL}B')$.
14. D — $A_{OL}B'$ is called the loop gain.

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UNIT 7

FIELD EFFECT TRANSISTORS

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INTRODUCTION

Like the bipolar transistor, or BJT, the field-effect transistor, or FET, is an example of a three-terminal amplifying device. However, since the FET only requires majority carriers for proper operation, it is referred to as a unipolar device.

Basically there are two types of field-effect transistors. One type is known as a junction field effect transistor, or JFET. The second type is called an insulated gate field effect transistor, or IGFET. This type transistor is also referred to as a metal-oxide semiconductor field effect transistor or MOSFET.

In this unit, you will examine both types of field-effect transistors. In addition, you will learn why FETs are superior to BJTs in certain applications. Finally, you will examine typical FET small-signal amplifier circuits, and compare the characteristics of these circuits with the BJT circuits discussed previously.

UNIT OBJECTIVES

When you have completed this unit, you should be able to:

1. Describe the basic structure and operation of JFETs and IGFETs.
2. Define the following FET parameters: I_{DSS} , $V_{GS(off)}$, g_{mo} , K , BV_{GSS} , and g_{os} .
3. Construct bias curves for self-bias and voltage-divider JFET circuits.
4. Analyze self-bias, voltage-divider bias, and current-source bias common-source voltage amplifiers.
5. Use simplified design procedures to design JFET common-source voltage amplifiers.

UNIT ACTIVITY GUIDE

- Read section on “FET Basics.”
- Answer Self-Test Review Questions 1-10.
- Read section on “FET Circuit Analysis and Design.”
- Answer Self-Test Review Questions 11-20.
- Perform Experiment 12 in Unit 9.
- Study Summary.
- Complete Unit Examination.
- Check Examination Answers.

FET BASICS

BJTs are current-controlled, low input resistance devices. Internally, in both NPN and PNP BJTs, the flow of electrons **and** holes is necessary for proper BJT operation.

FETs on the other hand are voltage-controlled high input resistance devices. Internally, FET operation depends only on the flow of majority carriers; electrons in N-channel devices and holes in P-channel devices. For this reason, FETs are considered unipolar devices.

A basic knowledge of FET construction is useful in order to understand how the device operates. Therefore, we will first consider the physical aspects of selected FETs prior to discussing their electrical characteristics.

JFET Construction

The construction of a JFET begins with a lightly doped, semiconductor slab of silicon, called the **substrate**. The substrate serves as a chassis on which the remaining electrodes are formed. This substrate can be either a P-type or an N-type material. Through the use of diffusion and epitaxial growth techniques, an oppositely doped region is formed within the substrate, thus creating a PN junction. However, it is the shape of this PN junction that provides the JFET with its unique characteristics.

The device created by the process just described is shown in Figure 7-1. Here, the U-shaped region embedded in the substrate forms a **channel** of oppositely doped semiconductor material through the substrate. When this channel is made from N-type material and embedded in a P-type substrate, the entire structure forms an N-channel JFET. Similarly, a P-channel JFET consists of a P-type channel embedded in an N-type substrate.

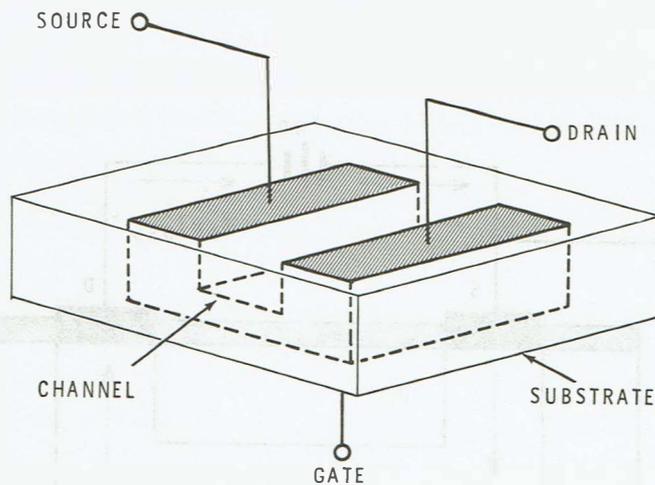


Figure 7-1

Basic construction of a JFET.

A JFET is similar to a BJT in that it can be constructed in two ways. The JFET is either an N-channel or a P-channel device, while the BJT is either an NPN or a PNP device. For this reason, the current directions and voltage polarities of N-channel JFETs are just the opposite of those for P-channel JFETs.

The construction of the JFET in Figure 7-1 is completed by attaching three leads to the device. The leads attached to each end of the channel are referred to as the **source** and **drain**, and the lead attached to the substrate is called the **gate**.

The schematic symbols used to represent JFETs are shown in Figure 7-2. Note that the only difference between the two symbols is the direction of the arrow on the gate lead, G. The N-channel JFET symbol has an arrow that points inward, while the P-channel JFET symbol has an arrow that points outward.

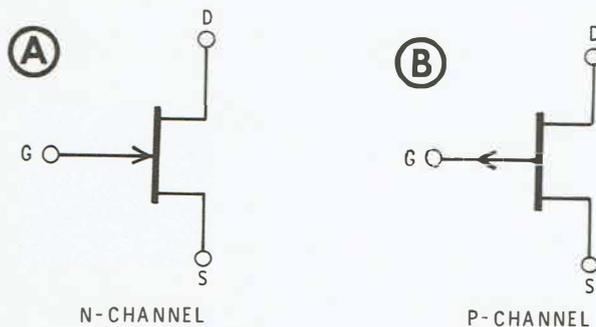


Figure 7-2

JFET schematic symbols.

- A. N-channel.
- B. P-channel.

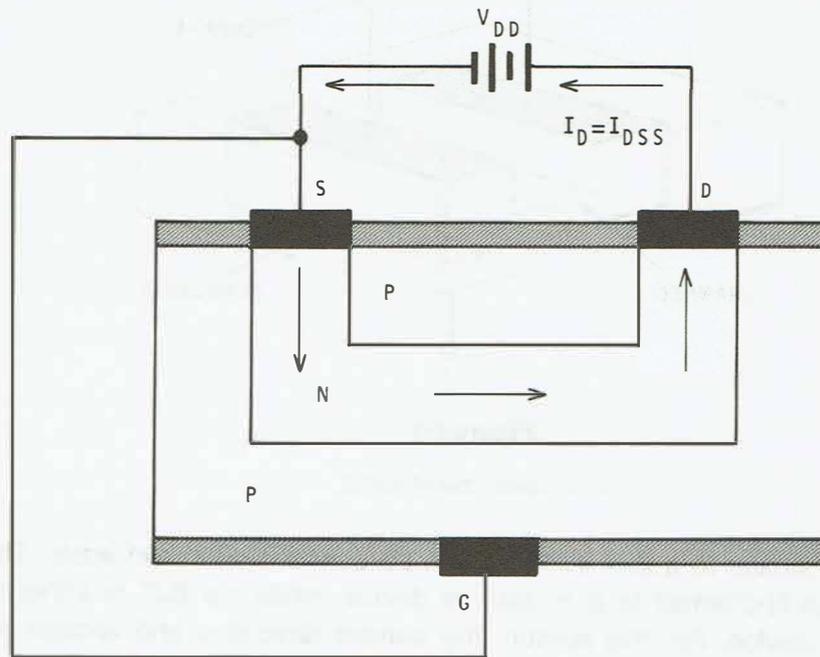


Figure 7-3

Cross section view of an N-channel JFET with $V_{GS} = 0V$. For this "shorted gate" condition, I_D is maximum and is designated as I_{DSS} .

JFET Operation

Like a conventional BJT, a JFET requires two bias voltages for proper operation. One voltage source is connected between the source and drain leads to establish a current flow through the channel within the JFET. The second voltage source is connected between the gate and source leads and is used to control the amount of current flowing through the channel.

A cross section view of an N-channel JFET is shown in Figure 7-3. Here, an external voltage source, V_{DD} , is connected between the drain, D, and the source, S, leads. Note that the gate, G, and source, S, leads are also connected together. For this reason, the gate-to-source voltage, V_{GS} , equals zero.

In Figure 7-3, V_{DD} establishes a current flow through the N-type channel because of the majority carriers, free electrons, within the N-type material. This source-to-drain current is simply referred to as the FET's drain current, I_D . The maximum possible drain current is obtained when V_{GS} equals zero. For a given FET, manufacturers specify this maximum value as I_{DSS} . Since $V_{GS} = 0V$ in Figure 7-3 it is clear that $I_D = I_{DSS}$.

Gate-To-Source Cutoff Voltage

In Figure 7-4A a second voltage source, V_{GG} , has been added to the circuit of Figure 7-3. The polarity of V_{GG} is such that the gate, G, is negative with respect to the source, S. Therefore, V_{GG} reverse biases the PN junction formed by the P-type gate and the N-type channel. Since the resistance of a reversed biased PN junction is quite large, the gate current is very small. For this reason, the input resistance of the JFET is very large — typically in excess of $10M\Omega$.

Most importantly, the reverse bias gate-to-source voltage causes a **depletion region** (an area devoid of majority carriers) to form within the vicinity of the PN junction. As indicated in Figure 7-4A, by the diagonal lines, the depletion region spreads inward along the length of the channel.

The formation of the depletion region effectively reduces the cross sectional area of the channel that is available for current flow. When this occurs, the effective resistance of the channel is increased. This, in turn, results in a value of drain current, I_D , that is less than the value of I_{DSS} .

Increasing the value of V_{GG} increases the size of the depletion region. This further reduces the effective width of the conducting channel. Thus, for a given value of V_{DD} , increases in V_{GG} produce smaller values of drain current, I_D .

If V_{GG} is sufficiently large, the conducting channel is effectively “pinched off” as shown in Figure 7-4B. For all practical purposes, when this happens, the drain current is zero. The gate-to-source voltage required to reduce I_D to zero, regardless of the value of V_{DD} , is referred to as the gate-to-source cutoff voltage and is represented by the symbol $V_{GS(off)}$.

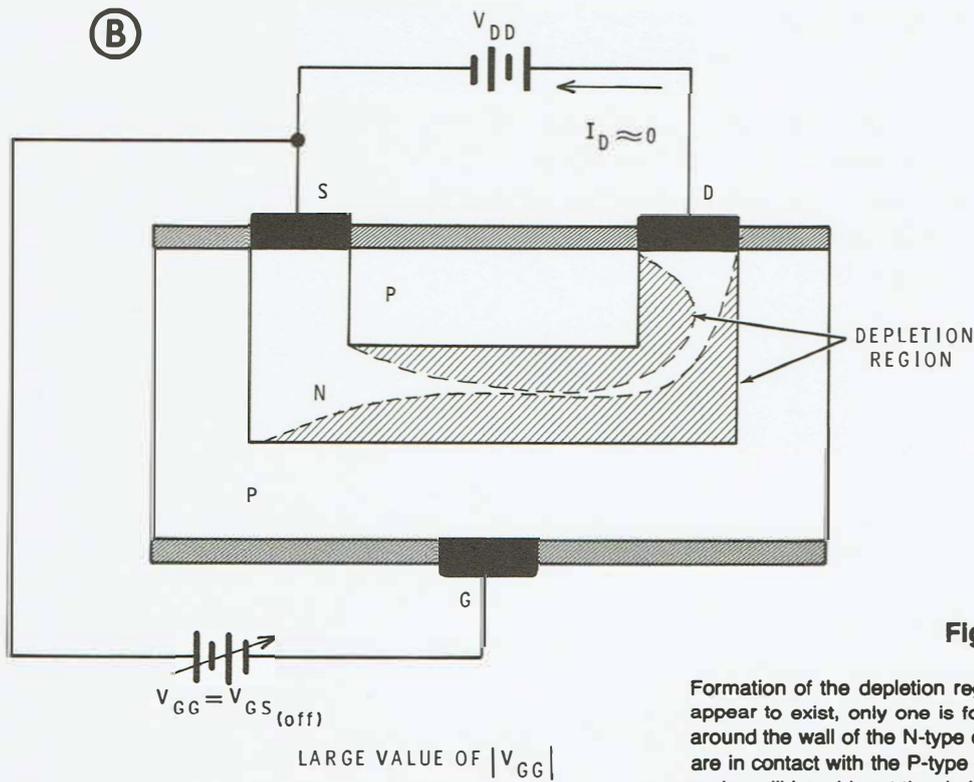
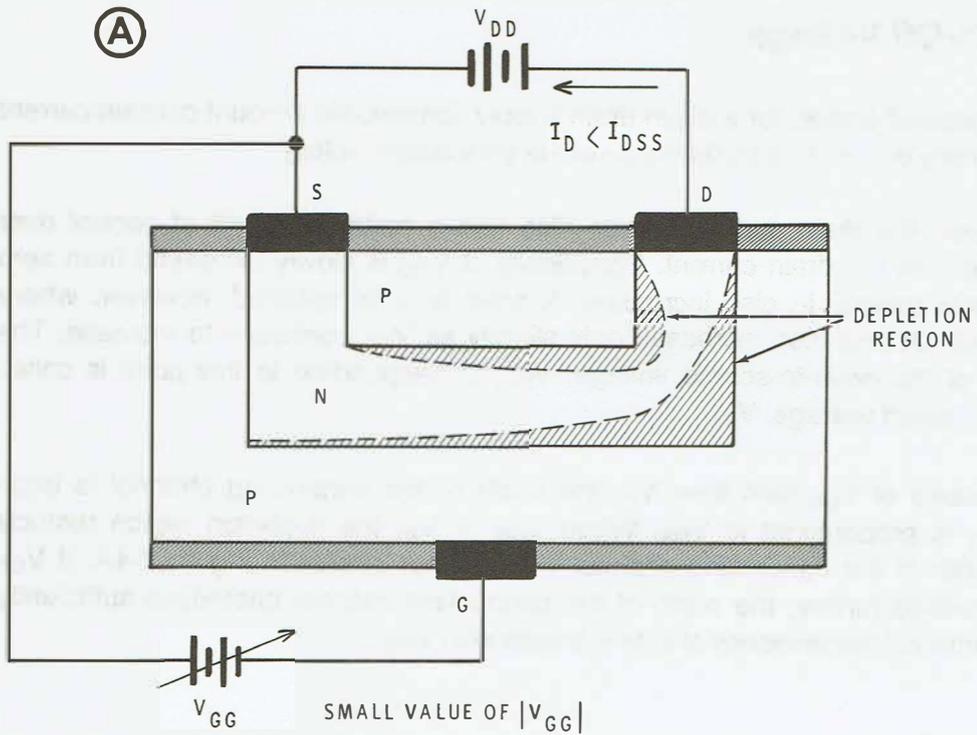


Figure 7-4

Formation of the depletion region. Although two depletion regions appear to exist, only one is formed. This depletion region extends around the wall of the N-type channel since all sides of the channel are in contact with the P-type substrate. Furthermore, the depletion region will be wider at the drain end of the channel. This is because V_{DD} effectively adds to V_{GG} so that the voltage across the drain end of the PN junction is higher than the voltage across the source end of the junction.

- A. Small value of $|V_{GG}|$.
 B. Large value of $|V_{GG}|$.

Pinch-Off Voltage

As explained earlier, for a given drain supply voltage, the amount of drain current is primarily determined by the value of the gate supply voltage.

However, the drain supply voltage also has a certain amount of control over the value of the drain current. Specifically, if V_{DD} is slowly increased from zero to higher values, I_D also increases. A point is soon reached, however, where I_D levels off and then increases only slightly as V_{DD} continues to increase. The value of the drain-to-source voltage, V_{DS} , corresponding to this point is called the **pinch-off voltage, V_P** .

For values of V_{DS} less than V_P , the width of the conducting channel is large and I_D is proportional to V_{DS} . When $V_{DS} = V_P$, the depletion region restricts the width of the conducting channel in a manner similar to Figure 7-4A. If V_{DS} is increased further, the width of the conducting channel decreases sufficiently to counteract the tendency of I_D to increase with V_{DS} .

A graph of drain current versus drain-to-source voltage for a typical JFET appears as shown in Figure 7-5. Note the following:

1. For values of $V_{DS} < V_P$, 3V in this case, I_D is proportional to V_{DS} .
2. For values of V_{DS} between 3V and 30V, I_D is essentially constant and equal to 8mA.
3. The maximum safe drain-to-source voltage, $V_{DS(MAX)}$, is 30V. If V_{DS} exceeds this value, breakdown occurs and the JFET can be damaged.

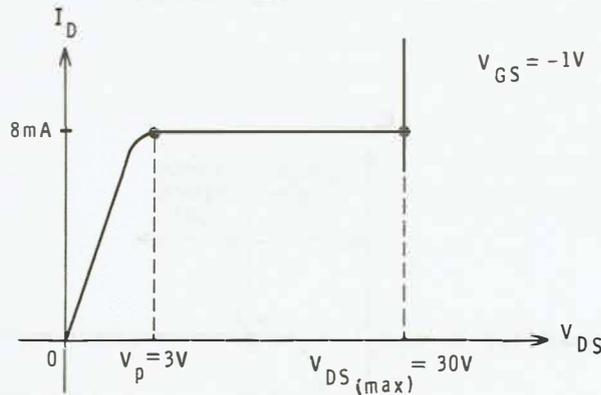


Figure 7-5

Typical drain current versus drain-to-source voltage curve.

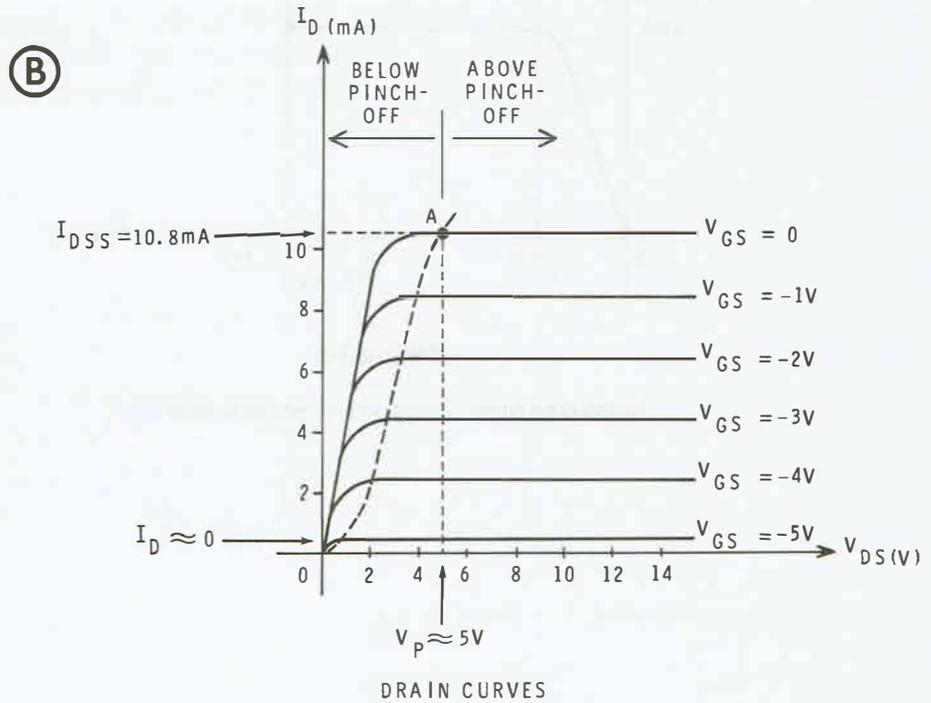
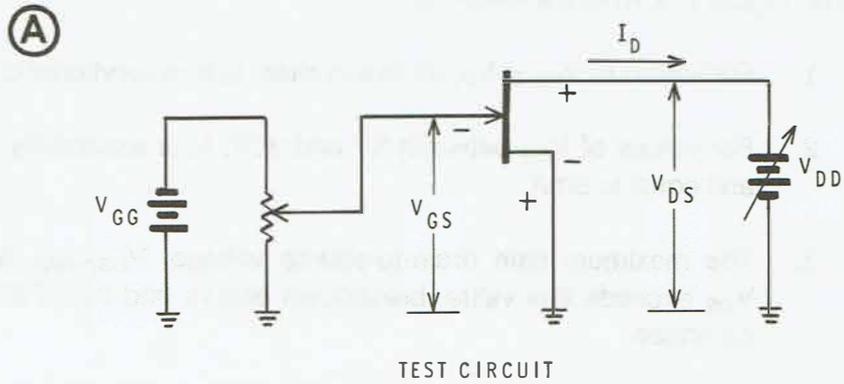


Figure 7-6

Typical drain characteristic curves for an N-channel JFET.

- A. Test circuit.
- B. Drain curves.

Drain Characteristic Curves

In a manner similar to obtaining the collector curves for a BJT, the test circuit shown in Figure 7-6A can be used to obtain the drain curves for an N-channel JFET. Typically, the procedure is as follows:

1. V_{GS} is set to zero.
2. V_{DS} is increased from zero to some maximum value, less than $V_{DS(MAX)}$, while observing the change in I_D .
3. V_{GS} is adjusted to various negative values, and step 2 is repeated for each value.

The resulting family of drain characteristic curves is provided in Figure 7-6B. Notice that when $V_{GS} = 0V$, I_D increases rapidly with increases in V_{DS} . However, I_D quickly levels off as indicated by point A. At point A, the corresponding values of I_D and V_{DS} are:

$$I_D = I_{DSS} = 10.8\text{mA}$$

$$V_{DS} = V_P = 5V$$

The remaining curves in Figure 7-6B are plotted for high values of V_{GS} . Notice that for each higher value of V_{GS} , I_D levels off at a lower value so that the corresponding pinch-off voltage, V_P , must also be lower. In Figure 7-6B, the dashed line that goes upward and to the right crosses each curve at the approximate point where I_D is pinched off. The region to the left of the dashed line is referred to as the ohmic region. On the other hand, the region to the right of the dashed line is referred to as the pinch-off region.

In most applications, the FET is biased so that:

$$V_P < V_{DS} < V_{DS(MAX)}$$

In Figure 7-6B note that:

1. When $V_{GS} = 0V$, $V_P \approx 5V$
2. $V_{GS(off)} \approx -5V$

In practice, the value of V_P will always be close to the absolute value of $V_{GS(off)}$. Consequently, operation within the pinch-off region is assured simply by making V_{DS} higher than V_P or $V_{GS(off)}$. In addition, since the operation of the JFET is controlled by varying the depletion region within the device, the JFET is said to operate in the **depletion mode**.

Transconductance Curve

Recall that a device's transconductance curve is obtained by plotting output current versus input voltage. For this reason, the transconductance curve for a JFET consists of a plot of drain current, I_D , versus gate-to-source voltage, V_{GS} , as shown in Figure 7-7. Note that:

1. The vertical intercept of the transconductance curve equals I_{DSS} .
2. The horizontal intercept of the transconductance curve equals $V_{GS(off)}$.
3. Mathematically, the equation that describes the transconductance curve is:

$$I_D = I_{DSS} \left[1 - \frac{|V_{GS}|}{|V_{GS(off)}|} \right]^2 \quad (\text{Eq. 7-2})$$

Assuming the values of I_{DSS} and $V_{GS(off)}$ are known, Equation 7-2 can be used to estimate the drain current, I_D , for different values of gate-to-source voltage, V_{GS} .

Example 7-1

An N-channel JFET has an I_{DSS} of 20mA, and a $V_{GS(off)}$ of $-2V$. Estimate the drain current if $V_{GS} = -1V$.

$$I_D = I_{DSS} \left[1 - \frac{|V_{GS}|}{|V_{GS(off)}|} \right]^2$$

$$I_D = 20\text{mA} \left[1 - \frac{1V}{2V} \right]^2$$

$$I_D = 20\text{mA}(0.5)^2 = 5\text{mA}$$

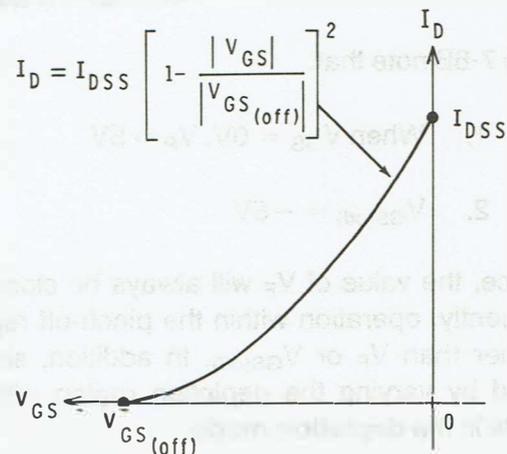


Figure 7-7

JFET transconductance curve.

Normalized Transconductance Curve

A JFET's drain current is described by Equation 7-2. If you divide both sides of Equation 7-2 by I_{DSS} you obtain:

$$\frac{I_D}{I_{DSS}} = \left[1 - \frac{|V_{GS}|}{|V_{GS(off)}|}\right]^2 \quad (\text{Eq. 7-3})$$

By substituting values between 0.05 and 1 into Equation 7-3 for the $|V_{GS}|/|V_{GS(off)}|$ ratio, you obtain the data provided in Table 7-1.

$ V_{GS} / V_{GS(off)} $	I_D/I_{DSS}
1	0
0.9	0.01
0.8	0.04
0.7	0.09
0.6	0.16
0.5	0.25
0.4	0.36
0.3	0.49
0.2	0.64
0.1	0.81
0.05	0.90

TABLE 7-1

Normalized JFET transconductance curve data

Similarly, by graphing the data in Table 7-1, you obtain the normalized JFET transconductance curve shown in Figure 7-8. Since this curve applies to virtually any JFET, it will prove useful for the analysis and design of JFET circuits.

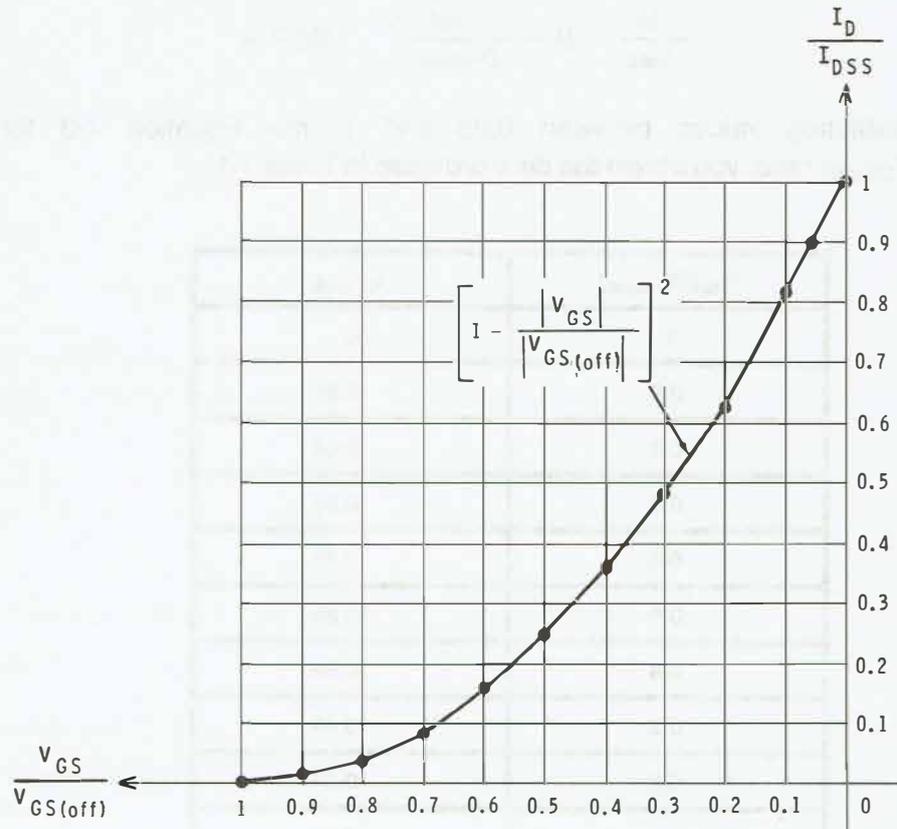


Figure 7-8

Normalized JFET transconductance curve.

Example 7-2

A JFET has an I_{DSS} of 8mA and a $V_{GS(off)}$ of $-4V$. What is the value of V_{GS} if the JFET is biased at $I_D = 4.4mA$?

$$\frac{I_D}{I_{DSS}} = \frac{4.4mA}{8mA} = 0.55$$

Referring to Figure 7-8, you can see that for $I_D/I_{DSS} = 0.55$, the corresponding value of $V_{GS}/V_{GS(off)}$ is approximately, 0.26.

Thus:

$$\frac{V_{GS}}{V_{GS(off)}} = 0.26$$

Since $V_{GS(off)} = -4V$:

$$V_{GS} = 0.26(-4V) = -1.04V$$

Transconductance

Transconductance, g_m , is measured in Siemens and is an important JFET parameter. Specifically, g_m is a measure of the ability of gate-to-source voltage to control drain current. Stated mathematically:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}, V_{DS} = \text{CONSTANT} \quad (\text{Eq. 7-4})$$

Where: ΔI_D and ΔV_{GS} represent **small changes** in the drain current, and gate-to-source voltages respectively.

On a data sheet, transconductance is usually indicated by one of the following symbols: g_m , g_{fs} , or y_{fs} . In addition, most data sheets list the value of g_m for $V_{GS} = 0$. This particular value of g_m , is denoted by g_{mo} .

The value of g_{mo} is related to the values of I_{DSS} and $V_{GS(off)}$ as follows:

$$g_{mo} = \frac{2I_{DSS}}{|V_{GS(off)}|} \quad (\text{Eq. 7-5})$$

Alternately, you can estimate $|V_{GS(off)}|$ if the values of g_{mo} and I_{DSS} are known through the equation:

$$|V_{GS(off)}| = \frac{2I_{DSS}}{g_{mo}} \quad (\text{Eq. 7-6})$$

Graphically, the transconductance parameter, g_m , represents the slope between two adjacent points on the JFET's transconductance curve. The following formula lets you estimate the value of g_m for V_{GS} values between 0 and $V_{GS(off)}$.

$$g_m = g_{mo} \left[1 - \frac{|V_{GS}|}{|V_{GS(off)}|} \right]$$

As with Equation 7-2, it is useful to normalize Equation 7-7 and plot the results.

Dividing both sides of Equation 7-7 by g_{m0} yields:

$$\frac{g_m}{g_{m0}} = \left[1 - \frac{|V_{GS}|}{|V_{GS(off)}|} \right] \quad (\text{Eq. 7-8})$$

Figure 7-9 is the graph of Equation 7-8 for values of the $|V_{GS}|/|V_{GS(off)}|$ ratio between 0.1 and 1.

Example 7-3

A JFET has an I_{DSS} of 4mA and a g_{m0} of $2,000\mu\text{S}$. Determine:

- (a) $V_{GS(off)}$
 (b) The values of I_D , V_{GS} , and g_m , assuming the JFET is biased at $I_D = 0.6I_{DSS}$.

$$(a) \quad |V_{GS(off)}| = \frac{2I_{DSS}}{g_{m0}} = \frac{2(4\text{mA})}{2,000\mu\text{S}} = 4\text{V}$$

Assuming the JFET is an N-channel device $V_{GS(off)} = -4\text{V}$.

$$(b) \quad I_D = 0.6I_{DSS} = 0.6(4\text{mA}) = 2.4\text{mA}$$

Referring to Figure 7-8 we note that an I_D/I_{DSS} ratio of 0.6 corresponds to a $V_{GS}/V_{GS(off)}$ ratio of, approximately, 0.225.

Thus:

$$V_{GS} = 0.225(-4\text{V}) = -0.9\text{V}$$

Referring to Figure 7-9 we see that a $V_{GS}/V_{GS(off)}$ ratio of 0.225 corresponds to a g_m/g_{m0} ratio of, approximately, 0.775.

Thus:

$$g_m = 0.775g_{m0} = 0.775(2,000\mu\text{S}) = 1,550\mu\text{S}$$

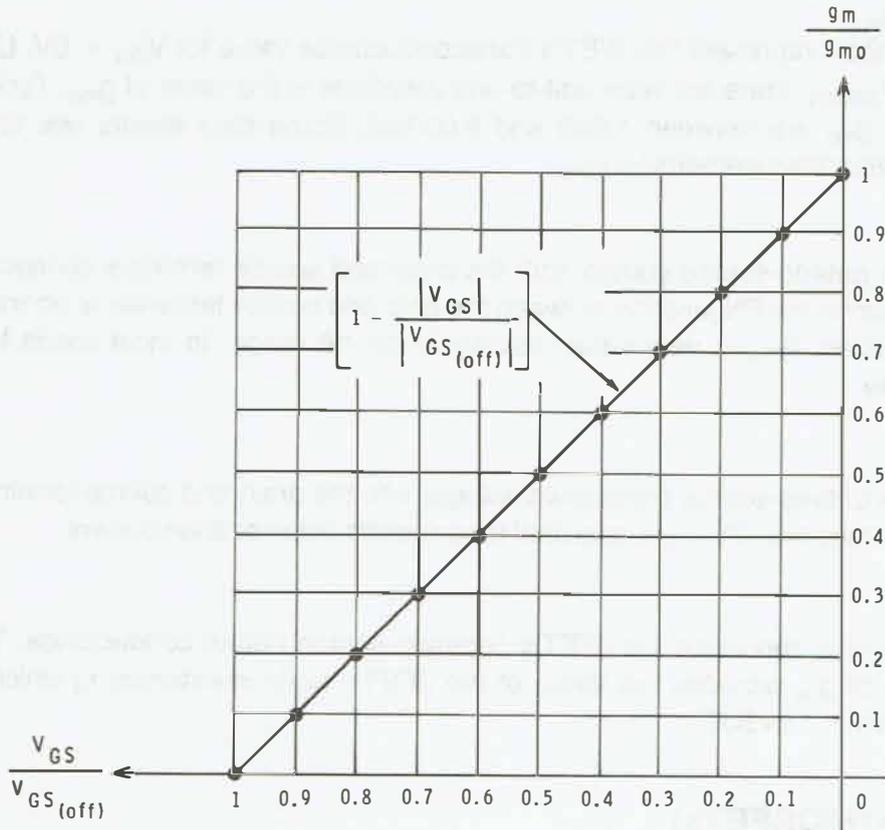


Figure 7-9

A normalized curve for the g_m/g_{m0} ratio.

JFET Parameters

The following is a summary of the major JFET parameters. Some of these parameters were introduced previously. In such cases, additional information is provided to complement and supplement the earlier material.

I_{DSS}

This is the value of I_D when $V_{GS} = 0V$. On some data sheets, I_{DSS} is listed as $I_{D(on)}$, for $V_{DS} > V_P$.

$V_{GS(off)}$

Ideally, $V_{GS(off)}$ is the value of the gate-to-source voltage that results in zero drain current. However, since a JFET's transconductance curve exhibits significant curvature in the vicinity of the knee, it is difficult to define the exact point where $I_D = 0$. For this reason, data sheets usually specify $V_{GS(off)}$ as the value of gate-to-source voltage that produces a drain current of 1% I_{DSS} , or less.

g_{mo} , g_{fs} , Y_{fs}

These symbols represent the JFET's transconductance value for $V_{GS} = 0V$. Like I_{DSS} and $V_{GS(off)}$, there are wide unit-to-unit variations in the value of g_{mo} . Typical values for g_{mo} are between 1,000 and 8,000 μ S. Some data sheets use units of mhos rather than siemens for g_{mo} .

 I_{GSS}

This is the gate-to-source current with the drain and source terminals connected together. Since the PN junction between the gate and source terminals is normally reverse biased, I_{GSS} is very small: usually in the nA range. In most cases I_{GSS} is negligible.

 BV_{GSS}

This is the gate-to-source breakdown voltage with the drain and source terminals connected together. BV_{GSS} is specified for a specific value of drain current.

 g_{os} , Y_{os}

These symbols represent the JFET's common-source output conductance. The reciprocal of g_{os} provides the value of the JFET's drain resistance, r_d which is analogous to r_C' for BJTs.

IGFETs (MOSFETs)

The gate and channel regions within a JFET form a conventional PN junction. This PN junction is reverse biased by an external voltage source. The reverse bias voltage causes the JFET to operate in the depletion mode and allows the device to have a large input resistance. However, there is another type of FET which does not have a conventional PN junction that has to be reversed-biased. This device uses a metal gate which is electrically insulated from its semiconductor channel by a thin layer of silicon dioxide, SiO_2 . Consequently, the device is referred to as an insulated gate FET, IGFET, or a metal-oxide semiconductor FET, MOSFET.

Unlike the JFET, which can only operate in the depletion mode, the IGFET may be either a depletion-mode device or an enhancement-mode device.

Depletion-Mode IGFET

The basic structure of a depletion-mode IGFET is shown in Figure 7-10A. Here, note that the metal gate is insulated from the channel by the layer of silicon dioxide. Note that an additional lead is connected to the substrate. In many IGFETs, this additional (substrate) lead is internally connected to the source; some IGFETs make the connection to the substrate available as a fourth external lead. For simplicity, we will concentrate on those applications where the substrate lead is either internally or externally connected to the source.

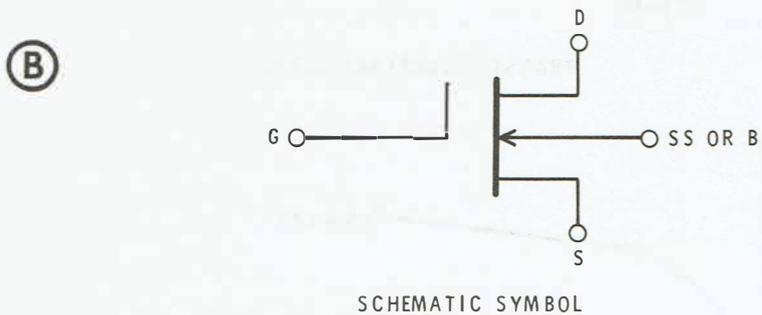
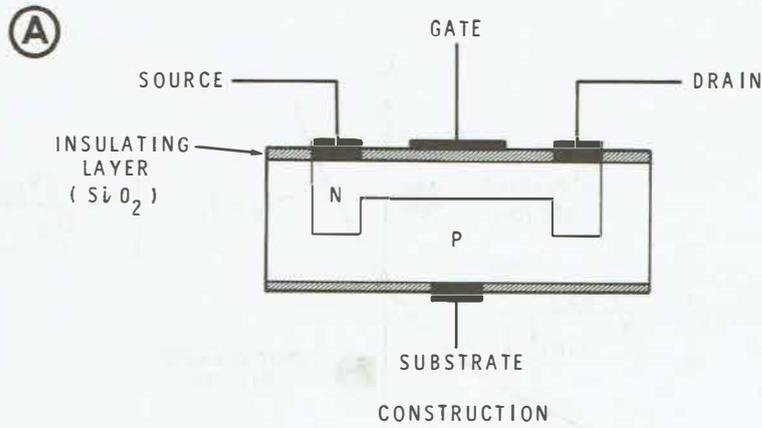


Figure 7-10

The N-channel depletion-mode IGFET (MOSFET).

- A. Construction.
- B. Schematic symbol.

The schematic symbol of an N-channel depletion-mode IGFET is shown in Figure 7-10B. Here, the drain, source, gate, and substrate leads are identified respectively by the letters D, S, G, and either SS or B. Furthermore, the arrow on the substrate lead points inward. As you might suppose, the arrow on the substrate lead of a P-channel depletion-mode IGFET would point outward as shown in Figure 7-11.

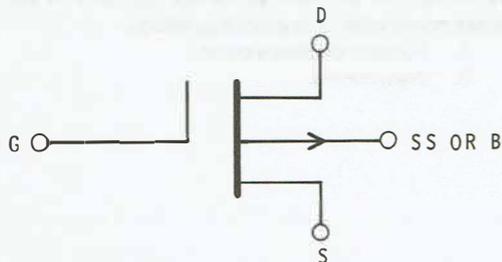


Figure 7-11

Schematic symbol of a P-channel depletion-mode IGFET (MOSFET)

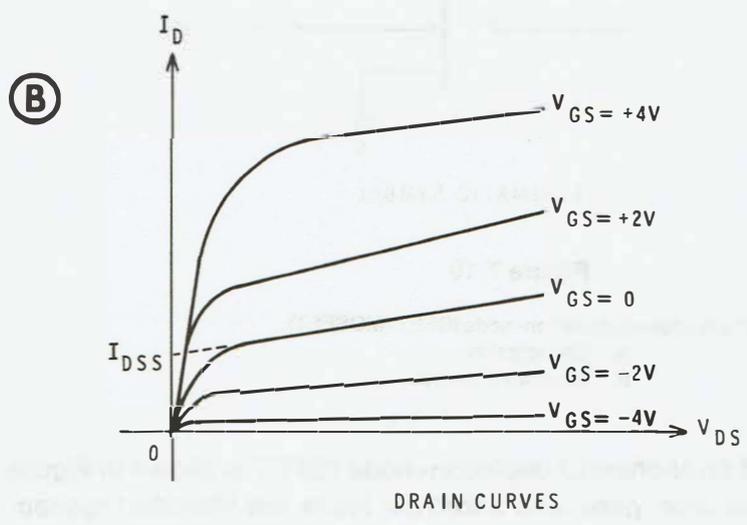
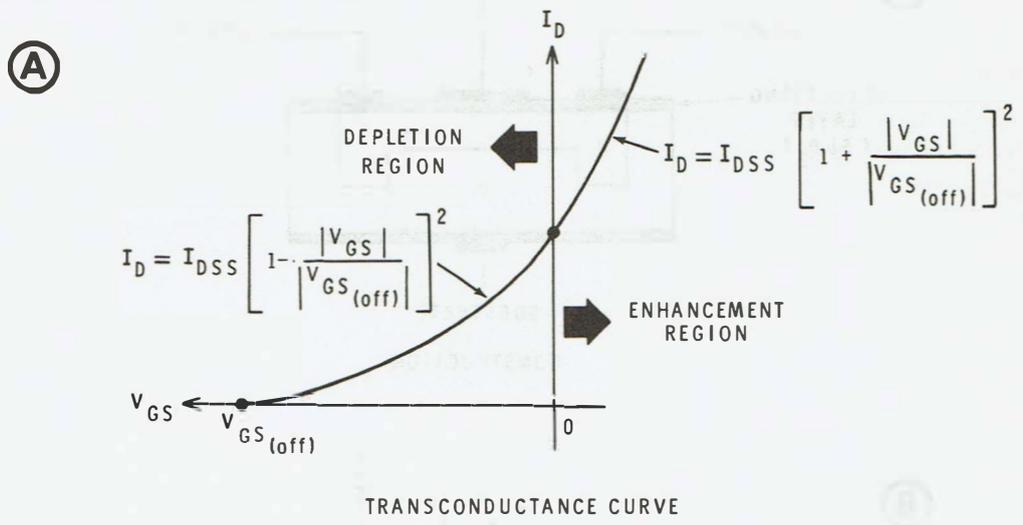


Figure 7-12

Transconductance and drain curves for an N-channel depletion-mode IGFET. Note that this **normally-on** device operates in the enhancement-mode for positive V_{GS} values.

- A. Transconductance curve.
- B. Drain curves.

Negative and Positive V_{GS} Values

Due to the insulating layer, the gate and channel do not form a conventional PN junction. However, a voltage applied between the insulated metal gate and source still controls the conductivity of the channel. Therefore, this voltage also controls the amount of drain current. Furthermore, both negative and positive V_{GS} values are permitted since the insulating layer of silicon dioxide prevents current from flowing through the gate lead.

For negative values of V_{GS} , the IGFET operates in a manner that is similar to a conventional JFET. This is apparent from an examination of the device's transconductance and drain curves shown in Figure 7-12. For negative V_{GS} values, the curves are essentially identical to those of an N-channel JFET. The term depletion-mode device arises from the fact that a negative gate-to-source voltage is required to "deplete" the conducting channel of electrons, and therefore reduce the value of the drain current.

Like the depletion mode JFET described earlier, the depletion-mode IGFET conducts a substantial amount of current, I_{DSS} , when $V_{GS} = 0$. For this reason, all depletion-mode devices, whether junction or insulated gate types, are said to be normally-conducting or **normally-on** when their gate-to-source voltages are zero.

Positive values of V_{GS} increase, or enhance, the number of electrons in the conducting channel of an N-channel IGFET. As shown in Figure 7-12, positive values of V_{GS} produce drain currents larger than I_{DSS} . This is quite different from the operation of a JFET, where positive values of V_{GS} are not permitted because the PN junction formed by the gate and channel would become forward biased.

The essential difference between a JFET and a depletion-mode IGFET is that the JFET can only operate in the depletion mode. An IGFET, on the other hand, can be biased to operate in either the depletion or enhancement mode.

Drain Current Formulas

The equation for the transconductance curve in Figure 7-12A is:

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(off)}} \right]^2 \quad (\text{Eq. 7-9})$$

Since V_{GS} can be positive or negative, the expression $V_{GS}/V_{GS(off)}$ will be positive when V_{GS} is negative, and negative when V_{GS} is positive. Since this can be confusing, it is advisable to divide Equation 7-9 into two parts as follows:

When V_{GS} is negative:

$$I_D = I_{DSS} \left[1 - \frac{|V_{GS}|}{|V_{GS(off)}|} \right]^2 \quad (\text{Eq. 7-9(a)})$$

Similarly, when V_{GS} is positive:

$$I_D = I_{DSS} \left[1 + \frac{|V_{GS}|}{|V_{GS(off)}|} \right]^2 \quad (\text{Eq. 7-9(b)})$$

Example 7-4

An N-channel depletion-mode IGFET has an I_{DSS} of 6mA, and a $V_{GS(off)}$ of $-4V$. Estimate the drain current for $V_{GS} = 0$, $-1V$, and $+1V$.

When $V_{GS} = 0$, $I_D = I_{DSS}$ or 6mA.

When V_{GS} is negative, I_D is calculated using Equation 7-9(a). Thus, for $V_{GS} = -1V$:

$$I_D = I_{DSS} \left[1 - \frac{|V_{GS}|}{|V_{GS(off)}|} \right]^2$$

$$I_D = 6\text{mA} \left[1 - \frac{1V}{4V} \right]^2 = 6\text{mA}(0.5625) = 3.375\text{mA}$$

When V_{GS} is positive, Equation 7-9(b) is used to calculate the drain current. Thus, for $V_{GS} = 1V$:

$$I_D = I_{DSS} \left[1 + \frac{|V_{GS}|}{|V_{GS(off)}|} \right]^2$$

$$I_D = 6\text{mA} \left[1 + \frac{1V}{4V} \right]^2 = 6\text{mA}(1.5625) = 9.375\text{mA}$$

Enhancement-Mode IGFET

An IGFET which functions as a **normally-off** device is shown in Figure 7-13A. This device is similar to the depletion-mode IGFET in Figure 7-10A, but it **does not** have a conducting channel that is imbedded in the substrate material. Instead, the device has source and drain regions that are diffused separately into the substrate.

In Figure 7-13A, the drain current is zero when $V_{GS} = 0$. This is because no conducting channel exists between the source and drain regions. For this reason, $I_{DSS} = 0$ in an enhancement-mode IGFET. Similarly, $I_D = 0$ for negative values of V_{GS} .

If the gate-to-source voltage is sufficiently positive, a conducting channel is induced between the source and drain regions. The action that takes place is similar to the action that takes place in a charging capacitor. In this case, the metal gate and substrate function as the upper and lower plates of a capacitor and the insulating layer functions as the dielectric. When the positive gate voltage charges the "capacitor" so that a negative charge builds up on the substrate plate, an induced N-type channel is formed. Furthermore, an increase in gate voltage tends to increase or enhance the conductivity of the induced channel. For this reason, the device in Figure 7-13A is referred to as an N-channel enhancement-mode IGFET.

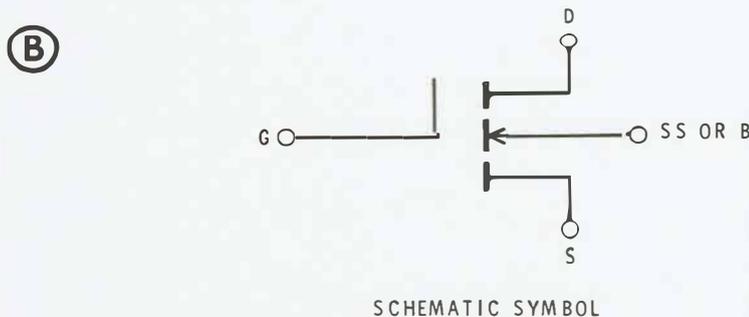
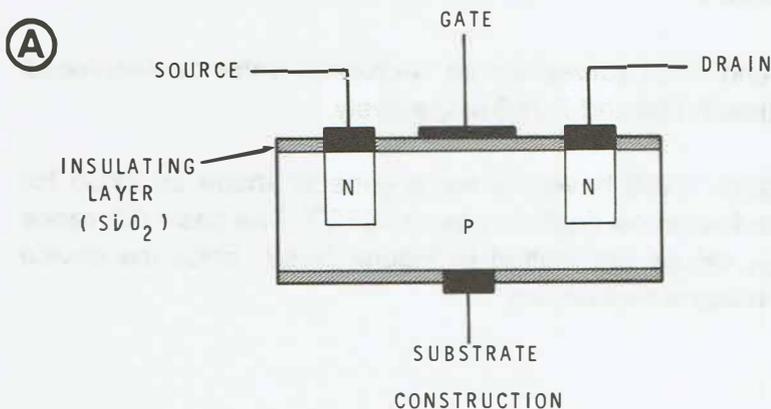


Figure 7-13

The N-channel enhancement-mode IGFET (MOSFET).

- A. Construction.
- B. Schematic symbol.

The schematic symbol for an N-channel, enhancement-mode IGFET is shown in Figure 7-12B. Notice that this symbol is similar to the symbol for the N-channel depletion-mode IGFET. The only difference is the use of a **broken line** instead of a solid line to interconnect the source, drain, and substrate regions. The solid line identifies the normally-on condition of the depletion-mode device, while the broken line is used to identify the normally-off condition of the enhancement-mode device. Once again, the schematic symbol for the P-channel device has the substrate arrow pointing outwards, as shown in Figure 7-14.

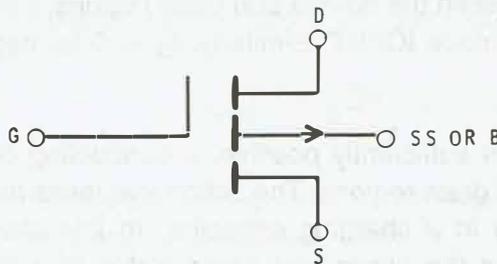


Figure 7-14

Schematic symbol of a P-channel enhancement-mode IGFET (MOSFET).

Characteristic Curves

The transconductance and drain curves for an N-channel enhancement-mode IGFET are shown in Figures 7-15A and 7-15B respectively.

The drain curves in Figure 7-15B have the same general shape as those for an N-channel JFET or an N-channel depletion-mode IGFET. The basic difference is that only positive V_{GS} values are plotted in Figure 7-15B, since the device can only operate in the enhancement region.

In Figure 7-15A note that, for drain current to flow, the gate-to-source voltage must exceed the value of the gate-to-source **threshold voltage**, $V_{GS(T)}$. $V_{GS(T)}$ is usually one volt or more. With appropriate biasing, the enhancement-mode device makes an excellent switch. It can be turned on by a sufficiently high gate voltage. The inherent threshold of the device provides a highly desirable region of noise immunity that prevents low or intermediate noise voltages, less than $V_{GS(T)}$, from falsely triggering the device on. This characteristic makes the enhancement-mode device ideal for digital applications.

As shown in Figure 7-15A, the drain current corresponding to a value of $V_{GS} > V_{GS(T)}$ is also indicated on the device's transconductance curve. Data sheets often provide the value of $V_{GS(on)}$ required to produce a drain current, $I_{D(on)}$, that approximately equals the maximum value given on the family of drain curves.

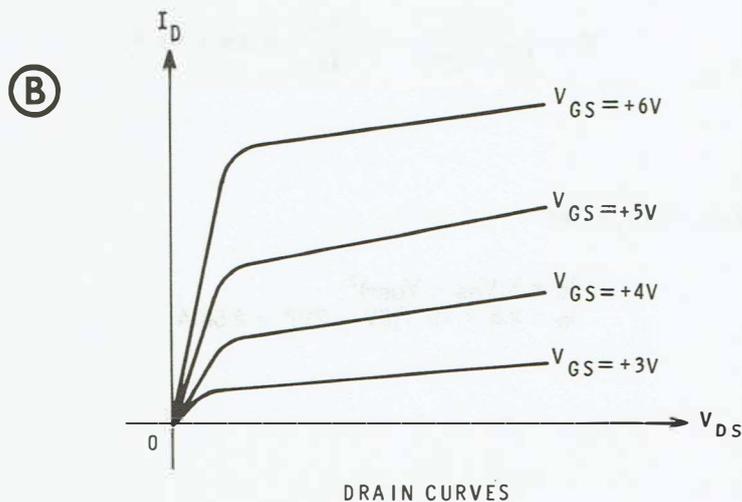
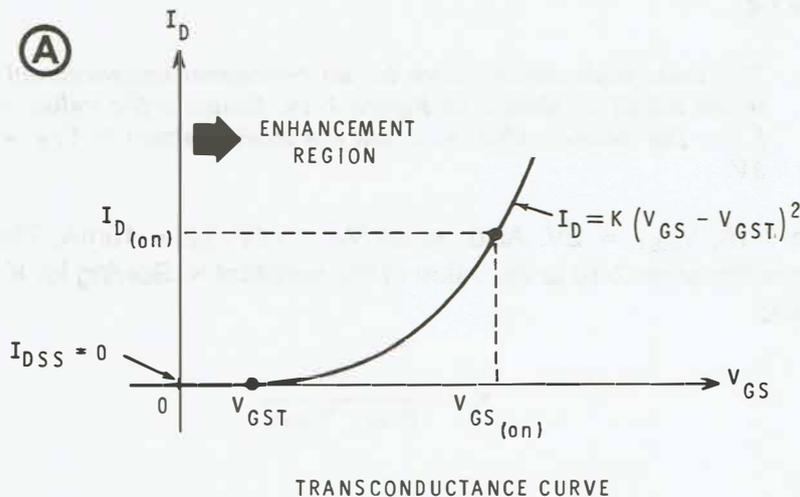


Figure 7-15

Transconductance and drain curves for an N-channel enhancement-mode IGFET. Note that this **normally-off** device only operates in the enhancement region.

- A. Transconductance curve.
- B. Drain curves.

Drain Current Formula

The transconductance curve of an enhancement-mode IGFET is described by:

$$I_D = K(V_{GS} - V_{GST})^2 \quad (\text{Eq. 7-10})$$

Where: K = constant for a particular type enhancement-mode IGFET.
 V_{GST} = gate-to-source threshold voltage.

Obviously, Equation 7-10 is only valid for values of $V_{GS} \geq V_{GST}$. Values of $V_{GS} < V_{GST}$ result in a drain current, I_D , of essentially zero.

Example 7-5

The transconductance curve for an N-channel enhancement-mode IGFET is shown in Figure 7-16. Estimate the value of K for the device. Also, estimate the drain current if $V_{GS} = 3V$.

In Figure 7-16, $V_{GST} = 2V$. Also, when $V_{GS} = 4V$, $I_D = 10mA$. Thus, the only unknown in Equation 7-10 is the value of the constant K . Solving for K in Equation 7-10 yields:

$$K = \frac{I_D}{(V_{GS} - V_{GST})^2}$$

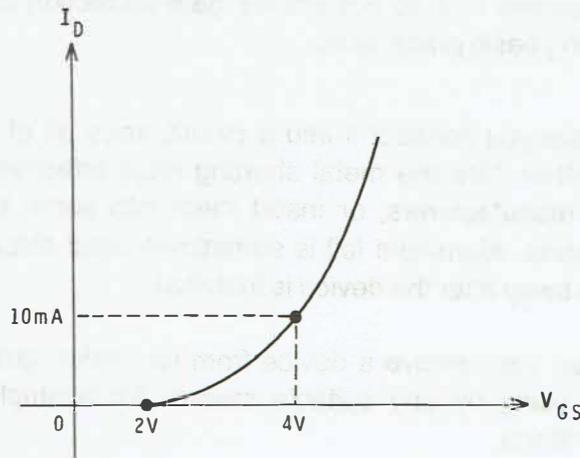
Thus:

$$K = \frac{10mA}{(4V - 2V)^2} = \frac{10mA}{4V} = 2.5 \times 10^{-3}$$

Now, when $V_{GS} = 3V$, I_D is:

$$I_D = K(V_{GS} - V_{GST})^2$$

$$I_D = 2.5 \times 10^{-3}[3V - 2V]^2 = 2.5mA$$

**Figure 7-16**

Transconductance curve for Example 7-5.

Safety Precautions

When you are using any IGFET, you must observe certain precautions. As with any solid-state component, it is necessary to check the manufacturer's maximum ratings so that the device is not damaged by excessively high operating voltages or currents. However, it is particularly important to observe the FET's maximum allowable gate-to-source voltages (V_{GS}). An IGFET (MOSFET) can accept only a limited range of V_{GS} values because of the extremely thin silicon dioxide insulating layer that separates its gate and channel. If V_{GS} is increased too much, the thin insulating layer will be punctured and the device will be ruined. In fact, the insulating layer is so sensitive that it can even be damaged by static charges that build up on the FET's leads. For example, the electrostatic charges on your fingers can be transferred to the FET's leads while you are handling the device or when you are mounting it in a circuit. The device could therefore be ruined before it is used. To avoid this type of damage, manufacturers usually ship these devices with their leads shorted together so that static charges cannot build up between the leads. The leads may be wrapped with a shorting wire, inserted within a shorting ring, pressed into a conducting foam material, or simply taped together. These shorting devices should not be removed until the FET is completely installed in its respective circuit.

Most modern IGFETS are protected by zener diodes which are electrically connected between each insulated gate and the transistor's source inside the device. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms.

You can handle devices that do not include gate-protection diodes safely if you observe the following basic precautions:

1. Before you connect it into a circuit, keep all of the leads shorted together. Use the metal shorting rings attached to the device by the manufacturers, or insert them into some kind of conductive material. Aluminum foil is sometimes used since it can be readily torn away after the device is installed.
2. When you remove a device from its carrier, ground the hand you are using by any suitable means, for example, with a metallic wristband.
3. Ground the tip of your soldering iron before you solder the device.
4. Never insert the device into a circuit or remove it with the power on.

These precautions apply to both depletion and enhancement-mode IGFETS (MOSFETs).

VMOS and CMOS

Until recently, commercially available FETs were relatively low power devices. For a given power rating, the chip area required to fabricate an FET was considerably larger than a comparable BJT. Consequently, even medium power FETs were very expensive.

Vertical MOS, or VMOS, is a relatively new FET technology that has provided economical high power FETs. The basic structure of the device is illustrated in Figure 7-17. In most applications, the two sources are connected together. In any event, current flow follows a vertical path, rather than a horizontal path as in a conventional enhancement-mode IGFET. Due to the reduced channel length and the fact that the V groove creates two channels, the current density and power handling ability of the device is increased significantly.

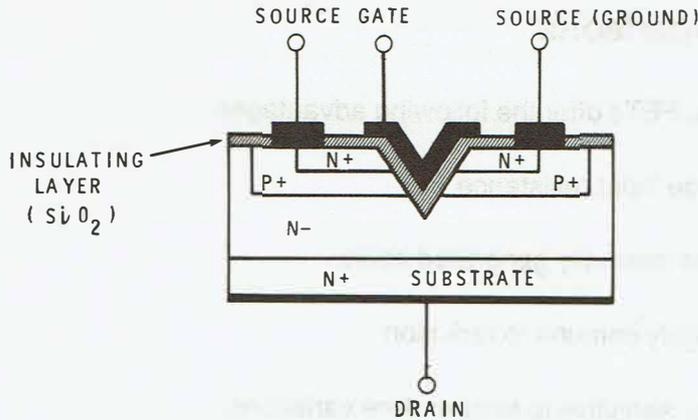


Figure 7-17

Structure of a VMOS FET.

Complementary MOS or CMOS circuits use both P-channel and N-channel enhancement-mode MOSFETs. The principle advantages of CMOS circuits are high noise immunity and low power consumption. These characteristics make CMOS very popular for digital applications.

A CMOS logic inverter is shown in Figure 7-18. Here, the input signal, A , drives the gates of each enhancement-mode MOSFET simultaneously. When the input goes positive, the P-channel MOSFET is cut off and the N-channel MOSFET conducts. In this case, v_O is essentially zero since the voltage across the N-channel MOSFET is essentially zero. Similarly, when the input is low, the P-channel MOSFET turns on and the N-channel MOSFET is cut off. In this instance, the output is connected to $+5V$ through the P-channel MOSFET. Since the on resistance of the conducting MOSFET is small compared to R_L , v_O essentially equals the supply voltage or $5V$ in this example.

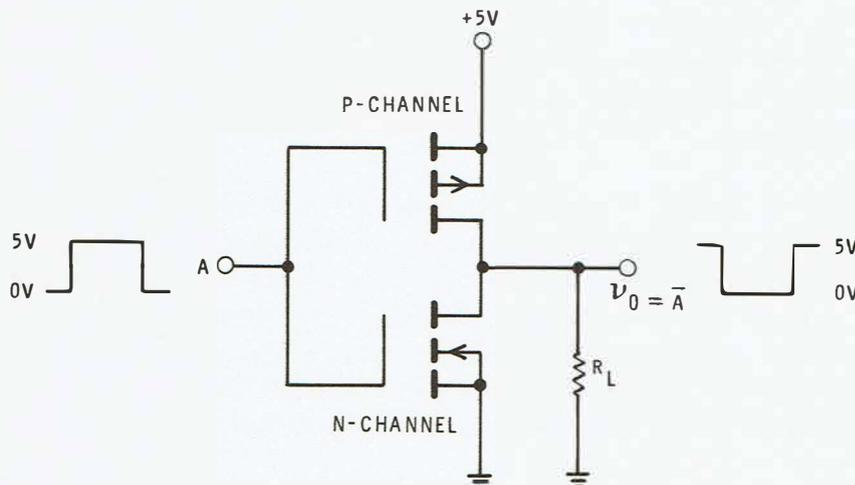


Figure 7-18

A CMOS logic inverter.

FET/BJT Comparisons

Compared to BJTs, FETs offer the following advantages.

1. Large input resistance.
2. Less internally generated noise.
3. Largely immune to radiation.
4. Less sensitive to temperature variations.
5. Easier to fabricate. This makes IGFETs especially suitable for LSI integrated circuits.

Generally speaking, FET circuits provide less voltage gain than comparable BJT circuits. In addition, for a specified output voltage, FET circuits usually require larger supply voltages than BJT circuits. Furthermore, conventional FET large-signal amplifiers exhibit more nonlinear distortion than comparable BJT amplifiers. For these reasons, FETs are not always superior to BJTs. As always, the specific application dictates which device is preferable.

Self-Test Review

1. The value of I_D , when $V_{GS} = 0$ is _____.
2. A JFET can only operate in the _____-mode.
3. A device that can operate in the depletion- or enhancement-mode is the _____-mode IGFET.
4. $I_{DSS} \approx$ _____ for an enhancement-mode IGFET.
5. Another name for an IGFET is a _____.
6. An enhancement-mode MOSFET is an example of a normally-_____ device.
7. A depletion-mode MOSFET is an example of a normally-_____ device.
8. An enhancement-mode IGFET has $V_{GST} = 3V$, $I_{DSS} = 0$, $I_{D(on)} = 10mA$, and $V_{GS(on)} = 5V$. The value of K , therefore is _____.
9. When IGFETs are not installed in a circuit the leads should be shorted together to prevent damage from _____.
10. A depletion-mode IGFET has $V_{GS(off)} = -4V$, and $I_{DSS} = 2.5mA$.
 - (a) $I_D \approx$ _____ when $V_{GS} = 0V$.
 - (b) $I_D \approx$ _____ when $V_{GS} = +2V$.
 - (c) $I_D \approx$ _____ when $V_{GS} = -2V$.

Answers

- | | |
|--------------|--------------------------|
| 1. I_{DSS} | 7. on |
| 2. depletion | 8. 2.5×10^{-3} |
| 3. depletion | 9. electrostatic charges |
| 4. zero | 10. (a) 2.5mA |
| 5. MOSFET | (b) 5.625mA |
| 6. off | (c) 0.625mA |

The solution to questions 8 and 10 follow:

8. $I_D = K(V_{GS} - V_{GS(T)})^2$

Thus:

$$K = \frac{I_D}{(V_{GS} - V_{GS(T)})^2}$$

Since $I_D = I_{D(on)} = 10\text{mA}$, and $V_{GS} = V_{GS(on)} = 5\text{V}$ we have:

$$K = \frac{I_D}{(V_{GS} - V_{GS(T)})^2} = \frac{10\text{mA}}{(5\text{V} - 3\text{V})^2} = 2.5 \times 10^{-3}$$

10. (a) When $V_{GS} = 0$, $I_D = I_{DSS}$ or 2.5mA in this case.

(b) For positive V_{GS} values:

$$I_D = I_{DSS} \left[1 + \frac{|V_{GS}|}{|V_{GS(off)}|} \right]^2$$

Thus, for $V_{GS} = +2\text{V}$:

$$I_D = 2.5\text{mA} \left[1 + \frac{2\text{V}}{4\text{V}} \right]^2 = 2.5\text{mA}(1.5)^2 = 5.625\text{mA}$$

(c) For negative V_{GS} values:

$$I_D = I_{DSS} \left[1 - \frac{|V_{GS}|}{|V_{GS(off)}|} \right]^2$$

Thus, for $V_{GS} = -2\text{V}$:

$$I_D = 2.5\text{mA} \left[1 - \frac{2\text{V}}{4\text{V}} \right]^2 = 2.5\text{mA}(0.5)^2 = 0.625\text{mA}$$

FET CIRCUIT ANALYSIS AND DESIGN

In this portion of the unit we will discuss the analysis and design of selected FET circuits. In discrete circuits, JFETs are used more frequently than IGFETs. For this reason, our discussion will emphasize the analysis and design of several popular JFET circuits.

Small signal FET amplifiers are classified as common-source, common-drain, or common-gate circuits. This system of classification is directly analogous to the BJT common-emitter, common-collector, and common-base circuits discussed previously. Consequently, common-source circuits are widely used as voltage amplifiers. Similarly, common-drain circuits are used as buffers to match impedances. The common-gate circuit is less frequently encountered since, like a common-base BJT circuit, its input resistance is quite small.

JFET Biasing Schemes

A JFET biasing scheme especially useful for small-signal amplifiers is the **self-bias** circuit shown in Figure 7-19. Here, the loop equation for the gate circuit is:

$$V_{GS} - I_S R_S - I_G R_G = 0$$

Due to the JFETs large input resistance, the gate current, I_G , is essentially zero. Consequently, $I_G R_G \approx 0$. Thus:

$$V_{GS} \approx -I_S R_S \quad (\text{Eq. 7-11})$$

Equation 7-11 indicates that the Q point is established by applying the voltage dropped across R_S to the gate. Since an external bias voltage is not required, the term self-bias is used to describe the circuit action.

Frequently, graphical methods are employed for the analysis and design of JFET circuits. The following example serves to introduce the appropriate procedure for a self-bias JFET circuit.

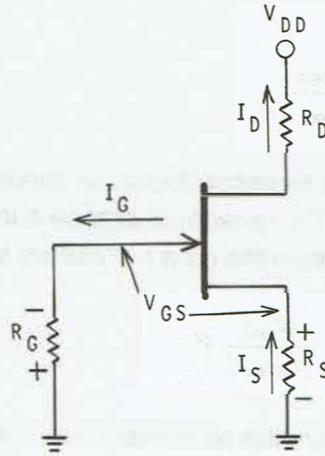


Figure 7-19

Self-bias.

Example 7-6

Calculate the values of I_{DQ} and V_{GSQ} for the circuit shown in Figure 7-20.

Regardless of the value of I_C , in most BJT circuits V_{BE} is approximately 0.7V. In FET circuits, however, V_{GS} varies significantly with changes in I_D . Because of this, the analysis of many JFET circuits requires graphical, or a combination of graphical and analytical, methods.

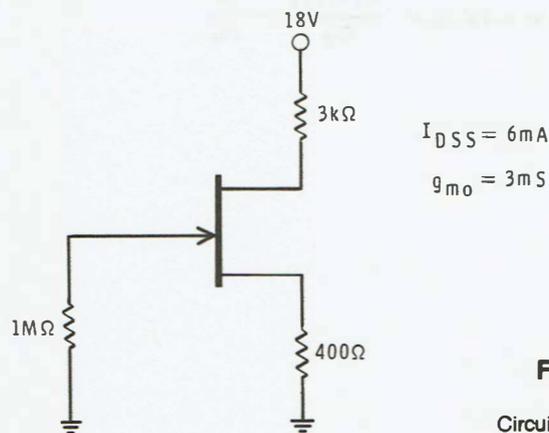


Figure 7-20

Circuit for Example 7-6.

In the case of a self-bias circuit, you can use the following procedure to determine the quiescent values of drain current and gate-to-source voltage.

1. Assuming I_{DSS} and g_{m0} are known, calculate $|V_{GS(off)}|$ from Equation 7-6.

$$|V_{GS(off)}| = \frac{2I_{DSS}}{g_{m0}}$$

2. If the JFET's transconductance curve is available, proceed to step 3. If the JFET's transconductance curve is not available, use Equation 7-3 to obtain the data necessary to plot the curve.

$$I_D = I_{DSS} \left[1 - \frac{|V_{GS}|}{|V_{GS(off)}|} \right]^2$$

Once you have the necessary data, plot the curve.

3. Since $I_G \approx 0$, $I_D \approx I_S$. Therefore, Equation 7-11 is equivalent to:

$$V_{GS} = -I_D R_S$$

The graph of this equation provides the **self-bias curve**. The intersection of the self-bias curve and the transconductance curve indicate the DC operating point. Furthermore, since the graph of Equation 7-11 is a straight line, only two data points are necessary to plot the curve. These points occur when:

$$V_{GS} = 0, I_D = 0.$$

Thus one point on the self-bias curve is the **origin**. And when:

$$V_{GS} = -1V, I_D = \frac{-(-1V)}{R_S} = \frac{1V}{R_S}$$

Thus, a second point, point P, on the self-bias curve is:

$$V_{GS} = -1V, I_D = \frac{1V}{R_S} \quad (\text{Point P})$$

Step 3 consists of plotting the self-bias curve, by drawing a line through point P and the origin.

4. Locate the point corresponding to the intersection of the two curves. This point, point Q, is the DC operating point. Read the values of I_{DQ} and V_{GSQ} .

Applying the procedure to the problem at hand:

1. $|V_{GS(off)}| = \frac{2I_{DSS}}{g_{mo}} = \frac{2(6mA)}{3mS} = 4V$

2. From Equation (7-3), the following data is obtained.

$V_{GS}(V)$	$I_{DSS}[1 - \frac{ V_{GS} }{ V_{GS(off)} }]^2$	$I_D(mA)$
-4	$6mA[1 - \frac{4}{4}]^2 =$	0
-3.5	$6mA[1 - \frac{3.5}{4}]^2 =$	0.094
-3	$6mA[1 - \frac{3}{4}]^2 =$	0.375
-2.5	$6mA[1 - \frac{2.5}{4}]^2 =$	0.844
-2	$6mA[1 - \frac{2}{4}]^2 =$	1.5
-1.5	$6mA[1 - \frac{1.5}{4}]^2 =$	2.34
-1	$6mA[1 - \frac{1}{4}]^2 =$	3.38
-0.5	$6mA[1 - \frac{0.5}{4}]^2 =$	4.6
0	$6mA[1 - \frac{0}{4}]^2 =$	6

By plotting the various V_{GS} , I_D points the transconductance curve shown in Figure 7-21 was obtained.

3. The coordinates of point P are $V_{GS} = -1\text{V}$ and:

$$I_D = \frac{1\text{V}}{R_S} = \frac{1\text{V}}{400\Omega} = 2.5\text{mA}$$

Drawing a line through point P and the origin produces the $R_S = 400\Omega$ bias line shown in Figure 7-21.

4. The intersection of the bias line and the transconductance curve provide a Q point at:

$$I_{DQ} = 3\text{mA}$$

$$V_{GSQ} = -1.2\text{V}$$

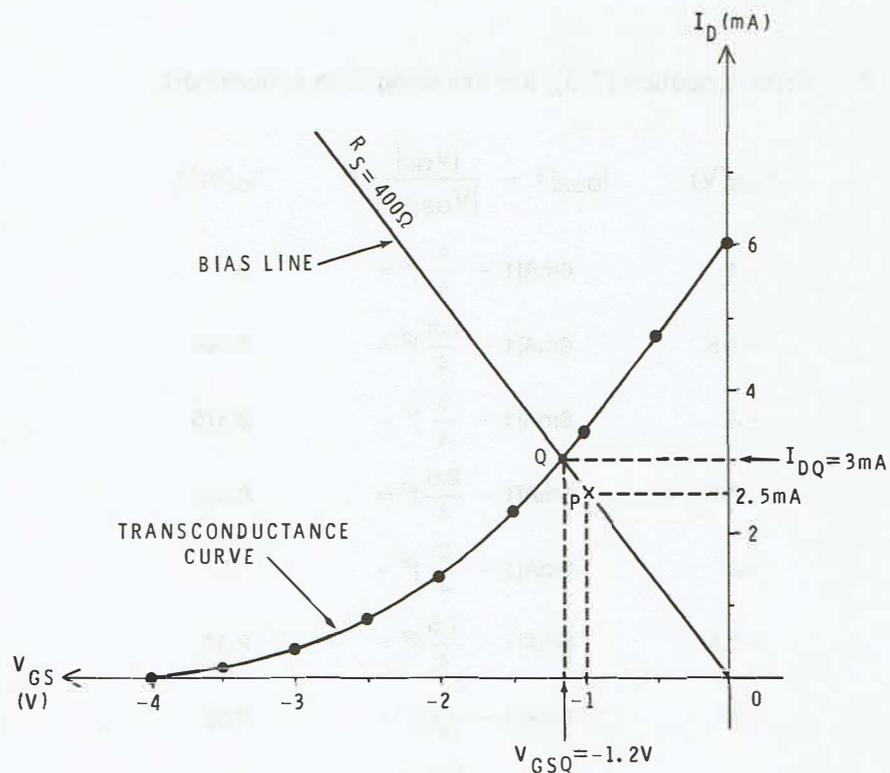


Figure 7-21

Graphical solution for Example 7-6.

Example 7-7

Calculate the terminal-to-ground voltage for the circuit in Figure 7-20. Also calculate values for V_{DSQ} , P_{DQ} , and the approximate transconductance under quiescent conditions.

In BJT circuits, the various DC voltages can be calculated once the value of I_C is known. Similarly, in FET circuits the analogous DC voltages are easily calculated once the value of I_D is known.

Referring to Figure 7-20:

Since $I_G \approx 0$, the voltage drop across the $1M\Omega$ gate resistor is essentially zero. Thus, $V_G = 0$.

$$V_S = I_S R_S$$

$$V_S = 3\text{mA}(400\Omega) = 1.2\text{V}$$

$$V_D = V_{DD} - I_D R_D$$

$$V_D = 18\text{V} - 3\text{mA}(3\text{K}\Omega) = 9\text{V}$$

$$V_{DS} = V_D - V_S$$

$$V_{DS} = 9\text{V} - 1.2\text{V} = 7.8\text{V} = V_{DSQ}$$

$$P_{DQ} = V_{DSQ} I_{DQ}$$

$$P_{DQ} = 7.8\text{V}(3\text{mA}) = 23.4\text{mW}$$

g_{m0} is the value of g_m , when $V_{GS} = 0$.

By employing Equation 7-7, or the normalized curve in Figure 7-9, you can estimate the value of g_m corresponding to any value of V_{GS} between 0 and $V_{GS(\text{off})}$. Thus:

$$g_m = g_{m0} \left[1 - \frac{|V_{GS}|}{|V_{GS(\text{off})}|} \right]$$

$$g_m = 3\text{mS} \left[1 - \frac{1.2\text{V}}{4\text{V}} \right] = 3\text{mS}(0.7) = 2.1\text{mS} = g_{m0}$$

If you prefer, you can calculate g_m from the normalized curve in Figure 7-9 as follows:

$$\frac{V_{GS}}{V_{GS(\text{off})}} = \frac{-1.2\text{V}}{-4\text{V}} = 0.3$$

In Figure 7-9, the value of g_m/g_{m0} corresponding to $V_{GS}/V_{GS(\text{off})} = 0.3$ is 0.7. Thus:

$$g_m = 0.7 g_{m0}$$

$$g_m = 0.7 (3\text{mS}) = 2.1\text{mS} = g_{m0}$$

Voltage Divider Bias

A second JFET biasing scheme is the voltage divider circuit shown in Figure 7-22A. By Thevenizing the voltage divider portion of the circuit, you obtain the equivalent circuit in Figure 7-22B. Here:

$$V_{GG} = V_{TH} = \frac{V_{DD}R_2}{R_1 + R_2} \quad (\text{Eq. 7-12})$$

$$R_G = R_{TH} = R_1 \parallel R_2 \quad (\text{Eq. 7-13})$$

In Figure 7-22B, the loop equation in the gate circuit is:

$$V_{GS} + I_S R_S - V_{GG} + I_G R_G = 0$$

Since $I_G \approx 0$ and $I_D \approx I_S$ we have:

$$V_{GS} = V_{GG} - I_D R_S \quad (\text{Eq. 7-14})$$

Equation 7-14 is the equation of the circuit's bias line. Solving for I_D yields:

$$I_D = \frac{V_{GG} - V_{GS}}{R_S} \quad (\text{Eq. 7-15})$$

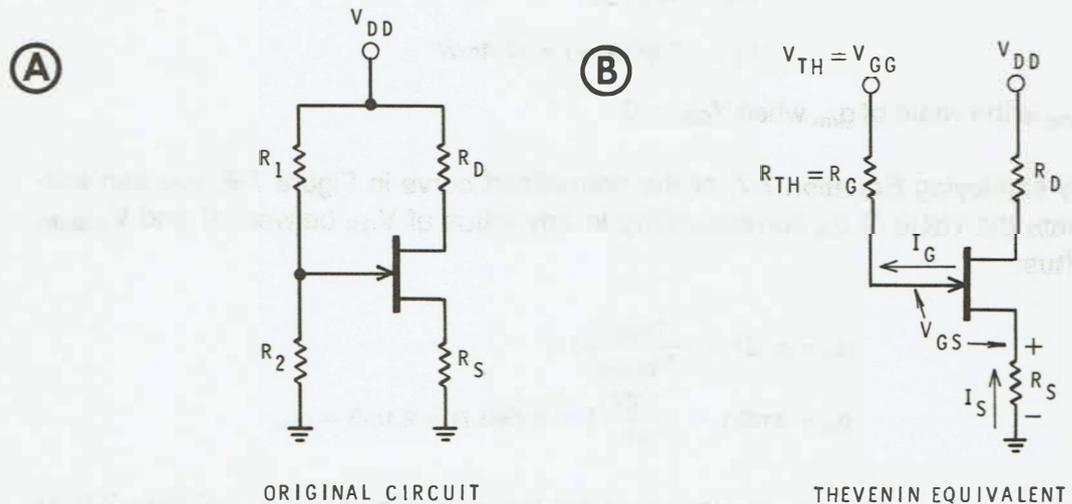


Figure 7-22

Voltage-divider bias.

- A. Original circuit.
- B. Thevenin equivalent.

In a self-bias circuit, I_D varies directly with the value of V_{GS} . Equation 7-15 indicates that with voltage-divider bias, the value of I_D depends upon the value of V_{GS} , and V_{GG} — which is essentially constant. For this reason, the Q point with voltage divider bias is somewhat more stable than with self-bias.

The procedure for analyzing a voltage-divider FET biasing scheme is similar to the one employed for the self-bias circuit. The essential difference is in the construction of the bias line on the JFET's transconductance curve. Specifically, the following procedure can be employed to determine I_{DQ} and V_{GSQ} for the voltage-divider circuit.

1. Calculate $|V_{GS(off)}|$

$$|V_{GS(off)}| = \frac{2I_{DSS}}{g_{mo}}$$

2. Obtain the JFET's transconductance curve from the data sheet or Equation 7-3.

$$I_D = I_{DSS} \left[1 - \frac{|V_{GS}|}{|V_{GS(off)}|} \right]^2$$

3. For the voltage-divider circuit, the equation of the bias line is:

$$V_{GS} = V_{GG} - I_D R_S$$

When $V_{GS} = 0$, $I_D = V_{GG}/R_S$. This defines one point on the bias line, P_1 , as shown in Figure 7-23.

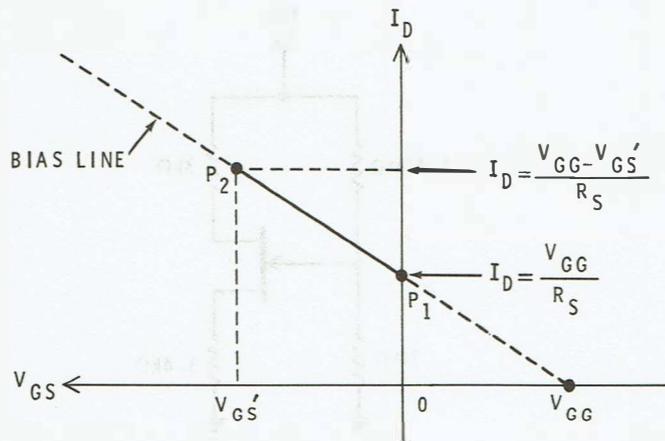


Figure 7-23

Constructing the bias line for the voltage-divider biasing scheme.

By selecting some convenient, non-zero, value of V_{GS} , V_{GS}' , the coordinates of a second point, P_2 , on the bias line can be determined. Specifically, when:

$$V_{GS} = V_{GS}', I_D = \frac{V_{GG} - V_{GS}'}{R_S}$$

For example, if $V_{GS}' = -1V$ is selected, the corresponding value of I_D is:

$$I_D = \frac{V_{GG} - (-1V)}{R_S} = \frac{V_{GG} + 1V}{R_S}$$

As shown in Figure 7-23, the voltage-divider bias line is constructed by drawing a line through points P_1 and P_2 .

- The intersection of the bias line and transconductance curve define the operating point, Q . Thus, once the bias line has been constructed, you simply note the values of I_{DQ} and V_{GSQ} in the same manner as you did with the self-bias circuit.

Example 7-8

The circuit shown in Figure 7-24 uses the JFET of Example 7-6. Thus $I_{DSS} = 6mA$, $g_{mo} = 3mS$, and $V_{GS(off)} = -4V$. Work out values of I_{DQ} , V_{GSQ} , and V_{DSQ} .

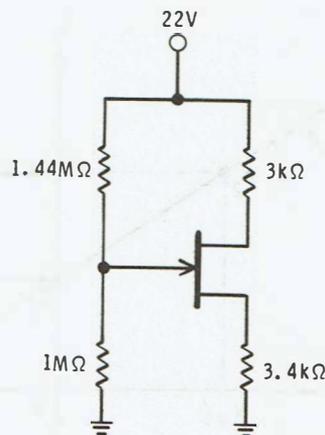


Figure 7-24

Circuit for Example 7-8.

Since the JFET is the same as in Example 7-6, steps 1 and 2 of the analysis are identical to steps 1 and 2 in Example 7-6.

Proceeding to step 3 we have:

$$3. \quad V_{GG} = \frac{V_{DD}R_2}{R_1 + R_2} = \frac{22V(1M\Omega)}{1.44M\Omega + 1M\Omega} = 9V$$

P_1 is located at $V_{GS} = 0$ and:

$$I_D = \frac{V_{GG}}{R_S} = \frac{9V}{3.4k\Omega} = 2.65mA$$

To determine the coordinates of P_2 , we arbitrarily select $V_{GS}' = -1V$. Thus:

$$I_D = \frac{V_{GG} - V_{GS}'}{R_S} = \frac{9V - (-1V)}{3.4k\Omega} = 2.94mA$$

By drawing a line that passes through points P_1 and P_2 , you can obtain the bias line shown in Figure 7-25.

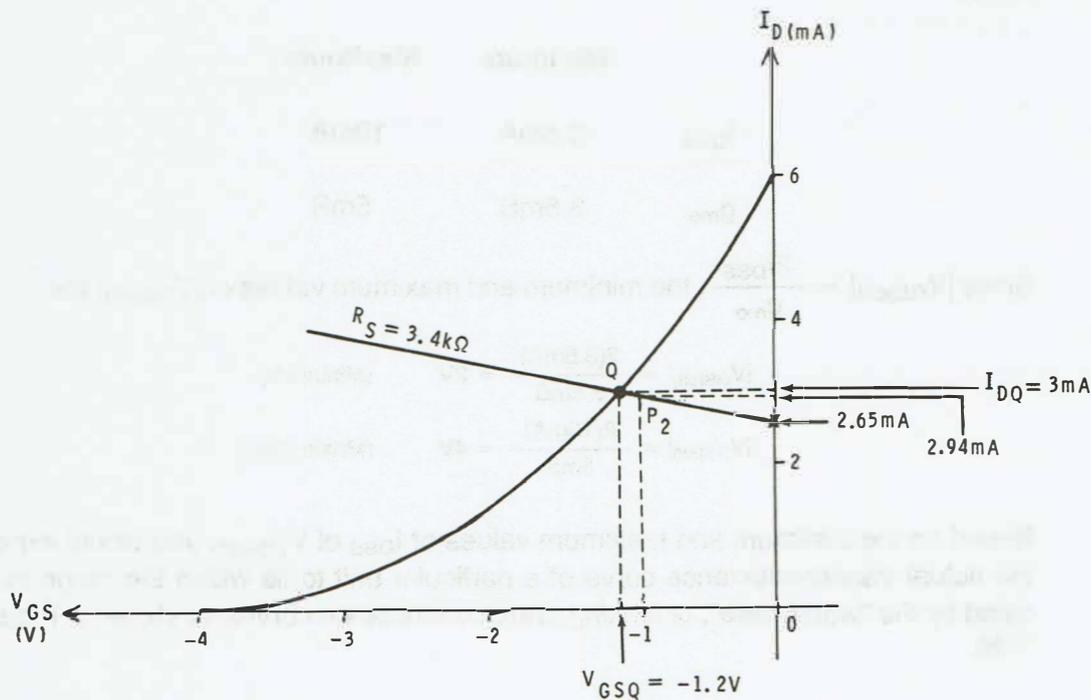


Figure 7-25

Graphical solution for Example 7-8.

4. In Figure 7-25, the intersection of the transconductance curve and bias line provide a Q point at:

$$I_{DQ} = 3\text{mA}$$

$$V_{GSQ} = -1.2\text{V}$$

$$\text{Since } I_{DQ} = 3\text{mA:}$$

$$V_S = I_S R_S = 3\text{mA}(3.4\text{k}\Omega) = 10.2\text{V}$$

$$V_D = V_{DD} - I_D R_D$$

$$V_D = 22\text{V} - 3\text{mA}(3\text{k}\Omega) = 13\text{V}$$

$$V_{DS} = V_D - V_S = 13\text{V} - 10.2\text{V} = 2.8\text{V} = V_{DSQ}$$

Parameter Variations

The basic JFET parameters include I_{DSS} , $V_{GS(off)}$, and g_{mo} . Unfortunately, for a given type JFET, there is considerable unit-to-unit variations in the values of these parameters.

For example, let's assume the data sheet for a certain JFET lists the following values:

	Minimum	Maximum
I_{DSS}	3.5mA	10mA
g_{mo}	3.5mS	5mS

Since $|V_{GS(off)}| = \frac{2I_{DSS}}{g_{mo}}$, the minimum and maximum values of $|V_{GS(off)}|$ are:

$$|V_{GS(off)}| = \frac{2(3.5\text{mA})}{3.5\text{mS}} = 2\text{V} \quad (\text{Minimum})$$

$$|V_{GS(off)}| = \frac{2(10\text{mA})}{5\text{mS}} = 4\text{V} \quad (\text{Maximum})$$

Based on the minimum and maximum values of I_{DSS} of $V_{GS(off)}$, you would expect the actual transconductance curve of a particular unit to lie within the range indicated by the "worst-case", or limiting, transconductance curves as shown in Figure 7-26.

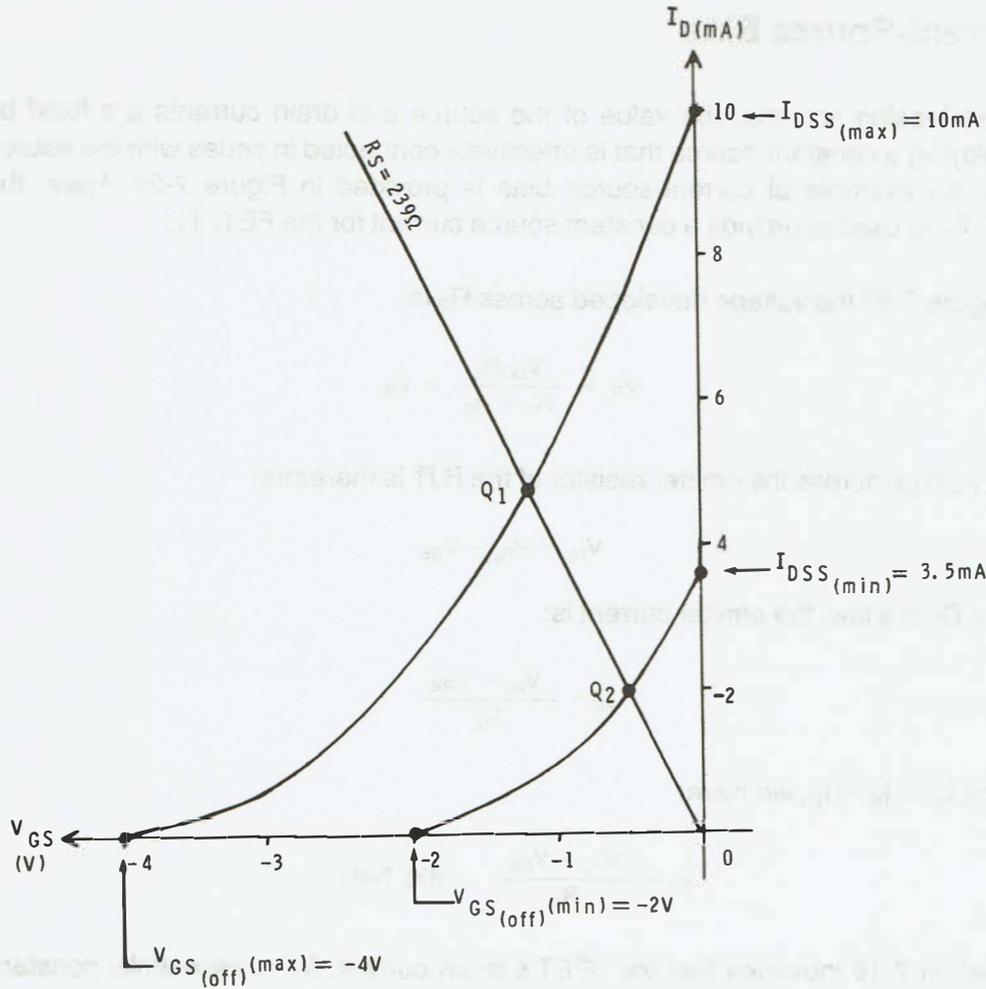


Figure 7-26

Parameter variations.

The indicated parameter variations result in an actual operating point that is between the limits established by Q₁ and Q₂.

For purposes of comparison, a 239Ω self-bias line has been included in Figure 7-26. Note that, if a particular unit has I_{DSS} and V_{GS(off)} values that are maximum, the operating point, Q, is:

$$I_{DQ} \approx 4.75\text{mA} \quad Q_1$$

$$V_{GSQ} \approx -1.2\text{V}$$

Similarly, if a particular unit has I_{DSS} and V_{GS(off)} values that are minimum, the operating point, Q, is:

$$I_{DQ} \approx 2\text{mA} \quad Q_2$$

$$V_{GSQ} \approx -0.5\text{V}$$

In some applications, the spread in I_{DQ} values illustrated by the preceding example are unacceptable. For such applications, a third type of biasing scheme, called current-source bias, is often employed.

Current-Source Bias

In this biasing scheme, the value of the source and drain currents are fixed by employing a constant-source that is effectively connected in series with the source lead. An example of current-source bias is provided in Figure 7-27. Here, the BJT, T_2 , is used to provide a constant source current for the FET, T_1 .

In Figure 7-27 the voltage developed across R_2 is:

$$V_{R_2} = \frac{V_{DD}R_2}{R_1 + R_2} = V_B$$

The voltage across the emitter resistor of the BJT is therefore:

$$V_{R_E} = V_{R_2} - V_{BE}$$

From Ohm's law, the emitter current is:

$$I_E = \frac{V_{R_2} - V_{BE}}{R_E}$$

Since $I_E = I_S \approx I_D$, we have:

$$I_D = \frac{V_{R_2} - V_{BE}}{R_E} \quad (\text{Eq. 7-16})$$

Equation 7-16 indicates that the JFET's drain current, I_D , is essentially constant, and therefore independent of variations in the JFET's parameters.

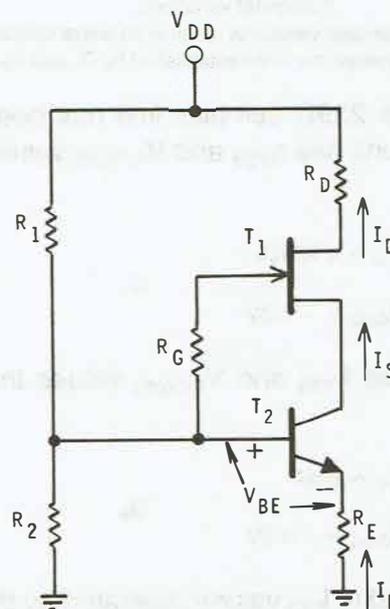


Figure 7-27

Current-source bias.

Example 7-9

Calculate the quiescent drain current for the circuit shown in Figure 7-28.

$$V_{R_2} = \frac{V_{DD}R_2}{R_1 + R_2} = \frac{40V(33k\Omega)}{100k\Omega + 33k\Omega} = 9.92V$$

$$I_D = I_E = \frac{V_{R_2} - V_{BE}}{R_E} = \frac{9.92V - 0.7V}{4.7k\Omega} = 1.96mA$$

To see how variations in I_{DSS} and $V_{GS(off)}$ affect the operation of a current-source bias circuit, let's assume the JFET in Figure 7-28 has the following specifications.

$$3.5mA \leq I_{DSS} \leq 10mA$$

$$2V \leq |V_{GS(off)}| \leq 4V$$

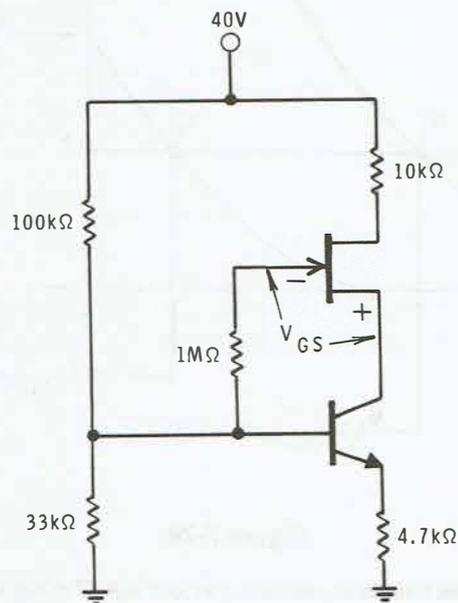


Figure 7-28

Circuit for Example 7-9.

Furthermore, let's assume the JFET's worst case transconductance curves are available, and appear as shown in Figure 7-29.

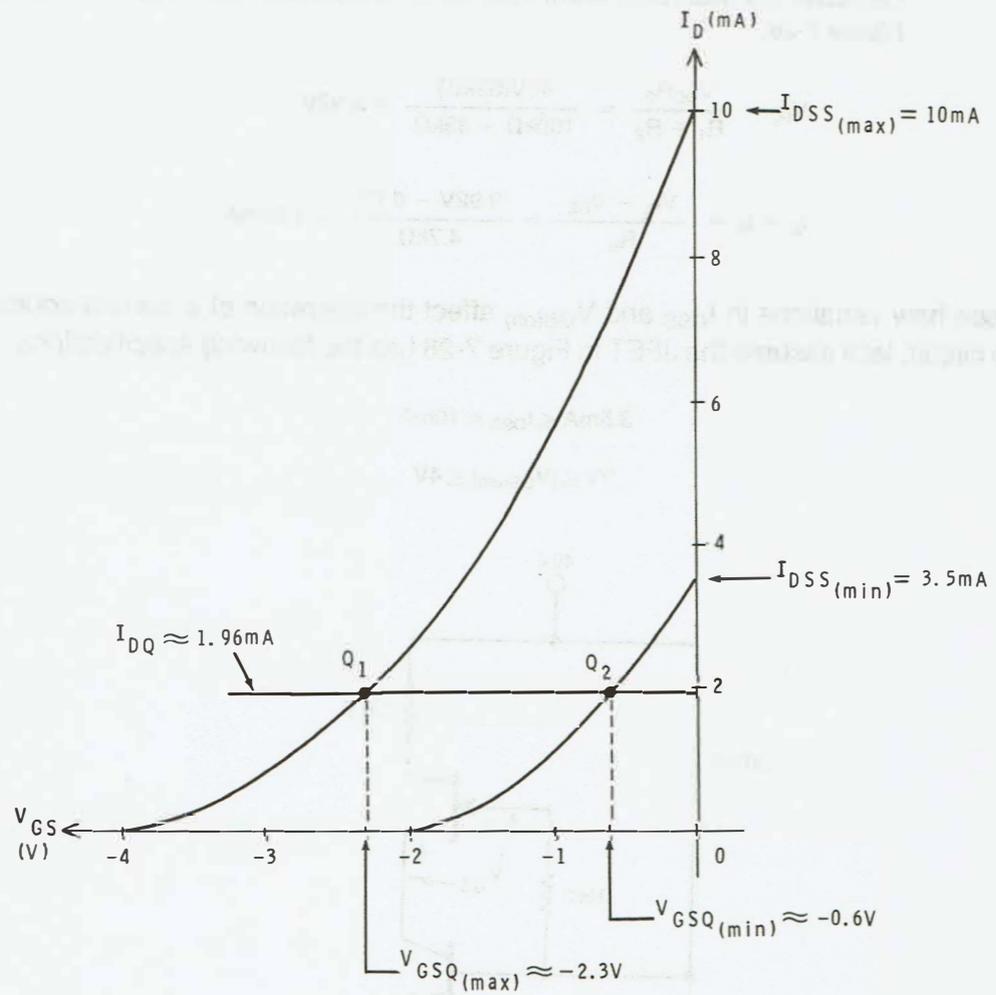


Figure 7-29

Worst case transconductance curves for the JFET in Figure 7-28.

Referring to Figure 7-28 and Figure 7-29, the following points should be noted.

1. Since the BJT acts like a constant current source, $I_{DQ} \approx I_E$, or 1.96mA in this case.
2. For the minimum curve, an I_{DQ} of 1.96mA results in $V_{GSQ} = -0.6V$. Similarly, for the maximum curve, an I_{DQ} of 1.96mA produces a V_{GSQ} of $-2.3V$.
3. To ensure that the gate is reverse biased, component values must be selected so that $I_{DQ} < I_{DSS(MIN)}$.

Based on the previous observations, it is clear that current-source bias stabilizes I_{DQ} against large variations in the JFET's parameters. However, for a given JFET, the value of V_{GSQ} depends upon the specific values of I_{DSS} and $V_{GS(off)}$, since these parameters determine the endpoints of the actual transconductance curve.

Example 7-10

In Figure 7-28, the JFET has the following specifications:

$$I_{DSS(MIN)} = 3.5\text{mA} \quad |V_{GS(off)(MIN)}| = 2V$$

$$I_{DSS(MAX)} = 10\text{mA} \quad |V_{GS(off)(MAX)}| = 4V$$

- Calculate the average I_{DSS} and $|V_{GS(off)}|$ values for a typical JFET.*
- Using the values obtained in (a), estimate the value of V_{GSQ} .*
- Based on the value of V_{GSQ} obtained in (b), calculate the various terminal-to-ground voltages. Also calculate the value of V_{DSQ} and V_{CEQ} .*

$$(a) \quad I_{DSS(ave)} = \frac{I_{DSS(MIN)} + I_{DSS(MAX)}}{2}$$

$$I_{DSS(ave)} = \frac{3.5\text{mA} + 10\text{mA}}{2} = 6.75\text{mA}$$

$$|V_{GS(off)(ave)}| = \frac{|V_{GS(off)(MIN)}| + |V_{GS(off)(MAX)}|}{2}$$

$$|V_{GS(off)(ave)}| = \frac{2V + 4V}{2} = 3V$$

$$(b) \quad \frac{I_D}{I_{DSS}} = \frac{1.96\text{mA}}{6.75\text{mA}} = 0.29$$

Referring to Figure 7-8, you find that an I_D/I_{DSS} ratio of 0.29 corresponds to a $V_{GS}/V_{GS(off)}$ ratio of approximately 0.46. Thus, in Figure 7-30:

$$V_{GS} = 0.46V_{GS(off)}$$

$$V_{GS} = 0.46(-3\text{V}) = -1.38\text{V} = V_{GSQ}$$

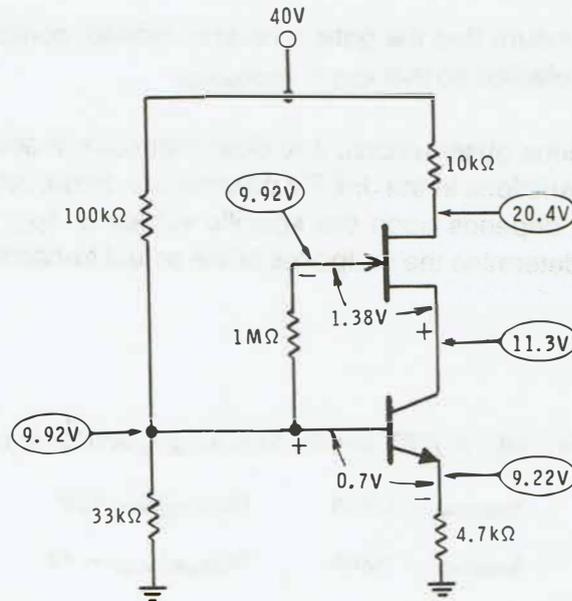


Figure 7-30

Approximate terminal-to-ground voltages for Example 7-10.

$$(c) \quad V_B = V_{R_2} = \frac{V_{DD}R_2}{R_1 + R_2} = \frac{40V(33k\Omega)}{100k\Omega + 33k\Omega} = 9.92V$$

$$V_E = V_B - V_{BE} = 9.92V - 0.7V = 9.22V$$

Since $I_G \approx 0$, the voltage drop across the $1M\Omega$ gate resistor is approximately 0V. Thus:

$$V_G = V_B = 9.92V$$

Since the collector and source leads are connected together, $V_C = V_S$. Therefore:

$$\begin{aligned} V_S &= V_{GS} + V_{RG} + V_{R_2} \\ V_S &= 1.38V + 0 + 9.92V \\ V_S &= 11.3V = V_C \end{aligned}$$

$$\begin{aligned} V_D &= V_{DD} = I_D R_D \\ V_D &= 40V - 1.96mA(10k\Omega) = 20.4V \end{aligned}$$

$$\begin{aligned} V_{DS} &= V_{DS} - V_S \\ V_{DS} &= 20.4V - 11.3V = 9.1V = V_{DSQ} \end{aligned}$$

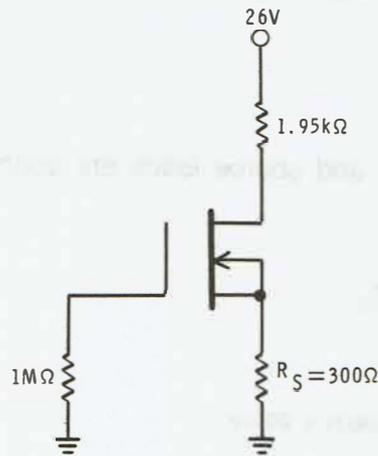
$$\begin{aligned} V_{CE} &= V_C - V_E \\ V_{CE} &= 11.3V - 9.22V = 2.08V = V_{CEQ} \end{aligned}$$

Biasing MOSFETs

For negative values of V_{GS} , the operation of an N-channel depletion-mode MOSFET is essentially the same as the operation of an N-channel JFET. Therefore, the JFET biasing schemes discussed previously can be used with depletion-mode MOSFETs, assuming the MOSFET operates in the depletion region.

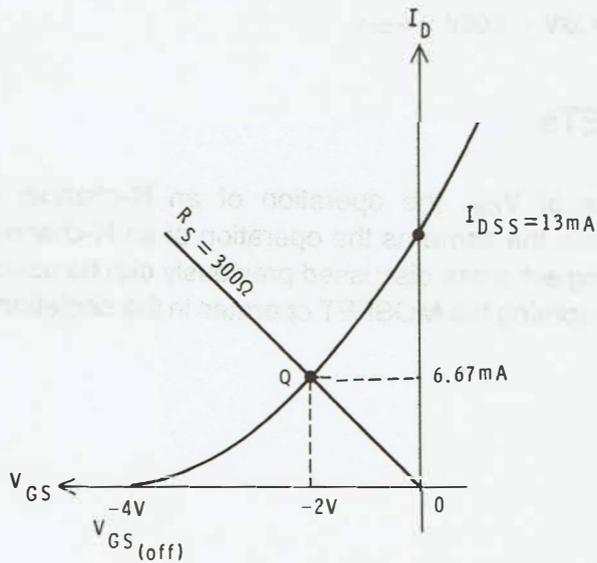
As an example, consider the self-bias circuit shown in Figure 7-31A. To determine the values of I_{DQ} and V_{GSQ} , an $R_S = 300\Omega$ self-bias line is constructed as shown in Figure 7-31B. Obviously, the intersection of the self-bias line and transconductance curve provide the desired Q-point values.

(A)



CIRCUIT

(B)



TRANSCONDUCTANCE CURVE AND 300Ω BIAS LINE

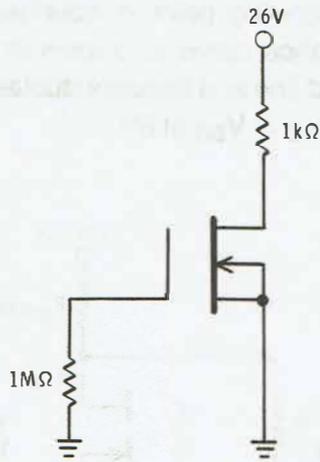
Figure 7-31

Self-bias of a depletion-mode MOSFET.

- A. Circuit.
- B. Transconductance curve and 300Ω bias line.

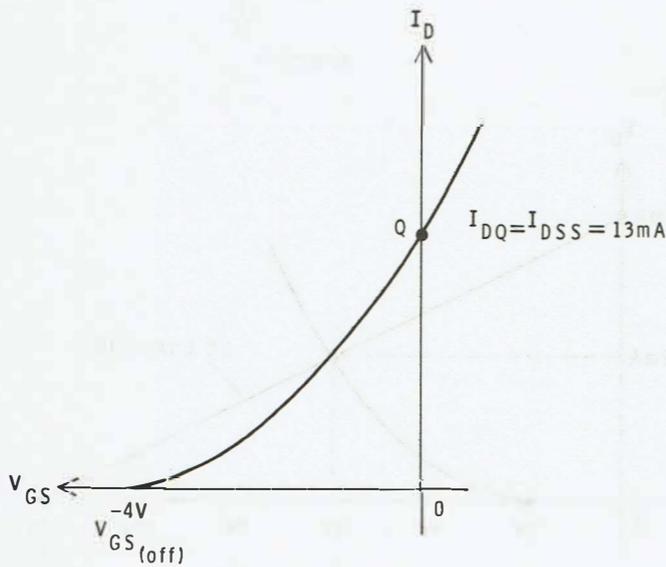
A special case of self-bias, called **zero bias**, occurs when $V_{GS} = 0$, as shown in Figure 7-32. Here, $V_S = 0$, $R_S = 0$, $V_G = 0$, and $I_G \approx 0$. For this reason, V_{GS} also equals 0. As you know, $I_D = I_{DSS}$ when $V_{GS} = 0$. Hence, the operating point appears as shown in Figure 7-32B. Zero bias is a popular biasing scheme for depletion-mode MOSFETs due to its inherent simplicity. Unfortunately, zero bias cannot be used with JFETs or enhancement-mode MOSFETs.

(A)



CIRCUIT

(B)



TRANSCONDUCTANCE CURVE

Figure 7-32

Zero-bias of a depletion-mode MOSFET.

- A. Circuit.
- B. Transconductance curve.

A popular biasing scheme for enhancement-mode MOSFETs is shown in the **drain feedback** circuit shown in Figure 7-33A. Here, $V_{DS} = V_{GS}$, since the voltage drop across R_G is essentially zero. In Figure 7-33A, the drain-to-source voltage, V_{DS} , is:

$$V_{DS} = V_{DD} - I_D R_D$$

When $V_{DS} = 0$, $I_D = I_{D(sat)} = V_{DD}/R_D$. Similarly, when $I_D = 0$, $V_{DS} = V_{DS(cut)} = V_{DD}$. The circuit's operating point is obtained by constructing the DC load line on the transconductance curve as shown in Figure 7-33B. In this case, the intersection of the DC load line and transconductance curve establish an operating point at $I_{DQ} = 2\text{mA}$ and $V_{GS} = V_{DQ}$ at 6V.

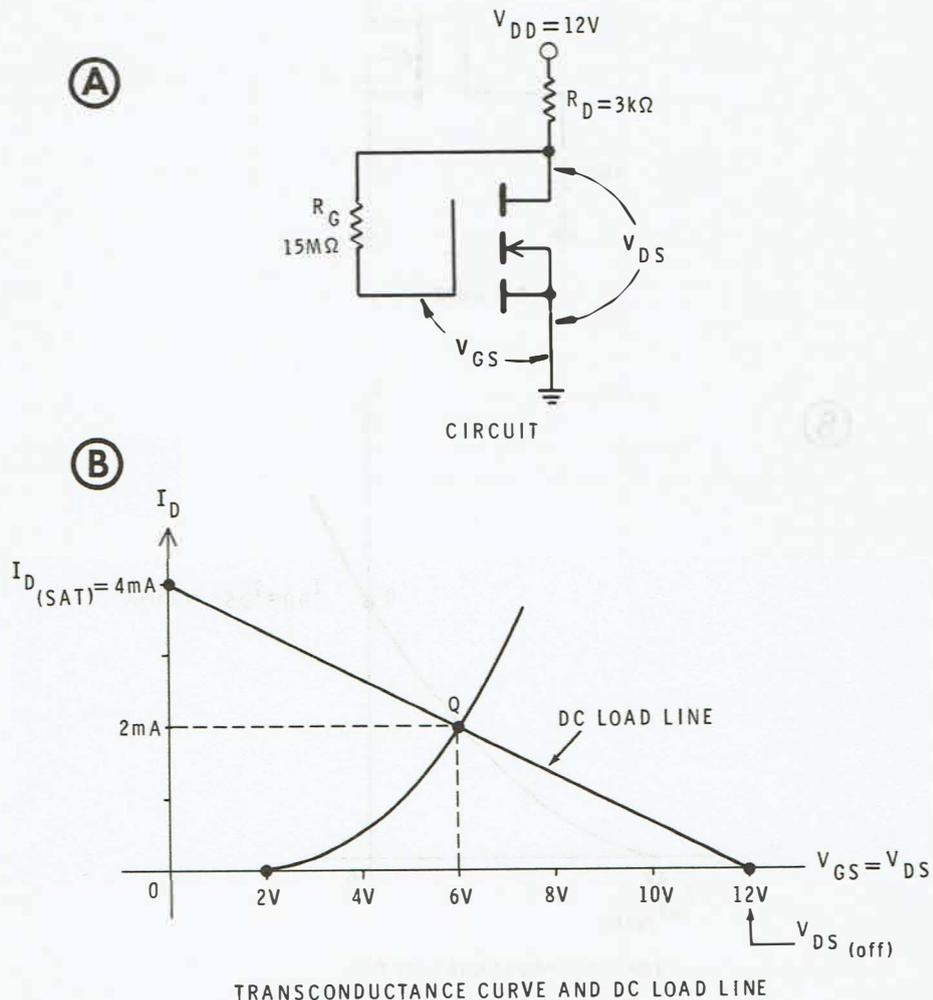


Figure 7-33

Drain-feedback bias of an enhancement-mode MOSFET.

- A. Circuit.
- B. Transconductance curve and DC load line.

Common-Source Voltage Amplifiers

An examination of transconductance and drain curves suggests the small-signal JFET model shown in Figure 7-34. Here, r_g represents the input resistance looking into the gate-source terminals of the JFET. Similarly, r_d represents the output resistance between the drain and source terminals. Typically, $r_g \geq 100\text{M}\Omega$. For this reason, we will assume r_g acts like an open circuit. The reciprocal of g_{os} , given on the JFET's data sheet, provides the approximate value of r_d . Typically, $r_d \geq 100\text{k}\Omega$. Consequently, r_d can also be assumed to approximate an open circuit when $r_d \gg R_D$. As a guide, we will neglect r_d when R_D is equal to or less than $10\text{k}\Omega$.

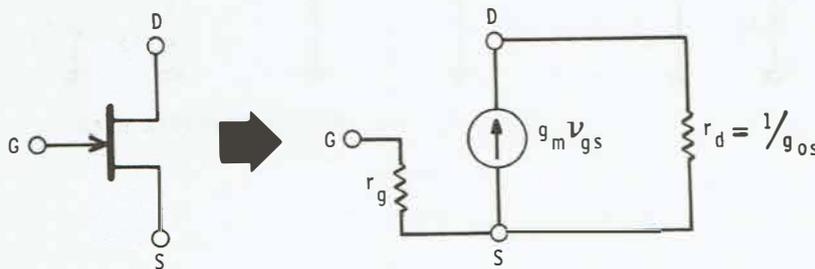


Figure 7-34

Small-signal JFET model.
In most circuits, r_g and r_d are approximated by open circuits.

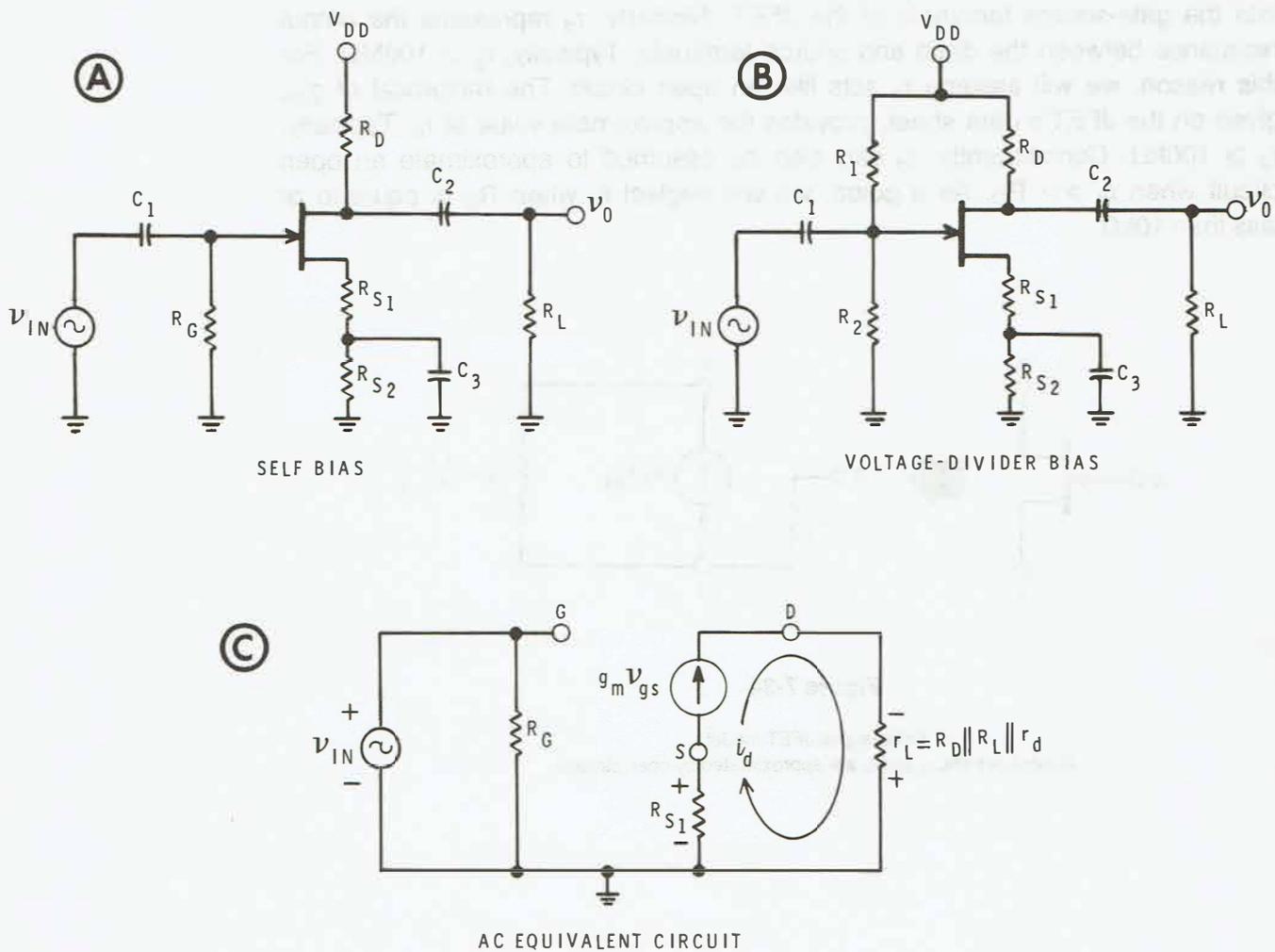


Figure 7-35

Common-source voltage amplifiers.

- A. Self-bias.
- B. Voltage-divider bias.
- C. AC equivalent circuit.

By adding coupling and bypass capacitors to the self-bias and voltage-divider bias circuits, you obtain the common-source amplifiers shown in Figure 7-35A and Figure 7-35B respectively. The AC equivalent circuit in Figure 7-35C is obtained by reducing V_{DD} to zero, shorting the coupling and bypass capacitors, and replacing the JFET with its small-signal model.

With reference to Figure 7-35C, a number of useful expressions can be derived as follows:

By inspection $v_o = -i_d r_L$. Since $i_d = g_m v_{gs}$, we have:

$$v_o = -g_m v_{gs} r_L \quad (1)$$

Starting at the gate terminal, G, and selecting a counterclockwise path we note that:

$$\begin{aligned} v_{gs} &= v_{IN} - i_d R_{S_1} \\ v_{gs} &= v_{IN} - g_m v_{gs} R_{S_1} \end{aligned} \quad (2)$$

Solving (2) for v_{IN} yields:

$$\begin{aligned} v_{IN} &= v_{gs} + g_m v_{gs} R_{S_1} \\ v_{IN} &= v_{gs}(1 + g_m R_{S_1}) \end{aligned} \quad (3)$$

By definition, $A_V = v_o/v_{IN}$. Thus, dividing equation (1) by equation (3) yields:

$$A_V = \frac{-g_m v_{gs} r_L}{v_{gs}(1 + g_m R_{S_1})} = - \frac{g_m r_L}{1 + g_m R_{S_1}}$$

Dividing numerator and denominator by g_m .

$$A_V = - \frac{r_L}{R_{S_1} + \frac{1}{g_m}}$$

Finally, defining the term $1/g_m$ to be r_s' we have:

$$A_V = \frac{-r_L}{R_{S_i} + r_s'} \quad (\text{Eq. 7-17})$$

Where: $r_s' = 1/g_m$

Equation 7-17 is in a form that is very similar to the formula derived in Unit 3 for the voltage gain of a BJT common-emitter amplifier. Specifically:

Common-Source Amplifiers

Common-Emitter Amplifiers

$$A_V = \frac{-r_L}{R_{S_i} + r_s'}$$

$$A_V = \frac{-r_L}{R_{E_i} + r_e'}$$

As you can see, R_{S_i} replaces R_{E_i} , and r_s' replaces r_e' . In each case, the negative sign simply indicates that the output voltage is 180° out of phase with the input voltage.

If the source resistor is fully bypassed, $R_{S_i} = 0$. For this special case, Equation 7-17 reduces to:

$$A_V = \frac{-r_L}{r_s'} = -g_m r_L \quad (\text{Eq. 7-18})$$

Equation 7-18 is analogous to the BJT formula:

$$A_V = \frac{-r_L}{r_e'}$$

In Figure 7-35C, the input resistance seen by the signal source equals R_G . Naturally, in the voltage-divider circuit, $R_G = R_1 \parallel R_2$. Thus:

$$R_{IN} = R_G \quad (\text{Eq. 7-19})$$

The output resistance is described by:

$$R_O = R_D \parallel r_d \quad (\text{Eq. 7-20})$$

Where: $r_d = 1/g_{os}$

In many circuits $r_d \gg R_D$, consequently, $R_O \approx R_D$.

Example 7-11

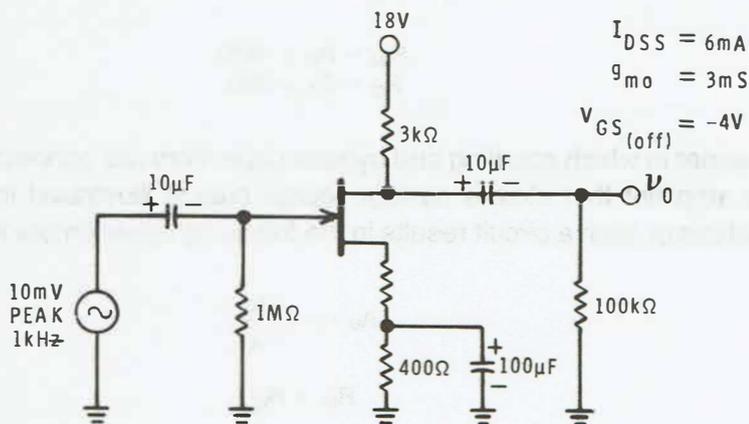
A DC analysis of the amplifier in Figure 7-36 was provided in Example 7-6. Recall that $I_{DQ} = 3\text{mA}$ and $V_{GSQ} = -1.2\text{V}$. Assuming $r_d \gg 3\text{k}\Omega$, calculate the peak output voltage. Also estimate the input and output resistance of the amplifier.

$$r_L = R_D \parallel R_L$$

$$r_L = 3\text{k}\Omega \parallel 100\text{k}\Omega = 2.91\text{k}\Omega$$

In order to calculate the voltage gain, the value of g_m at $I_D = I_{DQ}$ must first be determined. Since $V_{GS} = -1.2\text{V}$ and $V_{GS(\text{off})} = -4\text{V}$, the ratio of $V_{GS}/V_{GS(\text{off})}$ is:

$$\frac{V_{GS}}{V_{GS(\text{off})}} = \frac{-1.2\text{V}}{-4\text{V}} = 0.3$$

**Figure 7-36**

Circuit for Example 7-11.

Referring to Figure 7-9, note that a $V_{GS}/V_{GS(off)}$ ratio of 0.3 corresponds to a g_m/g_{m0} ratio of approximately, 0.7. Thus:

$$g_m = 0.7g_{m0} = 0.7(3\text{mS}) = 2.1\text{mS}$$

Now:

$$r_{s'} = \frac{1}{g_m} = \frac{1}{2.1\text{mS}} = 476.2\Omega$$

$$A_V = \frac{-r_L}{r_{s'}} = -\frac{2.91\text{k}\Omega}{476.2\Omega} = -6.11$$

Since $v_{iN} = 10\text{mV}$ peak, the magnitude of the peak output voltage is:

$$v_o = 6.11(10\text{mV}) = 61.1\text{mV peak}$$

And:

$$R_{iN} = R_G = 1\text{M}\Omega$$

$$R_o = R_D = 3\text{k}\Omega$$

The manner in which coupling and bypass capacitors are connected to a common-source amplifier that utilizes current-source bias is illustrated in Figure 7-37. An AC analysis of such a circuit results in the following approximate formulas:

$$A_V = -\frac{r_L}{r_{s'}}$$

$$R_{iN} = R_G$$

$$R_o = R_D || r_d \approx R_D$$

The following example illustrates how to analyze the amplifier in Figure 7-37.

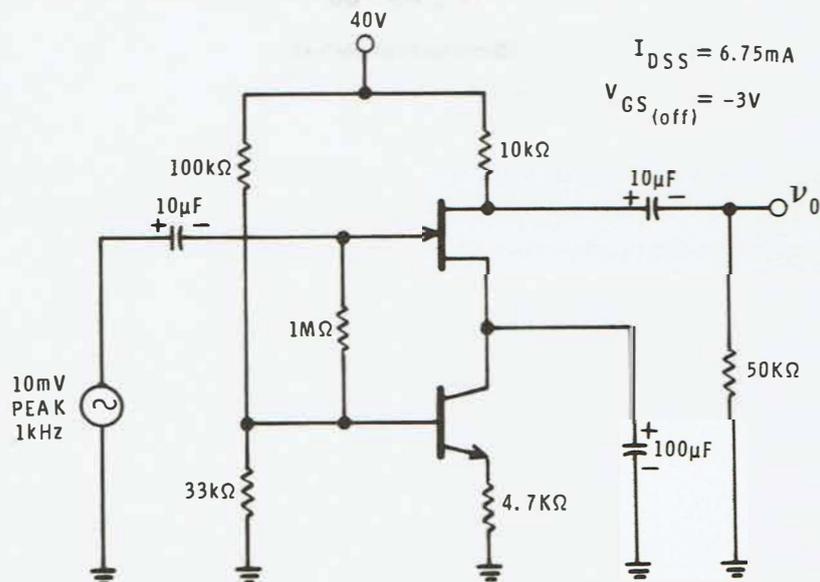


Figure 7-37

Circuit for Example 7-12.

Example 7-12

A DC analysis of the amplifier in Figure 7-37 was provided in Example 7-10. Recall that $I_{DQ} = 1.96\text{mA}$ and $V_{GSQ} = -1.38\text{V}$. Also, recall that “average values” were used in the calculations due to the large unit-to-unit parameter variations. Using the given information, estimate the expected voltage gain of the circuit. For simplicity, assume r_d is large enough to neglect.

$$r_L = 10\text{k}\Omega \parallel 50\text{k}\Omega = 8.33\text{k}\Omega$$

The average values of I_{DSS} and $V_{GS(\text{off})}$ are 6.75mA and -3V respectively. Consequently, the average g_{m0} is:

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(\text{off})}|} = \frac{2(6.75\text{mA})}{3\text{V}} = 4.5\text{mS}$$

For the known bias conditions, the approximate value of g_m is obtained as follows:

$$\frac{V_{GS}}{V_{GS(\text{off})}} = \frac{-1.38\text{V}}{-3\text{V}} = 0.46$$

Referring to Figure 7-9, the value of g_m/g_{m0} corresponding to $V_{GS}/V_{GS(\text{off})} = 0.46$ is approximately 0.54. Thus:

$$\begin{aligned} g_m &= 0.54g_{m0} \\ g_m &= 0.54(4.5\text{mS}) = 2.43\text{mS} \end{aligned}$$

$$r_s' = \frac{1}{g_m} = \frac{1}{2.43\text{mS}} = 411.5\Omega$$

$$A_v = \frac{-r_L}{r_s'} = -\frac{8.33\text{k}\Omega}{411.5\Omega} = -20.2$$

Common-Drain Amplifiers

The common-drain amplifier is the FET counterpart of the BJT common-collector amplifier. Whereas common-collector amplifiers are referred to as emitter-followers, common-drain amplifiers are called source-followers.

Two typical source-follower circuits are illustrated in Figure 7-38. Note that $R_D = 0$, and that the output is taken from the source terminal. As you might suppose, source-followers have voltage gains less than 1, large values of R_{IN} , and small values of R_O . The following equations can be used to analyze typical source-follower circuits:

$$A_V = \frac{r_L}{r_L + r_{S'}} \quad (\text{Eq. 7-21})$$

Where: $r_L = R_S \parallel R_L$
 $r_{S'} = \frac{1}{g_m}$

$$R_{IN} = R_G \quad (\text{Eq. 7-22})$$

And:

$$R_O \approx R_S \parallel r_{S'} \quad (\text{Eq. 7-23})$$

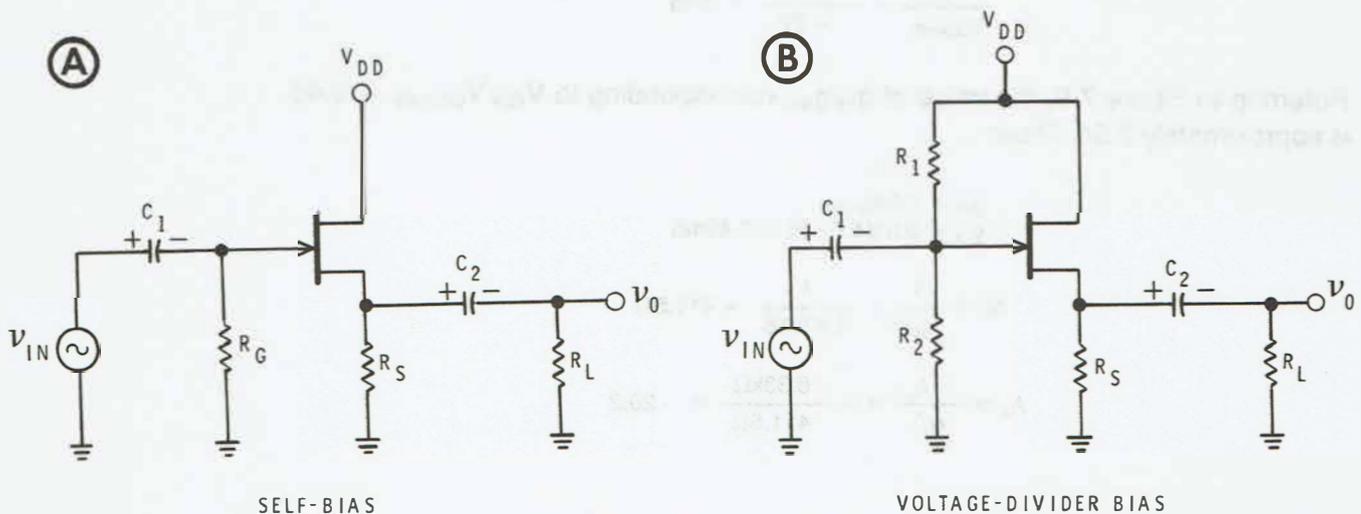
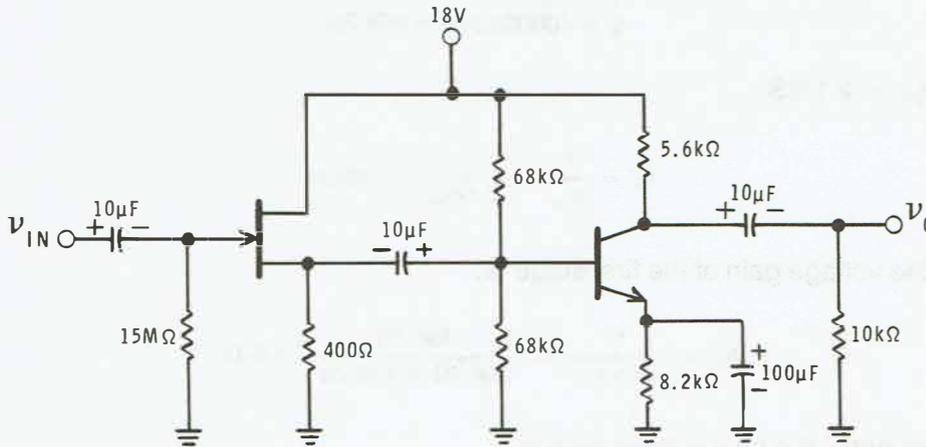


Figure 7-38

Typical common-drain, source-follower circuits.

Example 7-13

Figure 7-39 illustrates a two-stage amplifier that utilizes an FET "front end" to obtain a large input resistance. The first stage is a modified version of the circuit analyzed in Example 7-6. You can assume $I_{DQ} = 3\text{mA}$ and $g_m = 2.1\text{mS}$ for the first stage. Assuming that h_{fe} for the second stage is 100, estimate the voltage gain, input resistance, and output resistance of the two-stage amplifier.

**Figure 7-39**

Circuit for Example 7-13.

Starting with the second stage:

$$V_B = \frac{18\text{V}(68\text{k}\Omega)}{68\text{k}\Omega + 68\text{k}\Omega} = 9\text{V}$$

$$V_E = 9\text{V} - 0.7\text{V} = 8.3\text{V}$$

$$I_E = \frac{V_E}{R_E} = \frac{8.3\text{V}}{8.2\text{k}\Omega} = 1.01\text{mA}$$

$$r_e' = \frac{37\text{mV}}{I_E} = \frac{37\text{mV}}{1.01\text{mA}} = 36.6\Omega$$

$$r_L = 5.6\text{k}\Omega \parallel 10\text{k}\Omega = 3.59\text{k}\Omega$$

$$A_{v_2} = \frac{-r_L}{r_e'} = -\frac{3.59\text{k}\Omega}{36.6\Omega} = -98.1$$

The input resistance of the second stage is:

$$\begin{aligned} R_{iN} &= R_1 \parallel R_2 \parallel h_{re}(r_e') \\ R_{iN} &= 68\text{k}\Omega \parallel 68\text{k}\Omega \parallel 100(36.6\Omega) \\ R_{iN} &= 34\text{k}\Omega \parallel 3.66\text{k}\Omega \\ R_{iN} &= 3.3\text{k}\Omega \end{aligned}$$

The input resistance of the second stage is the effective load resistance of the first stage. Thus:

$$\begin{aligned} r_L &= R_S \parallel R_L \\ r_L &= 400\Omega \parallel 3.3\text{k}\Omega = 356.7\Omega \end{aligned}$$

Since $g_m = 2.1\text{mS}$:

$$r_{s'} = \frac{1}{g_m} = \frac{1}{2.1\text{mS}} = 476.2\Omega$$

Thus, the voltage gain of the first stage is:

$$A_{v_1} = \frac{r_L}{r_L + r_{s'}} = \frac{356.7\Omega}{356.7\Omega + 476.2\Omega} = 0.43$$

Consequently, the total voltage gain is:

$$\begin{aligned} A_{v_T} &= A_{v_1} A_{v_2} \\ A_{v_T} &= (0.43)(-98.1) = -42.2 \end{aligned}$$

By inspection, $R_{iN} = R_G = 15\text{M}\Omega$. Similarly, $R_O = R_C$ or $5.6\text{k}\Omega$.

Design Considerations

A combination of graphical and analytical methods are normally employed for the design of JFET circuits. Ideally, graphs of I_D vs V_{GS} , g_m vs V_{GS} , and I_D vs V_D are available for the particular JFET used in the circuit.

Unfortunately, JFET data sheets do not always supply all the desired information for a given JFET. In addition, since most readers probably do not have an extensive library of JFET data sheets, we will employ simplified design procedures that are suitable when approximate results are acceptable.

The initial step in the design process consists of selecting a suitable value for I_{DQ} . Values of I_{DQ} that approach the value of I_{DSS} impose severe limitations on the available output voltage. Similarly, values of I_{DQ} considerably less than I_{DSS} result in an operating point on the curved portion of the transconductance curve. In this case, even modest input signals result in an excessive amount of nonlinear distortion in the output signal. For these reasons, a compromise value of I_{DQ} is required. This value is usually between 40% and 60% of I_{DSS} .

Let's assume I_{DQ} is chosen so that $I_D/I_{DSS} = 0.6$. Referring to Figure 7-8, we find that an I_D/I_{DSS} ratio of 0.6 corresponds to a $V_{GS}/V_{GS(off)}$ ratio of 0.225. Similarly, by referring to Figure 7-9, we see that a $V_{GS}/V_{GS(off)}$ ratio of 0.225 corresponds to a g_m/g_{m0} ratio of 0.774. Based on these observations, we conclude the following.

When: $I_D = 0.6I_{DSS}$:

$$\begin{aligned} V_{GS} &= 0.225V_{GS(off)} \\ g_m &= 0.774g_{m0} \end{aligned}$$

In practice, the actual curves for a given JFET deviate somewhat from the ideal curves in Figure 7-8 and Figure 7-9. For this reason, the preceding conclusions are only approximate.

SELF-BIAS

In a self-bias circuit, the value of R_S is:

$$R_S = \frac{|V_{GS}|}{I_D}$$

Assuming the circuit is designed so that $I_D = 0.6I_{DSS}$ and $V_{GS} = 0.225V_{GS(off)}$, we have:

$$\begin{aligned} R_S &= \frac{0.225|V_{GS(off)}|}{0.6I_{DSS}} \\ R_S &= \frac{0.375|V_{GS(off)}|}{I_{DSS}} \end{aligned}$$

Substituting $\frac{2I_{DSS}}{g_{m0}}$ for $|V_{GS(off)}|$ yields:

$$R_S = \frac{0.75}{g_{m0}} \quad (\text{Eq. 7-24})$$

Equation 7-24 provides a simple means of calculating a "reasonable" value of R_S for a self-bias circuit. Since the unit-to-unit variations in g_{m0} are significant, the average g_{m0} value is used to calculate the required value of R_S . The following example illustrates a typical self-bias design problem.

Example 7-14

The JFET in Figure 7-40 has the following specifications:

Parameter	Minimum	Maximum
I_{DSS}	2mA	10mA
$V_{GS(off)}$	-1V	-3V
g_{mo}	4mS	7mS
BV_{GSS}	—	50V

The amplifier in Figure 7-40 should have a typical voltage gain of 10, and an $R_{IN} \geq 800k\Omega$. Work out values for R_C , R_S , R_D , and V_{DD} . How could values of C_1 , C_2 , and C_3 be determined?

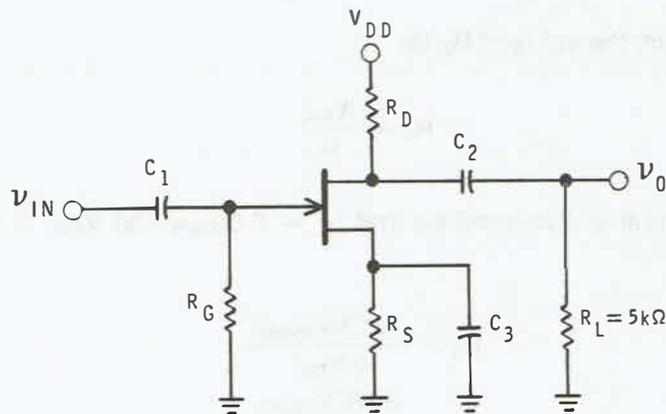


Figure 7-40

" $\times 10$ " self-bias common-source amplifier.

Since $R_{IN} = R_G$, a $1\text{M}\Omega$ resistor is chosen for R_G . Obviously, this satisfies the requirement that $R_{IN} \geq 800\text{k}\Omega$.

Based on the given specifications, the average parameter values are:

$$I_{DSS} = 6\text{mA}$$

$$V_{GS(off)} = -2\text{V}$$

$$g_{mo} = 5.5\text{mS}$$

Using these average values the circuit will be designed so that $I_{DQ} \approx 0.6I_{DSS}$. Thus:

$$R_S = \frac{0.75}{g_{mo}} = \frac{0.75}{5.5\text{mS}} = 136.4\Omega$$

$$I_D = 0.6I_{DSS} = 0.6(6\text{mA}) = 3.6\text{mA} = I_{DQ}$$

$$g_m = 0.774(g_{mo}) = 0.774(5.5\text{mS}) = 4.23\text{mS} = g_{mo}$$

Since $A_V = -g_m r_L$, the value of r_L required for a voltage gain of 10 is:

$$r_L = \frac{|A_V|}{g_m} = \frac{10}{4.23\text{mS}} = 2.36\text{k}\Omega$$

The required value of R_D is therefore:

$$R_D = \frac{R_L r_L}{R_L - r_L} = \frac{5\text{k}\Omega(2.36\text{k}\Omega)}{5\text{k}\Omega - 2.36\text{k}\Omega} = 4.47\text{k}\Omega$$

The drain-to-source voltage, V_{DS} , plus the voltage drops across R_D and R_S must add up to the supply voltage V_{DD} . Thus:

$$V_{DD} = V_{DS} + I_D(R_D + R_S)$$

$$V_{DD} = V_{DS} + 3.6\text{mA}(4.47\text{k}\Omega + 136.4\Omega)$$

$$V_{DD} = V_{DS} + 16.6\text{V}$$

Obviously, V_{DD} must be greater than 16.6V. It also should be less than BV_{GS} to prevent breakdown. Selecting $V_{DS} \approx 8V$ should permit ample signal swing in the output voltage. Consequently, we select $V_{DD} = 25V$.

The various capacitor values are selected to provide good coupling and bypass action at the lowest signal frequency. Similar to the approach used for BJT circuits, the following formulas can be used to calculate the various capacitor values:

$$C_1 \geq \frac{3.18}{f_1 R_G}, C_2 \geq \frac{3.18}{f_1 R_L}, C_3 \geq \frac{3.18}{f_1 R_S}$$

Voltage-Divider Bias

In a voltage-divider circuit, the value of R_S is given by:

$$R_S = \frac{V_{GG} - V_{GS}}{I_D}$$

The following example illustrates the design of a voltage-divider common-source amplifier based on average parameter values.

Example 7-15

The JFET in Figure 7-41 is the same type as in Example 7-14. Therefore, the average parameter values are:

$$I_{DSS} = 6\text{mA}$$

$$V_{GS(\text{off})} = -2\text{V}$$

$$g_{m0} = 5.5\text{mS}$$

Calculate the values for R_1 , R_2 , R_S , and R_D needed to provide a typical voltage gain of 5. What is the amplifier's input resistance?

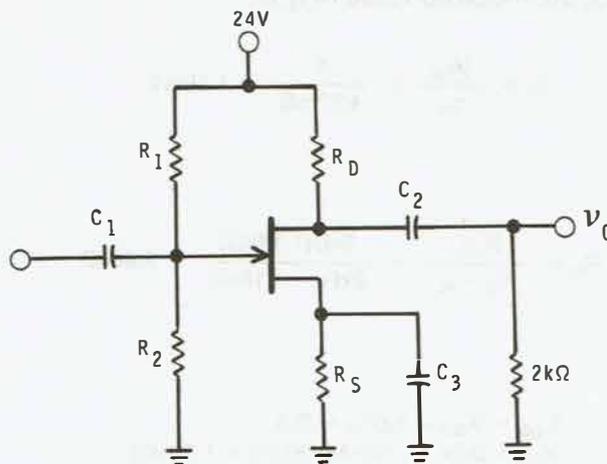


Figure 7-41

" $\times 5$ " voltage-divider common-source amplifier.

Using average values, the circuit will be designed so that $I_{DQ} = 0.6I_{DSS}$. Thus:

$$I_D = 0.6(6\text{mA}) = 3.6\text{mA} = I_{DQ}$$

$$V_{GS} = 0.225(-2\text{V}) = -0.45\text{V} = V_{GSQ}$$

$$g_m = 0.774(5.5\text{mS}) = 4.23\text{mS} = g_{mo}$$

Somewhat arbitrarily, we choose $V_{R_2} = V_{GG} = 6\text{V}$. Selecting $R_2 = 15\text{k}\Omega$ requires an R_1 value of:

$$R_1 = \frac{R_2[V_{DD} - V_{GG}]}{V_{GG}} = \frac{15\text{k}\Omega[24\text{V} - 6\text{V}]}{6\text{V}} = 45\text{k}\Omega$$

$$R_S = \frac{V_{GG} - V_{GS}}{I_D} = \frac{6\text{V} - (-0.45\text{V})}{3.6\text{mA}} = 1.79\text{k}\Omega$$

For a voltage gain of 5, the required value of r_L is:

$$r_L = \frac{|A_v|}{g_m} = \frac{5}{4.23\text{mS}} = 1.18\text{k}\Omega$$

R_D is therefore:

$$R_D = \frac{R_L r_L}{R_L - r_L} = \frac{2\text{k}\Omega(1.18\text{k}\Omega)}{2\text{k}\Omega - 1.18\text{k}\Omega} = 2.88\text{k}\Omega$$

As a check:

$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_D + R_S) \\ V_{DS} &= 24\text{V} - 3.6\text{mA}(2.88\text{k}\Omega + 1.79\text{k}\Omega) \\ V_{DS} &= 7.19\text{V} \end{aligned}$$

This is sufficiently large to provide a reasonable signal swing in the output voltage.

$$R_{IN} = R_1 \parallel R_2 = 45\text{k}\Omega \parallel 15\text{k}\Omega = 11.25\text{k}\Omega$$

The calculated value of R_{IN} is very small for a JFET circuit. By increasing the values of R_1 and R_2 , but maintaining the same ratio, the input resistance could be increased significantly. However, large resistance values are not always available in the desired ratio. A better solution is illustrated by the circuit shown in Figure 7-42. Here, a large resistor, R_G , is connected between the gate and mid-point of the voltage divider. In this case:

$$R_{IN} = R_1 \parallel R_2 + R_G$$

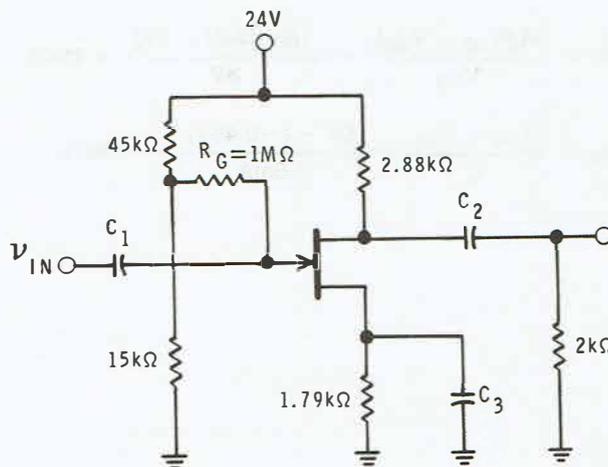


Figure 7-42

Modified form of the amplifier in Example 7-15 to obtain a large value of R_{IN} .

With the simple modification, small values of R_1 and R_2 can be used for the voltage-divider without decreasing the input resistance of the amplifier.

Current-Source Bias

To prevent the gate from becoming forward biased in a current-source bias circuit, you must select component values so that $I_D < I_{DSS(MIN)}$.

For this reason, the following design example sets up an $I_{DQ} \approx 0.6I_{DSS(MIN)}$ rather than $0.6I_{DSS(ave)}$.

Example 7-16

Assuming $I_{DSS(MIN)} = 2\text{mA}$, calculate the component values for the circuit shown in Figure 7-43. As before, assume the average JFET parameters are:

$$\begin{aligned} I_{DSS} &= 6\text{mA} \\ V_{GS(off)} &= -2\text{V} \\ g_{mo} &= 5.5\text{mS} \end{aligned}$$

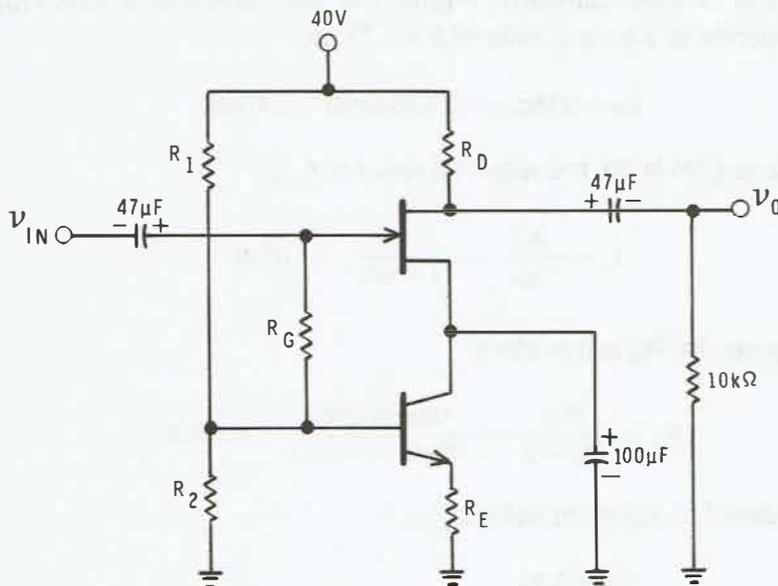


Figure 7-43

" $\times 10$ " current-source amplifier for Example 7-16.

Our basic approach is to set up an $I_{DQ} = 0.6I_{DSS(MIN)}$ or 1.2mA in this example. For simplicity, we will assume the values of I_{DSS} , $V_{GS(off)}$, and g_{mo} equal the average values calculated previously. Thus:

$$I_{DQ} = I_C = 1.2\text{mA}$$

Arbitrarily we select $V_B = 10V$ and $R_2 = 33k\Omega$. Thus, the required value of R_1 is:

$$R_1 = \frac{R_2[V_{DD} - V_B]}{V_B} = \frac{33k\Omega[30V - 10V]}{10V} = 66k\Omega$$

$$R_E = \frac{V_B - V_{BE}}{I_E} = \frac{10V - 0.7V}{1.2mA} = 7.75k\Omega$$

The input resistance equals $R_1 || R_2 + R_G$. Selecting $R_G = 1M\Omega$ provides a reasonably large value of R_{IN} . Thus:

$$R_G = 1M\Omega$$

In order to calculate r_L and R_D , you need to know the approximate value of g_m for the given bias conditions. Using average I_{DSS} we have:

$$\frac{I_D}{I_{DSS}} = \frac{1.2mA}{6mA} = 0.2$$

Referring to Figure 7-8, we find that an I_D/I_{DSS} ratio of 0.2 corresponds to a $V_{GS}/V_{GS(off)}$ ratio of 0.55. Similarly, Figure 7-9 indicates that a $V_{GS}/V_{GS(off)}$ ratio of 0.55 corresponds to a g_m/g_{mo} ratio of 0.45. Thus:

$$g_m = 0.45g_{mo} = 0.45(5.5mS) = 2.47mS$$

Since the voltage gain is 10, the required value of r_L is:

$$r_L = \frac{|A_V|}{g_m} = \frac{10}{2.47mS} = 4.05k\Omega$$

The value required for R_D is therefore:

$$R_D = \frac{R_L r_L}{R_L - r_L} = \frac{10k\Omega(4.05k\Omega)}{10k\Omega - 4.05k\Omega} = 6.81k\Omega$$

With the calculated component values:

$$V_E = 9.3V$$

$$V_C = V_S = |V_{GS}| + V_B$$

$$V_C = 2V + 10V = 12V$$

$$V_D = V_{DD} - I_D R_D$$

$$V_D = 40V - 1.2mA(6.81k\Omega) = 31.83V$$

Thus:

$$V_{DS} = V_D - V_S$$

$$V_{DS} = 31.83V - 12V = 19.8V$$

$$V_{CE} = V_C - V_E$$

$$V_{CE} = 12V - 9.3V = 2.7V$$

Self-Test Review

11. A source-follower is another name for a common-_____ amplifier.
12. Zero bias is a popular biasing scheme for _____ -mode MOSFETs.
13. Drain-feedback bias is frequently used for _____ -mode MOSFETs.
14. Assuming $g_{m0(\text{MIN})} = 1\text{mS}$ and $g_{m0(\text{MAX})} = 5\text{mS}$, $R_S \approx$ _____ Ω to provide an $I_D \approx 0.6I_{DSS}$ in a self-bias circuit.

Refer to Figure 7-44 for questions 15 through 20.

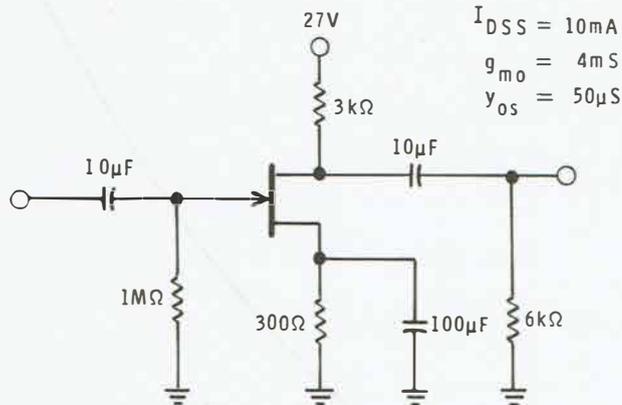


Figure 7-44

Circuit for Self-Test Review questions 15-20.

15. $V_{GS(\text{off})} \approx$ _____ V.
16. $R_{IN} \approx$ _____ Ω .
17. Neglecting y_{os} , $R_O \approx$ _____ k Ω .
18. Taking y_{os} into account, $R_O \approx$ _____ k Ω .

19. Figure 7-45 provides the JFET's transconductance curve. Using the transconductance curve, construct the bias curve for $R_S = 300\Omega$. Based on the resulting curve, $I_{DQ} = \underline{\hspace{2cm}}$ mA and $V_{GSQ} = \underline{\hspace{2cm}}$ V.
20. The voltage gain, A_V , is approximately .

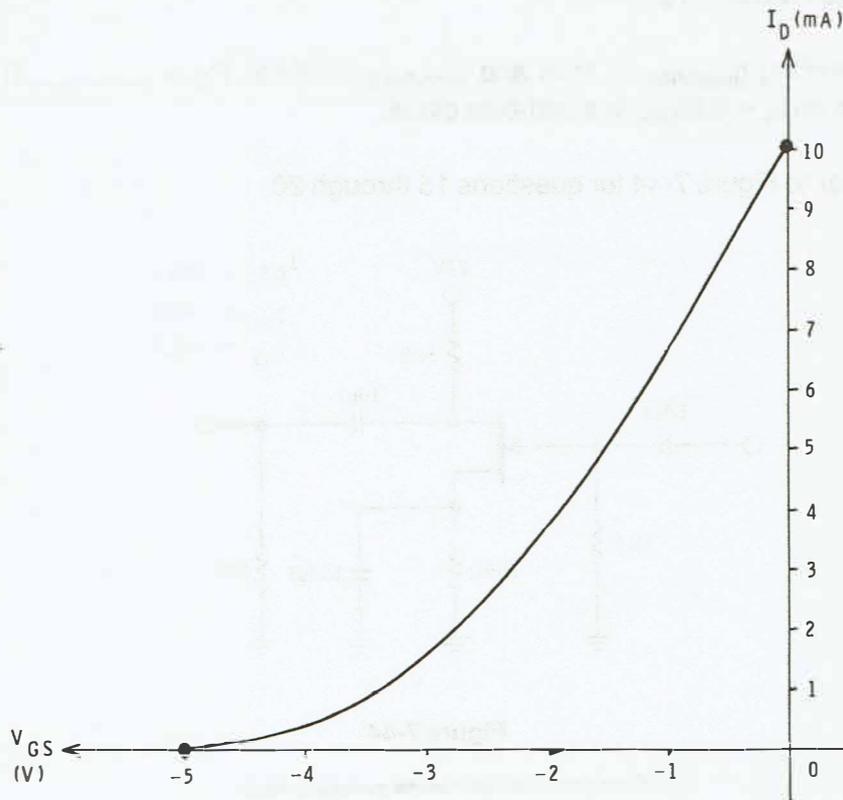


Figure 7-45

Transconductance curve for the JFET in Figure 7-44.

Answers

- | | |
|------------------|---------------------------------|
| 11. drain | 16. $1\text{M}\Omega$ |
| 12. depletion | 17. $3\text{k}\Omega$ |
| 13. enhancement | 18. $2.61\text{k}\Omega$ |
| 14. 250Ω | 19. $5\text{mA}, -1.47\text{V}$ |
| 15. -5V | 20. -5.16 |

The solution to appropriate questions follow:

14. The average g_{mo} is:

$$g_{mo} = \frac{1\text{mS} + 5\text{mS}}{2} = 3\text{mS}$$

Since:

$$R_S = \frac{0.75}{g_{mo}} \text{ for } I_D \approx 0.6I_{DSS}$$

Then:

$$R_S = \frac{0.75}{3\text{mS}} = 250\Omega$$

$$15. |V_{GS(\text{off})}| = \frac{2I_{DSS}}{g_{mo}} = \frac{2(10\text{mA})}{4\text{mS}} = 5\text{V}$$

Thus, $V_{GS(\text{off})} \approx -5\text{V}$ since the JFET in Figure 7-44 is an N-channel device.

$$16. R_{IN} = R_G = 1\text{M}\Omega.$$

$$17. R_O \approx R_D = 3\text{k}\Omega$$

$$18. r_d = \frac{1}{y_{os}} = \frac{1}{50\mu\text{S}} = 20\text{k}\Omega$$

$$R_O = r_d \parallel R_D$$

$$R_O = 20\text{k}\Omega \parallel 3\text{k}\Omega = 2.61\text{k}\Omega$$

19. The equation of the self-bias curve is $V_{GS} = -I_D R_S$. Thus, when $V_{GS} = 0$, $I_D = 0$. However, when $V_{GS} = -1V$:

$$I_D = \frac{-(-1V)}{R_S} = \frac{1V}{300\Omega} = 3.33mA$$

The construction is shown in Figure 7-46. Note that:

$$I_{DQ} \approx 5mA \text{ and } V_{GSQ} \approx -1.47V$$

20. $\frac{I_D}{I_{DSS}} = 0.5$

From Figure 7-8 we find $V_{GS}/V_{GS(off)} \approx 0.29$. Figure 7-9 indicates that a $V_{GS}/V_{GS(off)}$ ratio of 0.29 corresponds to a g_m/g_{m0} ratio of, approximately, 0.71. Thus:

$$g_m = 0.71g_{m0}$$

$$g_m = 0.71(4mS) = 2.84mS$$

$$r_L = r_d \parallel R_D \parallel R_L$$

$$r_L = 20k\Omega \parallel 3k\Omega \parallel 6k\Omega = 1.82k\Omega$$

$$A_v = -g_m r_L$$

$$A_v = -2.84mS(1.82k\Omega)$$

$$A_v = -5.16$$

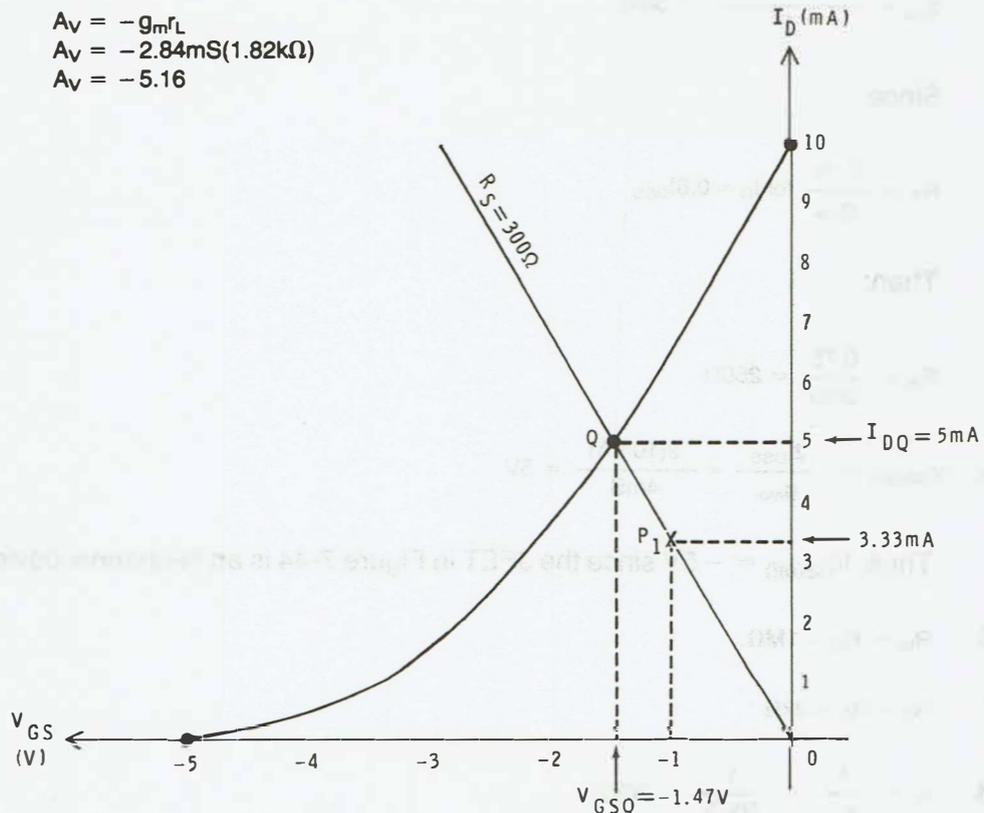


Figure 7-46

Graphical solution to Self-Test Review question number 19.

SUMMARY

Since only majority carriers are required for proper operation, FETs are referred to as unipolar devices. A summary of the various types of FETs is provided by the FET family tree in Figure 7-47.

Broadly speaking, FETs are classified as either JFETs or IGFETs (MOSFETs). Both JFETs and IGFETs are available in N-channel and P-channel varieties. From a user's point of view, the only difference between N-channel and P-channel devices are the current directions and voltage polarities.

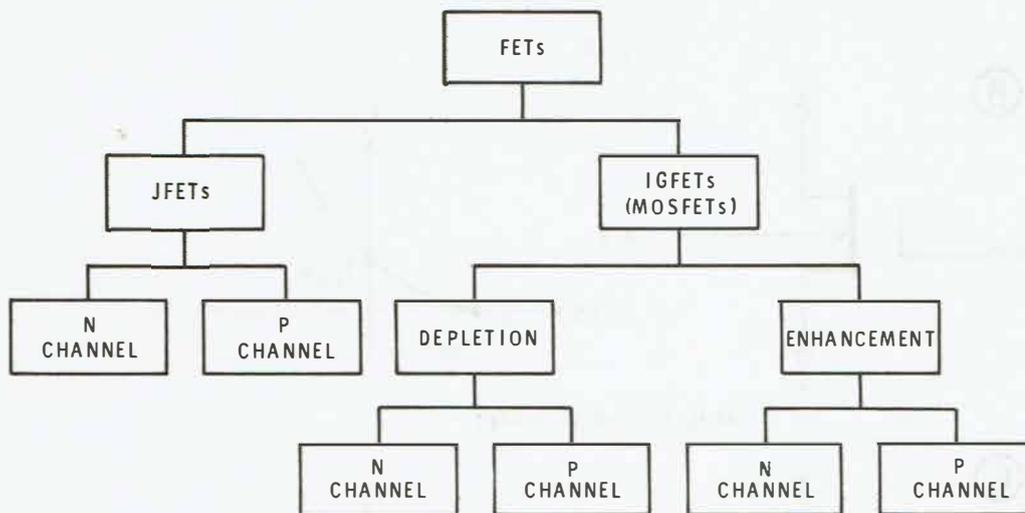


Figure 7-47

FET family tree.

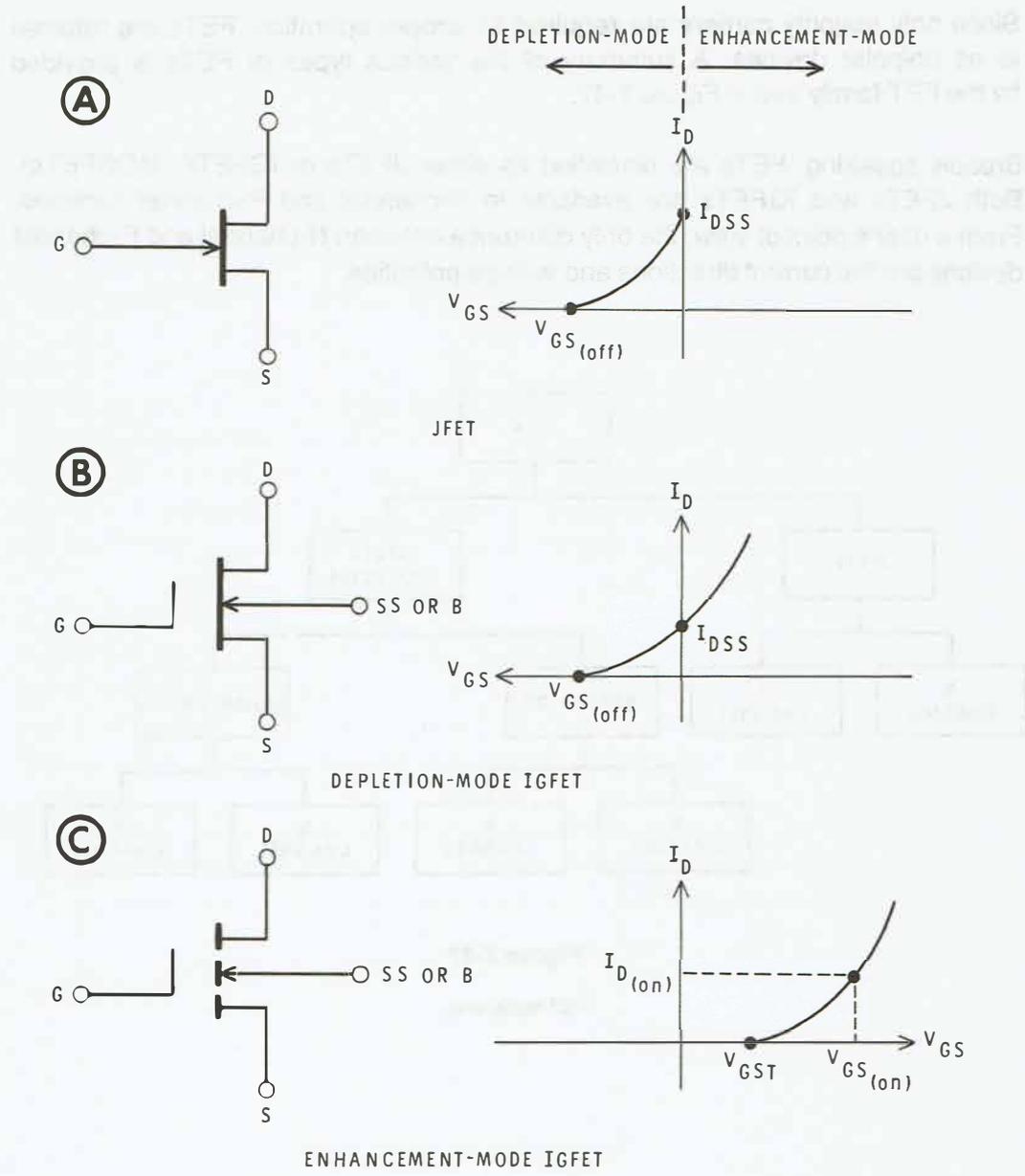


Figure 7-48

Schematic symbols and transconductance curves for N-channel FETs.

- A. JFET.
- B. Depletion-mode IGFET.
- C. Enhancement-mode IGFET.

JFETs can only operate in the depletion-mode. So called depletion-mode IGFETs can operate in either the depletion- or enhancement-mode. Finally, enhancement-mode IGFETs can only operate in the enhancement-mode. These various operating modes are summarized by the transconductance curves, for N-channel devices, in Figure 7-48. Note that a depletion-mode IGFET is normally on, while an enhancement-mode IGFET is normally off.

Today, high power FETs are available that are both efficient and economical. The development of VMOS technology made this possible. For digital applications, ICs are available that utilize both N-channel and P-channel enhancement-mode IGFETs. Due to their low power consumption, these CMOS chips are especially attractive for battery-operated equipment.

The analysis and design of FET circuits is complicated by the fact that graphical as well as analytical methods must be used. For analysis, a bias line is constructed on the FET's transconductance curve. The intersection of the bias line and transconductance curve provides the device's operating point. Examples in the unit illustrated how the Q point was located in self-bias and voltage-divider bias circuits.

Current-source bias provides a value of I_{DQ} that is essentially independent of parameter variations. The value of V_{GSQ} , however, does depend on the actual parameter values. In a current-source bias circuit, I_{DQ} must be less than $I_{DSS(MIN)}$. For this reason, the BJT current source should be designed so that $I_C < I_{DSS(MIN)}$.

Examples illustrating the design of self-bias, voltage-divider bias, and current-source bias circuits were provided in the unit. The simplified design procedures used in these examples are suitable when approximate results are acceptable.

The first step in the design of a power MOSFET is the selection of the device type. The most common type is the N-channel MOSFET, which is used for most power applications. The next step is to determine the required power and voltage ratings for the device. This is done by calculating the average power and peak-to-peak voltage across the device. The average power is determined by the duty cycle and the peak-to-peak voltage is determined by the switching frequency and the load inductance. Once the power and voltage ratings are determined, the next step is to select a device that meets these requirements. This is done by consulting the data sheets of various MOSFET manufacturers.

Once a device has been selected, the next step is to determine the required gate drive. The gate drive is the voltage and current required to turn the MOSFET on and off. The gate voltage is determined by the threshold voltage of the device and the gate-source capacitance. The gate current is determined by the gate-source capacitance and the switching frequency. Once the gate drive requirements are determined, the next step is to design the gate drive circuit. This is done by selecting a gate driver IC and designing the gate drive network.

The final step in the design of a power MOSFET is the selection of the heat sink. The heat sink is used to dissipate the heat generated by the MOSFET. The heat sink is selected based on the power dissipation of the MOSFET and the ambient temperature. The power dissipation is determined by the average power and the junction temperature. The ambient temperature is determined by the operating environment. Once the heat sink is selected, the next step is to design the heat sink mounting. This is done by selecting a mounting method and designing the heat sink mounting hardware.

Once the heat sink mounting has been designed, the next step is to design the MOSFET driver circuit. The MOSFET driver circuit is used to drive the MOSFET. It consists of a gate driver IC and a gate drive network. The gate driver IC is selected based on the gate drive requirements. The gate drive network is designed to provide the required gate voltage and current. Once the MOSFET driver circuit has been designed, the next step is to design the MOSFET switching circuit. This is done by selecting a switching method and designing the switching circuit hardware.

Once the MOSFET switching circuit has been designed, the next step is to design the MOSFET protection circuit. The MOSFET protection circuit is used to protect the MOSFET from overvoltage and overcurrent. It consists of a snubber network and a current limit circuit. The snubber network is designed to limit the voltage across the MOSFET during switching. The current limit circuit is designed to limit the current through the MOSFET during switching. Once the MOSFET protection circuit has been designed, the next step is to design the MOSFET test circuit. This is done by selecting a test method and designing the test circuit hardware.

UNIT EXAMINATION

The following multiple choice examination is designed to test your understanding of the material presented in this unit. Place a check beside the multiple choice answer (A, B, C, or D) that you feel is most correct. When you have completed the examination, compare your answers with the correct ones that appear after the exam.

1. An N-channel JFET has an I_{DSS} of 10mA and a V_P of 3V. The value of $V_{GS(off)}$ is therefore approximately:
 - A. +3V.
 - B. 0V.
 - C. -3V.
 - D. Twice the value of V_{GSQ} .
2. A depletion-mode IGFET can operate in the:
 - A. Depletion-mode only.
 - B. P- or N-channel modes.
 - C. Enhancement-mode only.
 - D. Depletion- or enhancement-mode.
3. Assuming $I_{DSS} = 10\text{mA}$, $g_{m0} = 5000\mu\text{S}$, and $g_{os} = 0.01\text{mS}$, then:
 - A. $r_d = 200\Omega$.
 - B. $|V_{GS(off)}| = 4\text{V}$.
 - C. $|V_{GS(off)}| = 2\text{kV}$.
 - D. The FET is saturated.
4. An N-channel JFET has $I_{DSS} = 12\text{mA}$, $V_{GS(off)} = -3\text{V}$, and $g_{m0} = 8\text{mS}$. A gate-to-source voltage of -1V produces a drain current of approximately:
 - A. 5.33mA.
 - B. 12mA.
 - C. more than 12mA.
 - D. 7.72mA.
5. In question 4, the value of g_m is approximately:
 - A. 8mS.
 - B. 5.34mS.
 - C. 10mS.
 - D. 6.48mS.

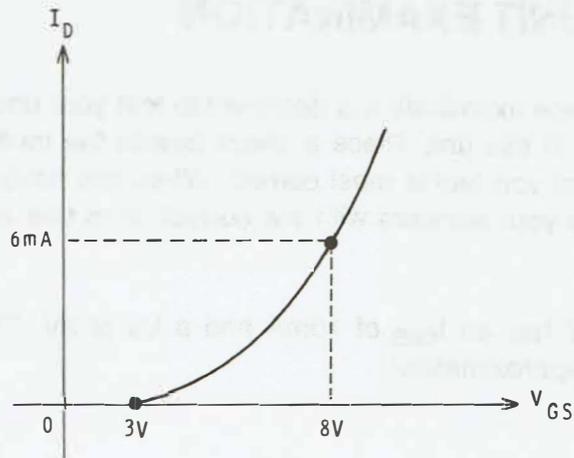


Figure 7-49

Transconductance curve for questions 6 and 7.

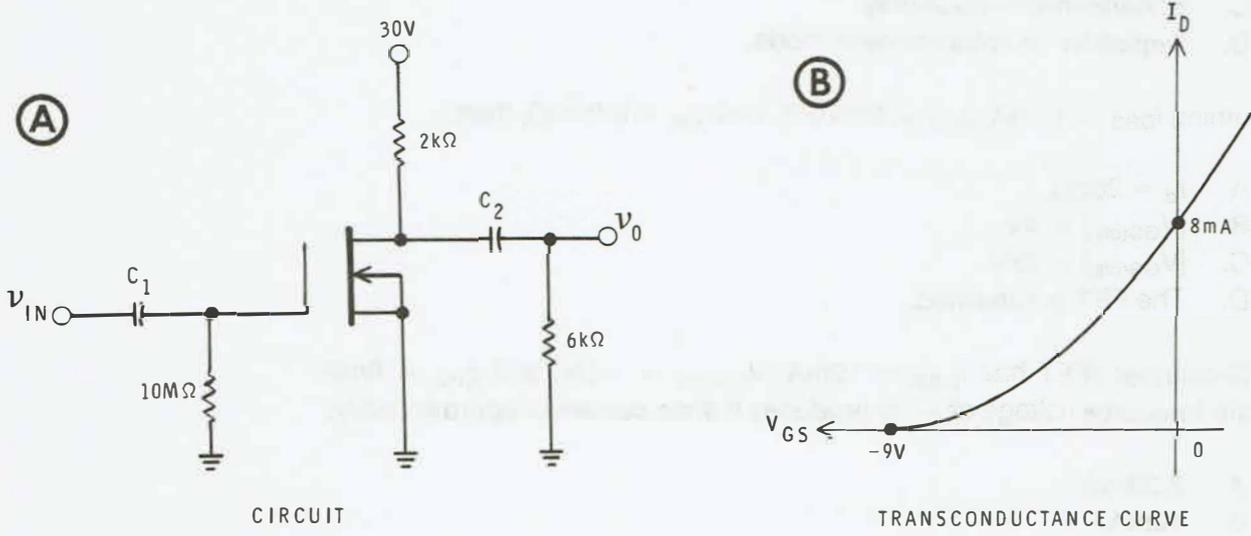


Figure 7-50

Circuit and transconductance curve for questions 9-11.

Refer to Figure 7-49 for questions 6 and 7.

6. Based on the sketch in figure 7-50, K has a value of approximately:
- A. +3.
 - B. +8.
 - C. -3.
 - D. 0.24×10^{-3} .
7. Assuming $V_{GS} = 10V$, I_D is approximately:
- A. 11.76mA.
 - B. 7.5mA.
 - C. Zero, since V_{GS} is positive.
 - D. Equal to I_{DSS} .
8. A JFET has $g_{m0} = 4mS$, $I_{DSS} = 10mA$, and $V_{GS(off)} = -5V$. The JFET is biased so that $I_{DQ} = 0.6I_{DSS}$. Assuming $r_L = 5k\Omega$, the common-source voltage gain is approximately:
- A. -20.
 - B. +20.
 - C. -15.5.
 - D. ≈ 1 .

Refer to Figure 7-50 for questions 9 through 11.

9. I_D is approximately equal to:
- A. 0.
 - B. $0.6I_{DSS}$.
 - C. $0.5I_{DSS}$.
 - D. 8mA.
10. V_D is approximately equal to:
- A. 14V.
 - B. $-(V_{GSQ})$.
 - C. 0V.
 - D. $0.225|V_{GSQ}|$.
11. The input resistance is approximately:
- A. $\infty\Omega$.
 - B. 10M Ω .
 - C. 30V/8mA.
 - D. V_{GSQ}/I_{DSS} .

Refer to Figure 7-51 for questions 12 through 15.

12. To provide an R_{IN} of $1\text{M}\Omega$, R_G should equal:

- A. $1\text{M}\Omega$.
- B. V_{GSS}/I_{DSS} .
- C. $25\text{V}/8\text{mA}$.
- D. $10r_{S'}$.

13. Assuming $I_{DC} = 0.6I_{DSS}$, R_S should approximately equal:

- A. R_G .
- B. R_D .
- C. r_L .
- D. 93.75Ω .

14. Assuming $I_D = 0.6I_{DSS}$, A_V is approximately:

- A. -12.38 .
- B. $+12.38$.
- C. -16 .
- D. $+16$.

15. Assuming $I_D = 0.6I_{DSS}$, V_D is approximately:

- A. 25V .
- B. 0.45V .
- C. 10.6V .
- D. 1V .

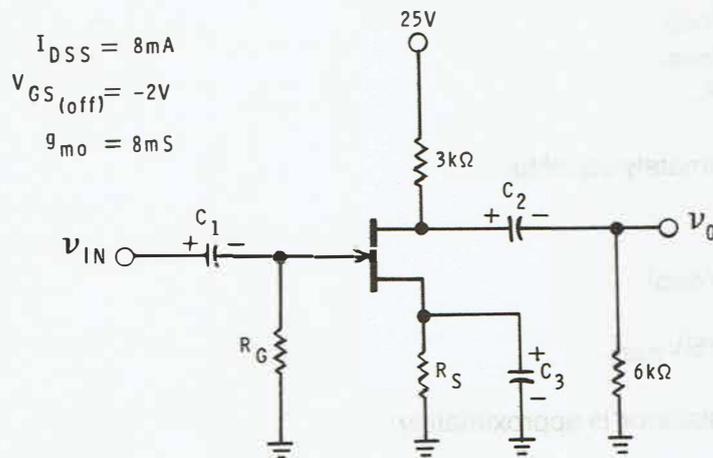


Figure 7-51

Circuit for questions 12-15.

EXAMINATION ANSWERS

1. C — $|V_{GS(off)}| = V_P$ or 3V in this case. For an N-channel JFET, $|V_{GS(off)}|$ is negative. Thus, $V_{GS(off)} = -3V$.
2. D — A depletion-mode IGFET can operate in either the depletion- or enhancement-mode.

3. B — $|V_{GS(off)}| = \frac{2I_{DSS}}{g_{m0}} = \frac{2(10mA)}{5000\mu S} = 4V$

4. A — For a JFET:

$$I_D = I_{DSS} \left[1 - \frac{|V_{GS}|}{|V_{GS(off)}|} \right]^2$$

Thus:

$$I_D = 12mA \left[1 - \frac{1}{3} \right]^2 = 5.33mA$$

5. B — $\frac{V_{GS}}{V_{GS(off)}} = \frac{-1V}{-3V} = 0.333$

Figure 7-9 indicates that a $V_{GS}/V_{GS(off)}$ ratio of 0.333 corresponds to a g_m/g_{m0} ratio of approximately 0.667. Thus:

$$g_m = 0.667g_{m0} = 0.667(8mS) = 5.34mS$$

6. D — For an enhancement-mode IGFET:

$$I_D = K[V_{GS} - V_{GST}]^2$$

Thus:

$$K = \frac{I_D}{(V_{GS} - V_{GST})^2}$$

Since $V_{GST} = 3V$ and $I_D = 6mA$, when $V_{GS} = 8V$ we have:

$$K = \frac{6mA}{(8V - 3V)^2} = 0.24 \times 10^{-3}$$

7. A — $I_D = K[V_{GS} - V_{GST}]^2$
 $I_D = 0.24 \times 10^{-3}[10V - 3V]^2 = 11.76mA$

8. C — When $I_D = 0.6I_{DSS}$, $g_m = 0.774g_{mo}$. Thus:

$$g_m = 0.774(4mS) = 3.096mS \approx 3.1mS$$

$$A_v = -g_m r_L$$

$$A_v = -3.1mS(5k\Omega) = -15.5$$

Here, the negative sign simply indicates that v_{IN} and v_O are 180° out of phase with each other.

9. D — This is an example of zero-bias. Since $V_{GS} = 0$, $I_D = I_{DSS}$ or $8mA$ in this case.

10. A — $V_D = V_{DD} - I_D R_D$
 $V_D = 30V - 8mA(2k\Omega) = 14V$

11. B — $R_{IN} \approx R_G = 10M\Omega$

12. A — Since $R_{IN} \approx R_G$, R_G should equal $1M\Omega$.

13. D — In a self-bias circuit $R_S = 0.75/g_{mo}$ when $I_D = 0.6I_{DSS}$. Thus:

$$R_S = \frac{0.75}{8mS} = 93.75\Omega$$

14. A — When $I_D = 0.6I_{DSS}$, $g_m \approx 0.774g_{mo}$. Thus:

$$g_m = 0.774(8mS) = 6.19mS$$

$$r_L = R_D || R_L = 3k\Omega || 6k\Omega = 2k\Omega$$

$$A_v = -g_m r_L = -6.19mS(2k\Omega) = -12.38$$

15. C — $I_D = 0.6I_{DSS}$
 $I_D = 0.6(8mA) = 4.8mA$

$$V_D = V_{DD} - I_D R_D$$

$$V_D = 25V - 4.8mA(3k\Omega)$$

$$V_D = 10.6V$$

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UNIT 8

**COMMON-EMITTER
FREQUENCY
EFFECTS**

CONTENTS

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INTRODUCTION

An ideal amplifier would provide the same amount of amplification for all signal frequencies. In other words, the voltage gain would be frequency independent. Similarly, the amplifier's input resistance, output resistance, and the phase shift between the input and output signals would also be frequency independent. However, real amplifiers always contain some capacitance. Most amplifiers, for example, have coupling and bypass capacitors. In addition, numerous "parasitic capacitances", due to internal characteristics and external stray or wiring capacitance, are always present.

Since capacitive reactance varies with frequency, the presence of capacitance in real amplifiers causes the characteristics of real amplifiers to vary with frequency. This unit discusses the nature of selected amplifier characteristics that are frequency dependent.

UNIT OBJECTIVES

When you have completed this unit, you should be able to:

1. Calculate the voltage gain, phase angle, and cutoff frequency for passive RC low-pass, and high-pass filters.
2. Estimate the cutoff frequencies for a passive bandpass filter.
3. Sketch Bode plots for passive RC filters.
4. Estimate C_{be} and C_{bc} from data sheet values.
5. Identify the three high-pass and two low-pass filters of a common-emitter amplifier.
6. Estimate F_1 and F_2 for a common-emitter amplifier.
7. Define rise time and sag time in frequency terms.
8. Estimate F_1 and F_2 from rise time and sag measurements.

UNIT ACTIVITY GUIDE

- Read section on "Essential Filter Concepts."
- Answer Self-Test Review Questions 1-12.
- Read section on "RC Coupled Amplifier Frequency Response."
- Answer Self-Test Review Questions 13-22.
- Perform Experiment 13 in Unit 9.
- Study Summary.
- Complete Unit Examination.
- Check Examination Answers.

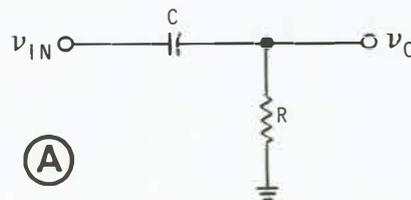
ESSENTIAL FILTER CONCEPTS

Amplifier frequency effects can be understood by considering the amplifier as an active bandpass filter. A bandpass filter exhibits the characteristics of both a high-pass and a low-pass filter. For this reason, we will begin this discussion of frequency effects by reviewing the characteristics of high-pass and low-pass filters.

The High-Pass Filter

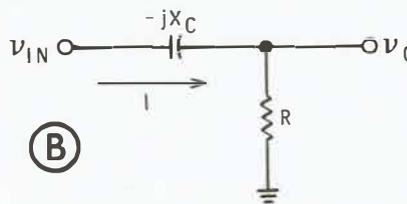
Filters are frequency selective circuits. Consequently, some signal frequencies pass through a filter with minimum attenuation, while other signal frequencies are greatly attenuated. The frequency above or below those signals that tend to be passed or blocked by the filter is referred to as the filter's **cutoff frequency**, F_{CO} .

A high-pass filter tends to pass signal frequencies that are above F_{CO} , and block signal frequencies that are below F_{CO} . An example of an elementary high-pass filter circuit is shown in Figure 8-1A.



(A)

ORIGINAL CIRCUIT



(B)

FREQUENCY DOMAIN CIRCUIT

Figure 8-1

High-pass filter.

- A. Original circuit.
- B. Frequency domain circuit.

Here, we wish to determine the manner in which the output voltage varies as the frequency of the input voltage varies between zero and infinity. To do this, we must use complex notation, as indicated by the frequency domain circuit in Figure 8-1B. The circuit's input impedance is:

$$Z = R - jX_C = R - \frac{j}{\omega C} = \frac{\omega RC - j}{\omega C}$$

Via Ohm's law:

$$I = \frac{V}{Z} = \frac{V}{\frac{\omega RC - j}{\omega C}} = \frac{V\omega C}{\omega RC - j}$$

Since $V_O = IR$ we have:

$$V_O = IR = \frac{V\omega RC}{\omega RC - j}$$

A thorough discussion of complex notation is provided in Heath's **Passive Circuit Design** course, EE-1001. Even if you are not familiar with this notation, you should still find the results of the analysis quite useful.

Dividing numerator and denominator by ωRC :

$$V_O = \frac{V}{1 - \frac{j}{\omega RC}}$$

The circuit's voltage gain, A_V , is the ratio of V_O to V . Thus:

$$A_V = \frac{V_O}{V} = \frac{1}{1 - j \frac{1}{\omega RC}}$$

Converting to polar notation:

$$A_V = \frac{1}{\sqrt{1 + \frac{1}{(\omega RC)^2}} - L \text{ arc tan } \frac{1}{\omega RC}}$$

$$A_V = \frac{1}{\sqrt{1 + \frac{1}{(\omega RC)^2}} \left(L \text{ arc tan } \frac{1}{\omega RC} \right)}$$

Finally, letting $\omega RC = n$ we have:

$$A_v = \frac{1}{\sqrt{1 + \frac{1}{n^2}}} \left(L \arctan \frac{1}{n} \right) \quad (\text{Eq. 8-1})$$

Equation 8-1 indicates that the voltage gain is described by a complex number. Consequently, the voltage gain consists of two components - a **magnitude**, $|A_v|$, and a **phase angle**, θ .

In some circuits, you are primarily interested in the magnitude of the gain. In other circuits, phase information, or both magnitude and phase information are important. Therefore, it is useful to divide Equation 8-1 into two parts as follows:

$$|A_v| = \frac{1}{\sqrt{1 + \frac{1}{n^2}}} \quad (\text{Eq. 8-1a})$$

$$\theta = \arctan \frac{1}{n} \quad (\text{Eq. 8-1b})$$

By substituting different values of n into Equation 8-1a and Equation 8-1b, you can obtain the data required to plot the frequency response curves sketched in Figure 8-2B and Figure 8-2C respectively. Here, note that when $\omega RC = 1$, the voltage gain has a value of 0.707 and the phase angle, θ , equals 45° . The frequency at which this occurs defines the filter's cutoff frequency, F_{CO} , and may be calculated as follows:

$$\omega RC = 1 = n$$

Substituting $2\pi F_{CO}$ for ω :

$$2\pi F_{CO} RC = 1$$

$$F_{CO} = \frac{1}{2\pi RC} \quad (\text{Eq. 8-2})$$

The ratio of any frequency, F_1 , to the filter's cutoff frequency, F_{CO} is:

$$\frac{F}{F_{CO}} = F \div \frac{1}{2\pi RC} = 2\pi FRC = \omega RC$$

Since $\omega RC = n$ and the ratio of F to F_{CO} equals ωRC , it follows that the ratio of F to F_{CO} also equals n .

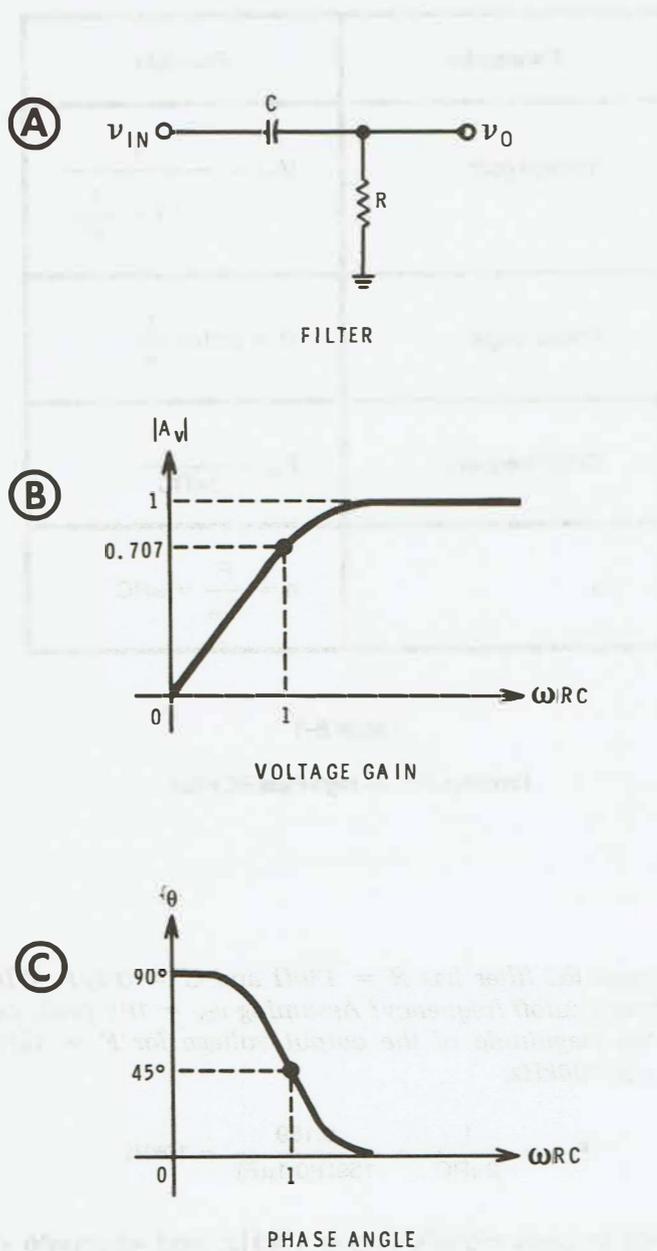


Figure 8-2

Frequency response of the high-pass RC filter.

- A. Filter.
- B. Voltage gain.
- C. Phase angle.

The result of our analysis is summarized in Table 8-1:

Parameter	Formula
Voltage gain	$ A_V = \frac{1}{\sqrt{1 + \frac{1}{n^2}}}$
Phase angle	$\Theta = \arctan \frac{1}{n}$
Cutoff frequency	$F_{\infty} = \frac{1}{2\pi RC}$
n	$n = \frac{F}{F_{\infty}} = \omega RC$

Table 8-1

Formulas For The High-Pass RC Filter.

Example 8-1

A high-pass RC filter has $R = 159\Omega$ and $C = 0.1\mu F$. What is the filter's cutoff frequency? Assuming $v_{IN} = 10V$ peak, calculate the magnitude of the output voltage for $F = 1kHz$, $10kHz$, and $100kHz$.

$$F_{CO} = \frac{1}{2\pi RC} = \frac{0.159}{159\Omega(0.1\mu F)} = 10kHz$$

Thus the filter tends to pass signals above 10kHz, and attenuate signals below 10kHz.

When $F = 1\text{kHz}$:

$$n = \frac{F}{F_{CO}} = \frac{1\text{kHz}}{10\text{kHz}} = 0.1$$

$$|A_V| = \frac{1}{\sqrt{1 + \frac{1}{n^2}}} = \frac{1}{\sqrt{101}} = 0.0995 \approx 0.1$$

$$\begin{aligned} v_O &= |A_V| v_{IN} \\ v_O &= 0.1(10V) = 1V_{\text{peak}} \end{aligned}$$

$$\theta = \arctan \frac{1}{n}$$

$$\theta = \arctan \frac{1}{0.1} = \arctan 10 = 84.3^\circ$$

When $F = 10\text{kHz}$:

$$n = \frac{F}{F_{CO}} = \frac{10\text{kHz}}{10\text{kHz}} = 1$$

$$|A_V| = \frac{1}{\sqrt{1 + \frac{1}{n^2}}} = \frac{1}{\sqrt{2}} = 0.707$$

$$\begin{aligned} v_O &= |A_V| v_{IN} \\ v_O &= 0.707(10V) = 7.07V \end{aligned}$$

$$\theta = \arctan \frac{1}{n}$$

$$\theta = \arctan \frac{1}{1} = 45^\circ$$

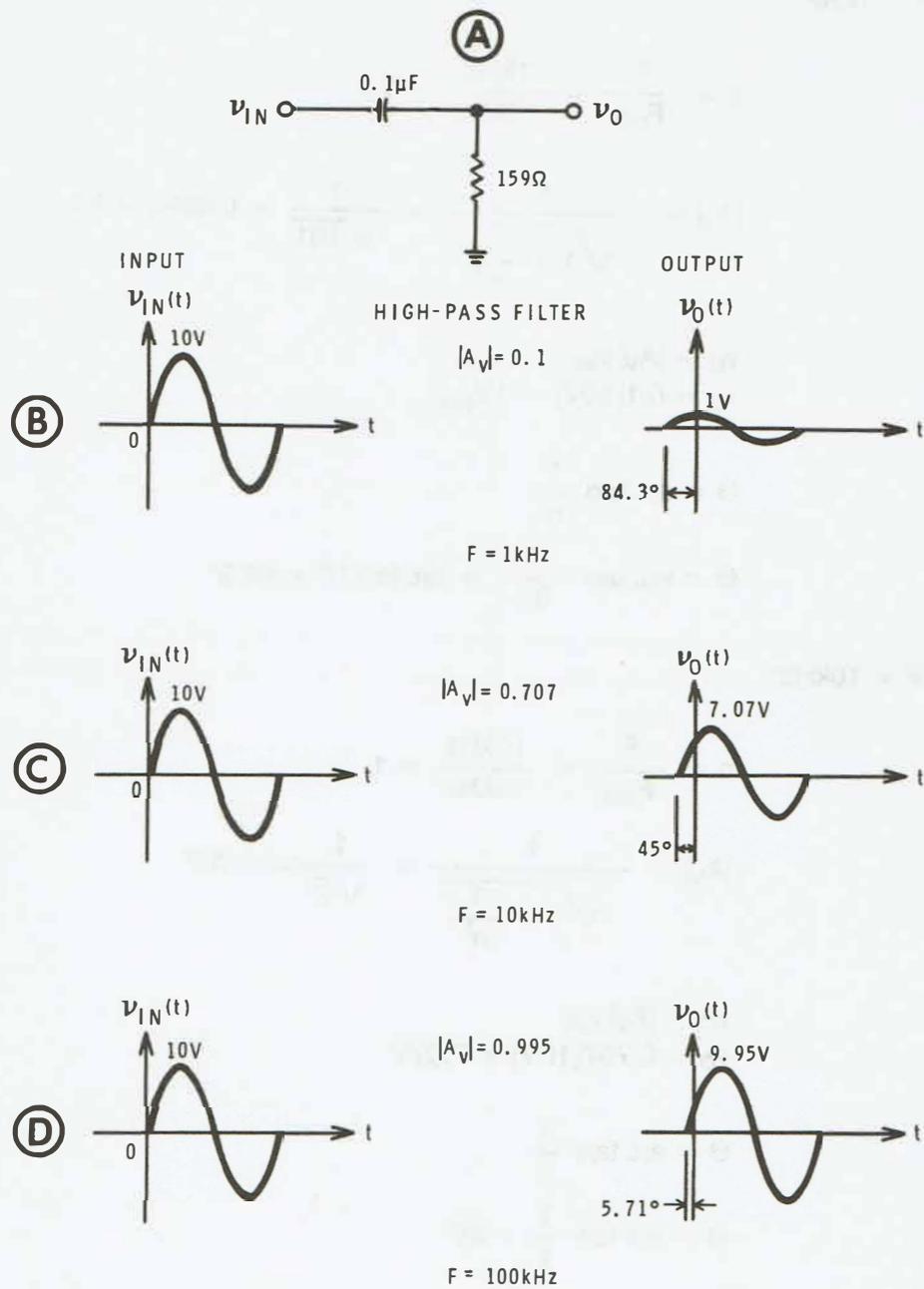


Figure 8-3

Input and output waveforms for Example 8-1.

- A. High-pass filter.
- B. $F = 1 \text{ kHz}$.
- C. $F = 10 \text{ kHz}$.
- D. $F = 100 \text{ kHz}$.

Finally, when $F = 100\text{kHz}$:

$$n = \frac{F}{F_{CO}} = \frac{100\text{kHz}}{10\text{kHz}} = 10$$

$$|A_V| = \frac{1}{\sqrt{1 + \frac{1}{n^2}}} = \frac{1}{\sqrt{1.01}} = 0.995$$

$$v_O = |A_V| v_{IN}$$

$$v_O = 0.995(10V) = 9.95V$$

$$\theta = \arctan \frac{1}{n}$$

$$\theta = \arctan \frac{1}{10} = 5.71^\circ$$

A sketch of the input and output voltages at 1kHz, 10kHz, and 100kHz are provided in Figure 8-3. Here, note that the output voltages agree with the sketches in Figure 8-2. Specifically:

1. Figure 8-2B and Figure 8-2C indicate that:

- (a) When $F \ll F_{CO}$, $|A_V| \ll 1$ and $\theta \approx 90^\circ$
- (b) When $F = F_{CO}$, $|A_V| = 0.707$ and $\theta = 45^\circ$
- (c) When $F \gg F_{CO}$, $|A_V| = 1$ and $\theta \approx 0^\circ$

2. In Figure 8-3 note that:

- (a) When $F = \frac{F_{CO}}{10}$, or 1kHz, $|A_V| = 0.1$ and $\theta = 84.3^\circ$
- (b) When $F = F_{CO}$, or 10kHz, $|A_V| = 0.707$ and $\theta = 45^\circ$
- (c) When $F = 10F_{CO}$, or 100kHz, $|A_V| = 0.995$ and $\theta = 5.71^\circ$

The Low-Pass Filter

A low-pass filter has characteristics that are just the opposite of a high-pass filter. Thus, a low-pass filter tends to pass signal frequencies that are below the filter's cutoff frequency, and attenuates those frequencies that are above the filter's cutoff frequency.

Figure 8-4A is an example of an elementary low-pass filter. Note that the output voltage is taken across the capacitor rather than the resistor. The high-pass filter and frequency domain circuit in Figure 8-4B can be analyzed to determine how voltage gain varies with frequency. Such an analysis results in the following equation for voltage gain:

$$A_v = \frac{1}{\sqrt{1 + n^2}} - L \text{ arc tan } n \quad (\text{Eq. 8-3})$$

$$\text{Where } n = \frac{F}{F_{CO}} = \omega RC$$

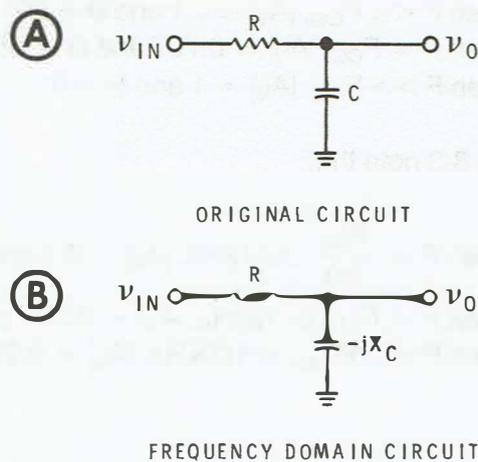


Figure 8-4

Low-pass filter.

- A. Original circuit.
- B. Frequency domain circuit.

Splitting equation 8-3 into two parts:

$$|A_v| = \frac{1}{\sqrt{1 + n^2}} \quad (\text{Eq. 8-3a})$$

$$-\alpha = \arctan n \quad (\text{Eq. 8-3b})$$

As before, the filter's cutoff frequency is given by:

$$F_{co} = \frac{1}{2\pi RC}$$

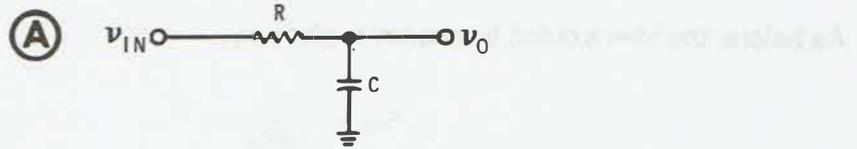
The various formulas for low-pass filters are summarized in Table 8-2.

Parameter	Formula
Voltage gain	$ A_v = \frac{1}{\sqrt{1 + n^2}}$
Phase angle	$-\alpha = \arctan n$
Cutoff frequency	$F_{\infty} = \frac{1}{2\pi RC}$
n	$n = \frac{F}{F_{\infty}} = \omega RC$

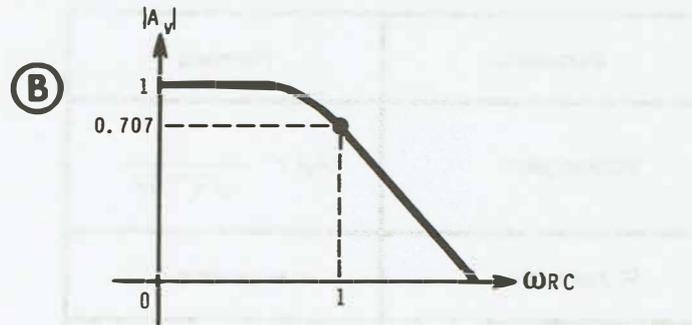
Table 8-2

Formulas For The Low-Pass RC Filter.

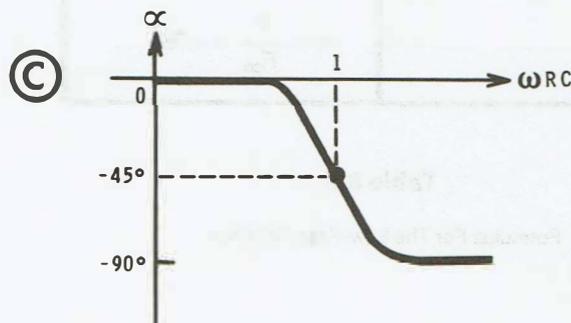
By substituting different values of n into Equation 8-3a and 8-3b, the necessary data is obtained to sketch the frequency response curves shown in Figure 8-5B and Figure 8-5C respectively. Comparing Figure 8-5 with Figure 8-2 illustrates the "opposite nature" of the low-pass and high-pass filters.



FILTER



VOLTAGE GAIN



PHASE ANGLE

Figure 8-5

Frequency response of the low-pass RC filter.

- A. Filter.
- B. Voltage gain.
- C. Phase angle.

Example 8-2

A low-pass RC filter has $C = 0.1\mu F$ and $R = 159\Omega$. Since these are the same component values used for the high-pass filter in Example 8-1, $F_{CO} = 10\text{kHz}$. Calculate the magnitude of the voltage gain and phase angle for $F = 1\text{kHz}$, 10kHz , and 100kHz .

Referring back to Table 8-2:

When $F = 1\text{kHz}$, $n = 0.1$

$$|A_V| = \frac{1}{\sqrt{1+n^2}} = \frac{1}{\sqrt{101}} = 0.995$$

$$-\alpha = \arctan n = \arctan 0.1$$

$$\alpha = -5.71^\circ$$

When $F = 10\text{kHz}$, $n = 1$

$$|A_V| = \frac{1}{\sqrt{1+n^2}} = \frac{1}{\sqrt{2}} = 0.707$$

$$-\alpha = \arctan n = \arctan 1$$

$$\alpha = -45^\circ$$

When $F = 100\text{kHz}$, $n = 10$

$$|A_V| = \frac{1}{\sqrt{1+n^2}} = \frac{1}{\sqrt{101}} = 0.1$$

$$-\alpha = \arctan n = \arctan 10$$

$$\alpha = -84.3^\circ$$

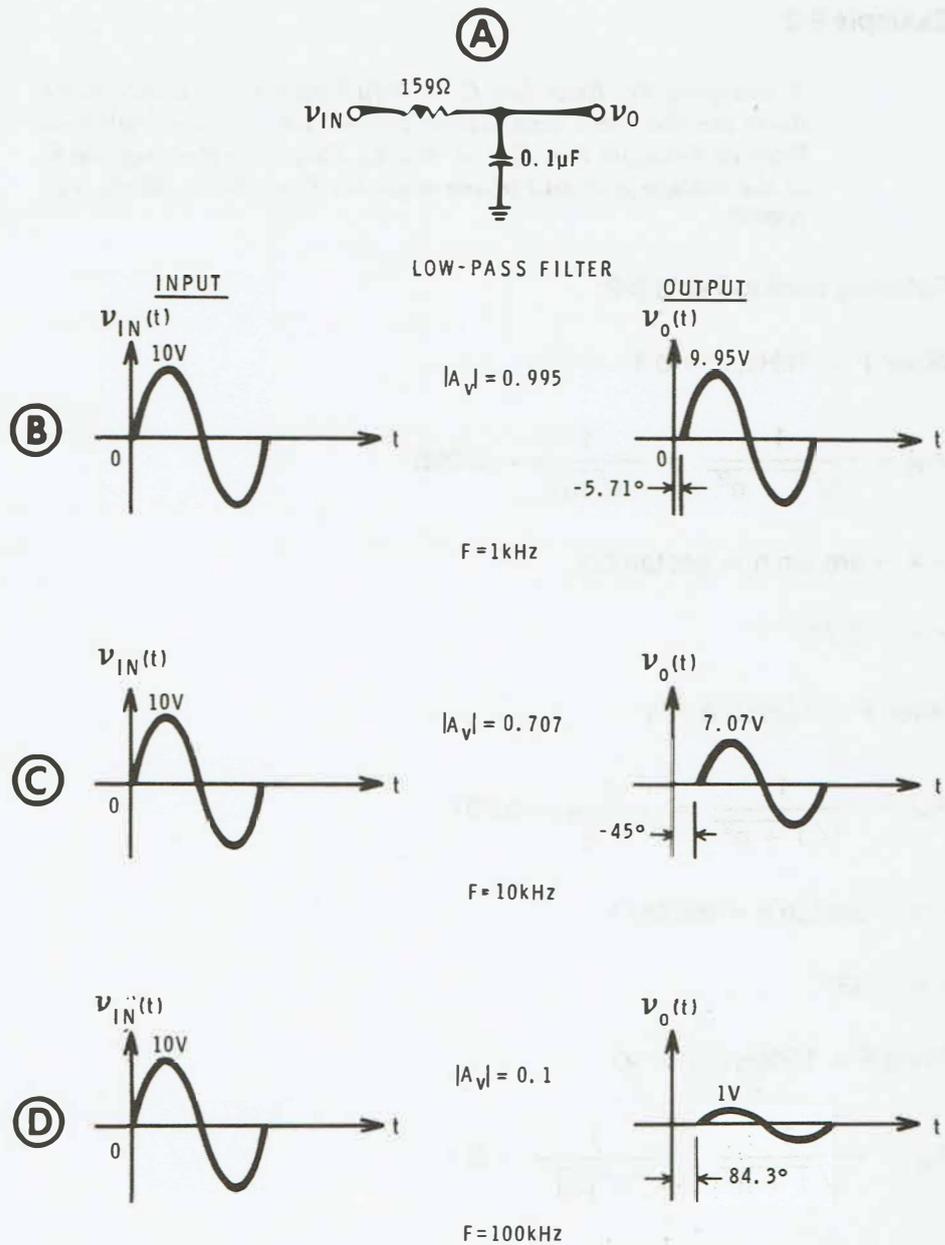


Figure 8-6

Input and output waveforms for Example 8-2.

- A. Low-pass filter.
- B. $F = 1\text{kHz}$.
- C. $F = 10\text{kHz}$.
- D. $F = 100\text{kHz}$.

Figure 8-6 is a sketch of the input and output voltages at 1kHz, 10kHz, and 100kHz. A comparison of these waveforms with those for the analogous high-pass filter in Figure 8-3, again illustrates the opposite nature of the two types of filters.

In both high-pass and low-pass filters, it is important to note that the output voltage differs from the input voltage in two respects. Specifically:

1. The amplitude of the output voltage is less than the amplitude of the input voltage.
2. The output voltage is out of phase with the input voltage.

Since the output voltage of a high-pass filter leads the input voltage, high-pass filters are sometimes referred to as **lead circuits**. Similarly, low-pass filters may be referred to as **lag circuits**, since the output voltage of a low-pass filter **lags** the input voltage.

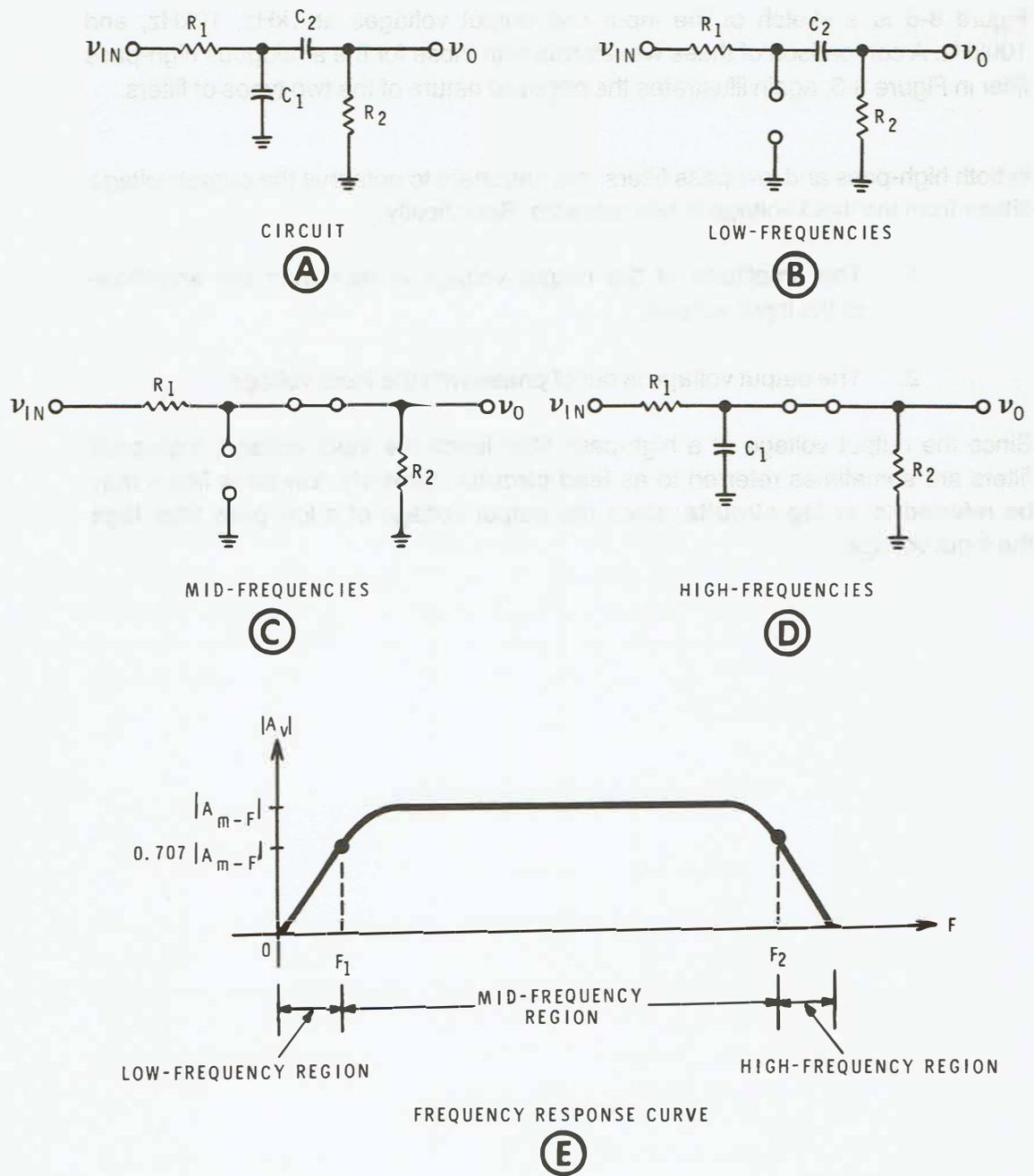


Figure 8-7

The bandpass filter.

- A. Circuit.
- B. Low frequencies.
- C. Medium frequencies.
- D. High frequencies.
- E. Frequency response curve.

The Bandpass Filter

By cascading a low-pass filter with a high-pass filter, you obtain the bandpass filter shown in Figure 8-7A. Here, it is assumed that $C_2 \gg C_1$, and $R_2 \gg R_1$. Typically, C_2 would have units of μF and C_1 units of pF .

With the previous restrictions in mind, the operation of the bandpass filter can be described as follows:

1. **Low Frequencies** — For low signal frequencies, the reactance of C_1 is so large that C_1 approximates an open circuit, as shown in Figure 8-7B. Here, the reactance of C_2 is on the same order of magnitude as R_2 . Consequently, C_2 must be included in the low-frequency model.
2. **Mid-Frequencies** — For medium signal frequencies, the reactance of C_1 is still large enough to neglect. In addition, the reactance of C_2 is small compared to R_2 . For these reasons, C_1 approximates an open circuit, and C_2 approximates a short circuit as shown in Figure 8-7C. Consequently, the magnitude of the mid-frequency voltage gain is:

$$|A_{M-F}| = \frac{R_2}{R_1 + R_2} \quad (\text{Eq. 8-4})$$

Since R_2 is assumed to be large compared to R_1 , $|A_{M-F}| \approx 1$.

3. **High Frequencies** — In this region, the reactance of C_2 is even less than in the mid frequency region. Consequently, C_2 approximates a short circuit. For high signal frequencies the reactance of C_1 has decreased to the point where C_1 can no longer be approximated by an open circuit. Therefore, C_1 must be included in the high-frequency model as shown in Figure 8-7D.

A sketch of the frequency response curve for the bandpass filter is provided in Figure 8-7E. The filter essentially passes signal frequencies that are greater than F_1 , but less than F_2 . The term **bandpass** (or **BW**) is the band of frequencies passed by the filter.

Stated mathematically:

$$\text{BW} = F_2 - F_1 \quad (\text{Eq. 8-5})$$

The frequencies F_2 and F_1 are usually referred to as the upper and lower cutoff frequencies respectively. Alternately, these frequencies may be referred to as corner, break, 3dB, or critical frequencies.

In Figure 8-7E note that the frequency response curve has been divided into three distinct regions. Furthermore, it is especially important to take note of the following:

1. For frequencies less than F_1 , the low-frequency region, the circuit acts like a high-pass filter, as shown in Figure 8-7B. The cutoff frequency of this high-pass filter determines the lower cutoff frequency of the bandpass filter. Neglecting R_1 , since $R_2 \gg R_1$, we note:

$$F_1 \approx \frac{1}{2\pi R_2 C_2} \quad (\text{Eq. 8-6})$$

2. For frequencies between F_1 and F_2 , the mid-frequency region, the circuit acts like the resistive voltage divider in Figure 8-7C.
3. For frequencies greater than F_2 , the high-frequency region, the circuit acts like the low-pass filter in Figure 8-7D. The cutoff frequency of this low-pass filter determines the upper cutoff frequency of the bandpass filter. Thus:

$$F_2 = \frac{1}{2\pi R_1 C_1} \quad (\text{Eq. 8-7})$$

Example 8-3

Calculate the cutoff frequencies for a bandpass filter that has the following component values. $R_1 = 10\text{k}\Omega$, $R_2 = 100\text{k}\Omega$, $C_1 = 40\text{pF}$, and $C_2 = 0.1\mu\text{F}$. Also estimate the mid-frequency voltage gain, and the voltage gain at the cutoff frequencies.

$$F_1 = \frac{1}{2\pi R_2 C_2} = \frac{0.159}{100\text{k}\Omega(0.1\mu\text{F})} = 15.9\text{Hz}$$

$$F_2 = \frac{1}{2\pi R_1 C_1} = \frac{0.159}{10\text{k}\Omega(40\text{pF})} = 397.5\text{kHz}$$

In the mid-frequency region:

$$|A_{M-F}| = \frac{R_2}{R_1 + R_2} = \frac{100\text{k}\Omega}{10\text{k}\Omega + 100\text{k}\Omega} = 0.909$$

Note that $|A_{M-F}| \approx 1$

At both F_1 and F_2 :

$$\begin{aligned} |A_V| &= 0.707|A_{M-F}| \\ |A_V| &= 0.707(0.909) = 0.643 \end{aligned}$$

The circuit and frequency response curve are illustrated in Figure 8-8A and Figure 8-8B respectively.

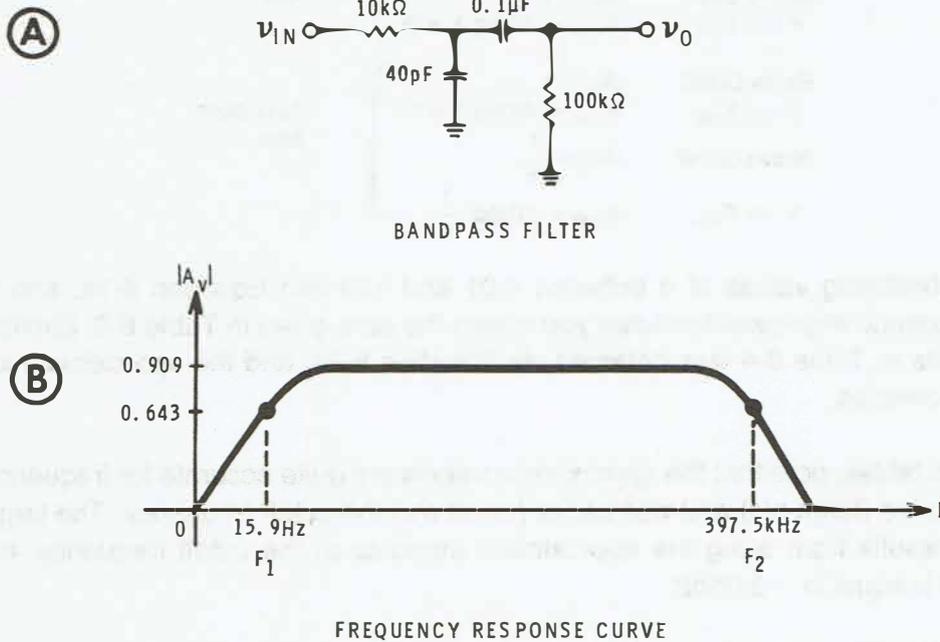


Figure 8-8

Circuit and frequency response curve for Example 8-3.

- A. Circuit.
- B. Frequency response curve.

Bode Plots

Curves of voltage-gain-versus-frequency are normally plotted on semilog paper. Furthermore, voltage gain is frequently expressed in units of decibels, dB. Recall that for a voltage ratio, the decibel voltage gain, A_{VdB} is:

$$A_{VdB} = 20 \log |A_V|$$

At any frequency, the magnitude of the voltage gain is given by Equation 8-1a (high-pass filter), and Equation 8-3a (low-pass filter). In each case, n is large for frequencies well above cutoff, and small for frequencies well below cutoff. Based on these observations, and an examination of Equation 8-1a and 8-3a, the following **approximate** formulas can be deduced:

Below Cutoff $F \ll F_{CO}$	$ A_V \approx n$ $A_{VdB} = 20 \log n$	}	High-pass filter
Above Cutoff $F \gg F_{CO}$	$ A_V \approx 1$ $A_{VdB} = 20 \log 1 = 0$		
Below Cutoff $F \ll F_{CO}$	$ A_V \approx 1$ $A_{VdB} = 20 \log 1 = 0$	}	Low-pass filter
Above Cutoff $F \gg F_{CO}$	$ A_V \approx \frac{1}{n}$ $A_{VdB} = 20 \log \frac{1}{n}$		

By substituting values of n between 0.01 and 100 into Equation 8-1a, and the approximate high-pass formulas you obtain the data given in Table 8-3. Similarly, the data in Table 8-4 was obtained via Equation 8-3a, and the approximate low-pass formulas.

In both tables, note that the approximate values are quite accurate for frequencies well above (large n 's) and well below (small n 's) the cutoff frequency. The largest error results from using the approximate formulas at the cutoff frequency, $n = 1$, and is equal to -3.01 dB.

A graph of decibel voltage-gain-versus-frequency, based on the approximate formulas, is called a **Bode plot**. Bode plots are popular because they are easy to sketch, and they provide a useful summary of a filter's characteristics.

n	$A_{v_{dB}}$ (Approximate)	$A_{v_{dB}}$ (Eq. 8-1a)
0.01	-40	-40
0.1	-20	-20.04
0.25	-12	-12.3
0.5	-6.02	-6.99
1	0	-3.01
2	0	-0.97
4	0	-0.26
10	0	-0.04
100	0	≈ 0

Table 8-3

High-Pass Filter Data

n	$A_{v_{dB}}$ (Approximate)	$A_{v_{dB}}$ (Eq. 8-3a)
0.01	0	≈ 0
0.1	0	-0.04
0.25	0	-0.26
0.5	0	-0.97
1	0	-3.01
2	-6.02	-6.99
4	-12	-12.3
10	-20	-20.04
100	-40	-40

Table 8-4

Low-Pass Filter Data

In Table 8-3 and Table 8-4, notice that when the frequency changes by a factor of 2 (an octave), the dB gain changes by approximately 6dB. Similarly, when the frequency changes by a factor of 10 (a decade), the dB gain changes by approximately 20. Consequently, the Bode plots for the high-pass, low-pass, and bandpass RC filters appear as shown in Figure 8-9.

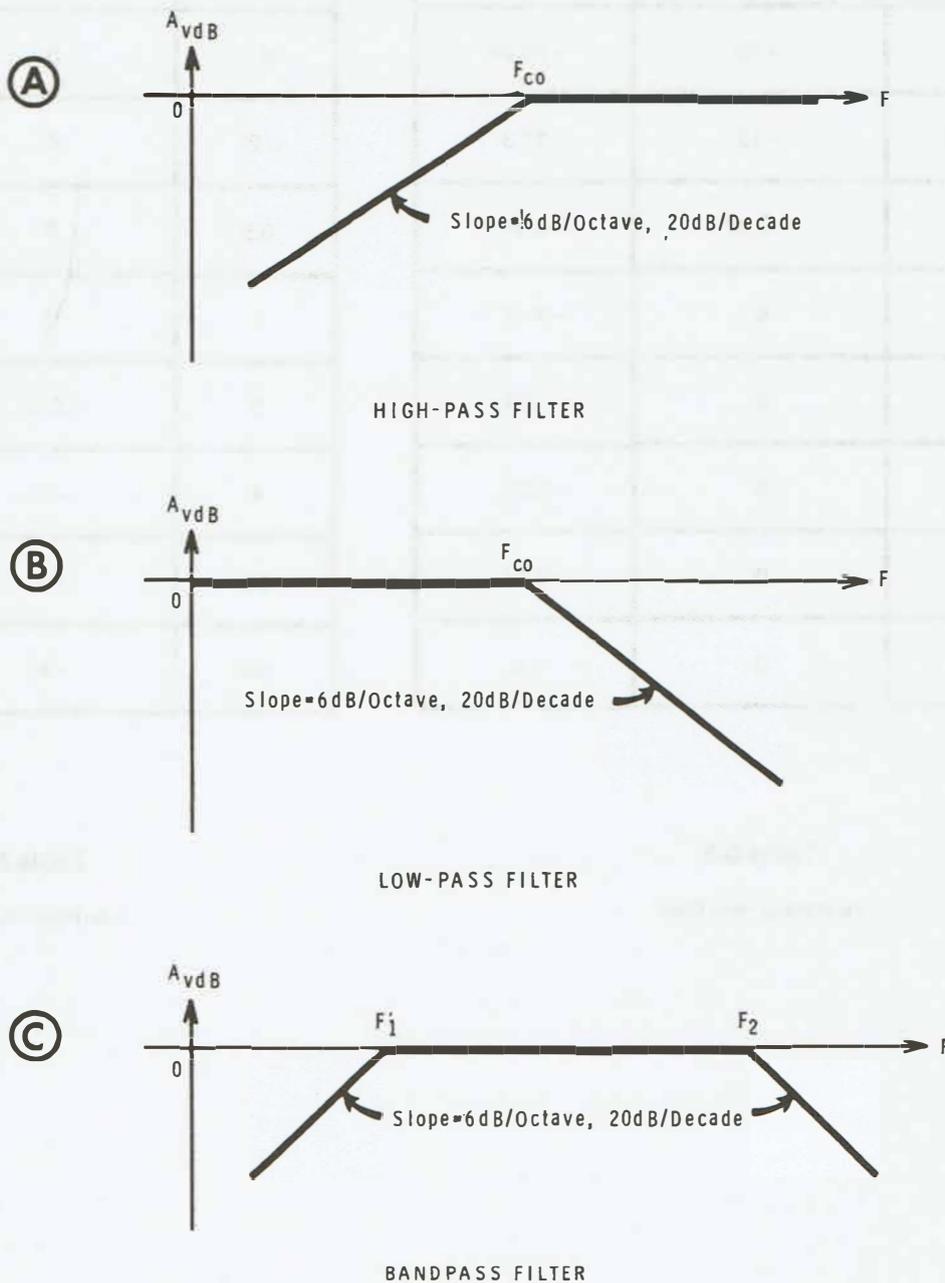


Figure 8-9

- Filter Bode plots.
- A. High-pass filter.
 - B. Low-pass filter.
 - C. Bandpass filter.

Example 8-4

The bandpass filter in Example 8-3 had:

$$F_1 = 15.9\text{Hz}, F_2 = 397.5\text{kHz}, \text{ and } |A_{M-F}| \approx 1.$$

- Use Equation 8-1a to calculate the voltage gain for $F = F_1/8$ or 1.9875Hz .
- Use Equation 8-3a to calculate the voltage gain at $F = 20F_2$ or 7.95MHz .
- Convert the voltage gains calculated in (a) and (b) to dB notation.
- Sketch a Bode plot for the filter.

Based on the 6dB/octave, 20dB/decade rolloff, estimate the dB voltage gain at 1.9875Hz and 7.95MHz.

$$(a) \quad n = \frac{F}{F_1} = \frac{1.9875\text{Hz}}{15.9\text{Hz}} = 0.125$$

$$|A_V| = \frac{1}{\sqrt{1 + \frac{1}{n^2}}} = \frac{1}{\sqrt{1 + 64}} = 0.124$$

$$(b) \quad n = \frac{F}{F_2} = \frac{7.95\text{MHz}}{397.5\text{kHz}} = 20$$

$$|A_V| = \frac{1}{\sqrt{1 + n^2}} = \frac{1}{\sqrt{401}} = 0.0499$$

$$(c) \quad \begin{aligned} A_{VdB} &= 20 \log |A_V| \\ A_{VdB} &= 20 \log 0.124 = -18.13\text{dB when } F = 1.9875\text{Hz} \\ A_{VdB} &= 20 \log |A_V| \\ A_{VdB} &= 20 \log 0.0499 = -26.04\text{dB when } F = 7.95\text{MHz} \end{aligned}$$

Steps (a) through (c) illustrate how you can calculate the theoretically exact value of dB voltage gain in the low and high frequency regions. Step (d) illustrates the simplicity of the approximate Bode plot approach.

- (d) Below F_1 or above F_2 , the dB voltage gain changes by 6dB each time the frequency changes by a factor of 2. Similarly, the dB voltage gain changes by 20dB each time the frequency changes by a factor of 10. Thus when:

$$\begin{array}{ll} F = F_1 & A_{v\text{dB}} \approx 0 \\ F = F_1 \div 2 & A_{v\text{dB}} \approx -6\text{dB} \\ F = F_1 \div 4 & A_{v\text{dB}} \approx -12\text{dB} \\ F = F_1 \div 8 & A_{v\text{dB}} \approx -18\text{dB} \end{array}$$

Since 1.9875Hz equals $F_1 \div 8$, $A_{v\text{dB}} \approx -18\text{dB}$

When:

$$\begin{array}{ll} F = F_2 & A_{v\text{dB}} \approx 0 \\ F = 2F_2 & A_{v\text{dB}} \approx -6\text{dB} \\ F = 20F_2 & A_{v\text{dB}} \approx -6\text{dB} + (-20\text{dB}) = -26\text{dB} \end{array}$$

Since 7.95MHz equals $20F_2$, $A_{v\text{dB}} \approx -26\text{dB}$.

Note that the approximate values are close to the "exact" values. A sketch of the filter's Bode plot is shown in Figure 8-10.

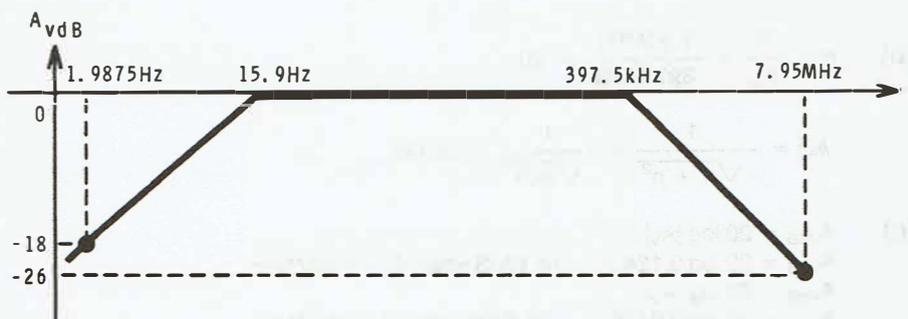


Figure 8-10

Bode plot for Example 8-4.

Self-Test Review

1. The output voltage from a filter differs from the input voltage in both amplitude and _____.
2. The output voltage from a high-pass filter _____ the input voltage.
leads/lags
3. The output voltage from a low-pass filter _____ the input voltage.
leads/lags
4. For frequencies well above F_{CO} the dB voltage gain of a high-pass filter is approximately _____dB.
5. For frequencies well below cutoff, the dB voltage gain of a low-pass filter is approximately _____dB.
6. In the bandpass filter, F_1 is determined by the cutoff frequency of the _____ filter.
low-pass/high-pass
7. In the bandpass filter, F_2 is determined by the cutoff frequency of the _____ filter.
low-pass/high-pass

Refer to Figure 8-11 for questions 8 through 12.

8. The circuit's lower cutoff frequency is approximately _____Hz.
9. The circuit's upper cutoff frequency is approximately _____MHz.
10. At $F = 8.83\text{MHz}$, the approximate dB voltage gain is _____dB.
11. At $F = 100\text{kHz}$, the approximate dB voltage gain is _____dB.
12. At $F = F_1$, the output voltage will _____ the input voltage by 45° .
lead/lag

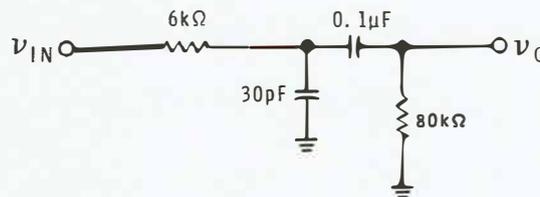


Figure 8-11

Circuit for Self-Test Review questions 8-12.

Answers

- | | |
|--------------|-------------|
| 1. phase | 7. low-pass |
| 2. leads | 8. 19.875Hz |
| 3. lags | 9. 0.883MHz |
| 4. 0 | 10. -20dB |
| 5. 0 | 11. 0dB |
| 6. high-pass | 12. lead |

Solutions to questions 8-12 follow:

$$8. \quad F_1 = \frac{1}{2\pi R_2 C_2} = \frac{0.159}{80\text{k}\Omega(0.1\mu\text{F})} = 19.875\text{Hz}.$$

$$9. \quad F_2 = \frac{1}{2\pi R_1 C_1} = \frac{0.159}{6\text{k}\Omega(30\text{pF})} = 0.883\text{MHz}.$$

10. 8.83MHz is one decade above F_2 . The dB voltage gain decreases by 20dB/decade. Thus $A_{\text{vdB}} = -20\text{dB}$.
11. 100kHz is between F_1 and F_2 . In this "passband" region, $A_{\text{v}} \approx 1$ and $A_{\text{vdB}} \approx 0$.
12. For frequencies less than F_1 , the bandpass filter acts like a high-pass filter, as shown in Figure 8-7B. For this reason, the output voltage **leads** the input voltage.

RC-COUPLED AMPLIFIER FREQUENCY RESPONSE

In conjunction with numerous circuit resistances, the various capacitances in an amplifier form a number of high-pass and low-pass RC filters. Collectively, these filters produce an overall frequency response that is similar to that of a bandpass filter. In the following sections, you will learn how to identify the individual RC filter sections. By analyzing these filters, you will be able to predict the overall frequency response that is characteristic of a given amplifier.

Coupling Capacitors

It is important to realize that the AC equivalent circuits in Units 1 through 7 are valid only for mid-frequency operation. In these circuits, coupling and bypass capacitors were assumed to approximate AC short circuits. Specifically, the component values were selected so that the following inequalities were satisfied at the lowest signal frequency, F_1 .

$$\begin{aligned} |X_{C_1}| &<< R_{IN} \\ |X_{C_2}| &<< R_L \end{aligned}$$

For signal frequencies less than F_1 , it is clear that the previous inequalities are no longer satisfied. For this reason, both C_1 and C_2 must be included in the low-frequency equivalent circuit.

The common-emitter amplifier shown in Figure 8-12A illustrates this concept. Note that the effective load seen by the signal source, v_{IN} , consists of the series combination of C_1 and the amplifier's input resistance, R_{IN} , as shown in Figure 8-12B.

Clearly, R_S , C_1 , and R_{IN} constitute a high-pass RC filter. In a typical amplifier, R_{IN} may not be 10 or more times larger than R_S . For this reason, the value of R_S is taken into account when calculating the cutoff frequency of the high-pass base filter. Specifically:

$$F_{b_1} = \frac{1}{2\pi(R_S + R_{IN})C_1} \quad (\text{Eq. 8-8})$$

Where F_{b_1} = cutoff frequency of the high-pass base filter.

$$R_{IN} = R_1 \parallel R_2 \parallel h_{fe}(R_E + r_e')$$

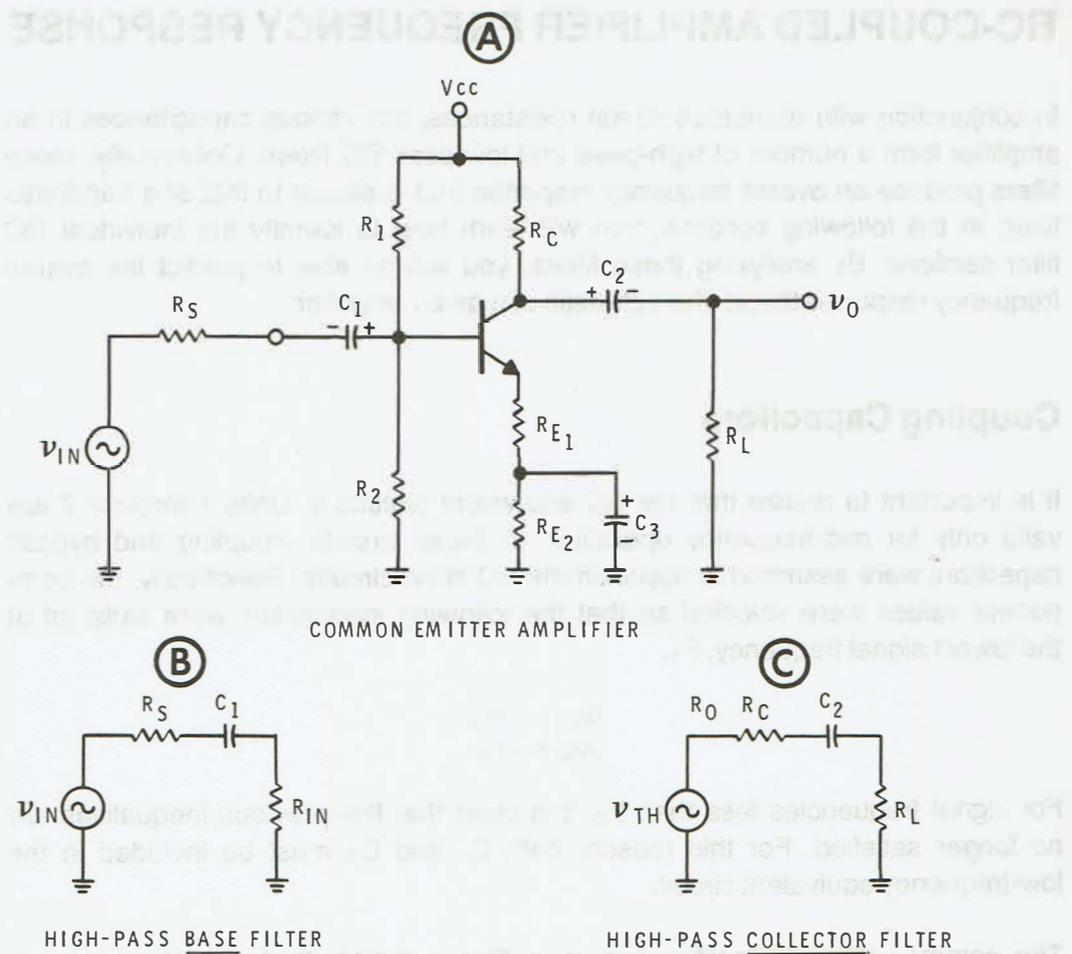


Figure 8-12

High-pass filters due to the use of coupling capacitors.

- A. Common-emitter amplifier.
- B. High-pass **base** filter.
- C. High-pass **collector** filter.

By “looking back” into the amplifier in Figure 8-12A, from the collector terminal, you can visualize a Thevenin equivalent circuit consisting of a Thevenin voltage source, v_{TH} , in series with the amplifier’s output resistance, R_O . This Thevenin equivalent circuit drives the series combination of C_2 and R_L as shown in Figure 8-12C. R_C , C_2 , and R_L constitute a second high-pass RC filter. In this case, the filter’s cutoff frequency is given by:

$$F_{C_1} = \frac{1}{2\pi(R_C + R_L)C_2} \quad (\text{Eq. 8-9})$$

Where F_{C_1} = cutoff frequency of the high-pass collector filter.

Bypass Capacitor

In addition to the coupling capacitors, C_1 and C_2 , the emitter bypass capacitor, C_3 , must also be considered in the low-frequency region.

To begin, let's consider the bypass circuit shown in Figure 8-13A. In the mid-frequency region, $|X_{C_3}|$ is small compared to the value of R_{E_2} . For this reason, C_3 approximates a short circuit as shown in Figure 8-13B. Note that the impedance between point A and ground is essentially 0Ω . Also, recall that for mid-frequency operation, the AC emitter current and voltage gain are:

$$\left. \begin{aligned} i_e \approx i_c &= \frac{v_{IN}}{R_{E_1} + r_e'} \\ A_v &= \frac{-r_L}{R_{E_1} + r_e'} \end{aligned} \right\} \text{Mid-frequency operation}$$

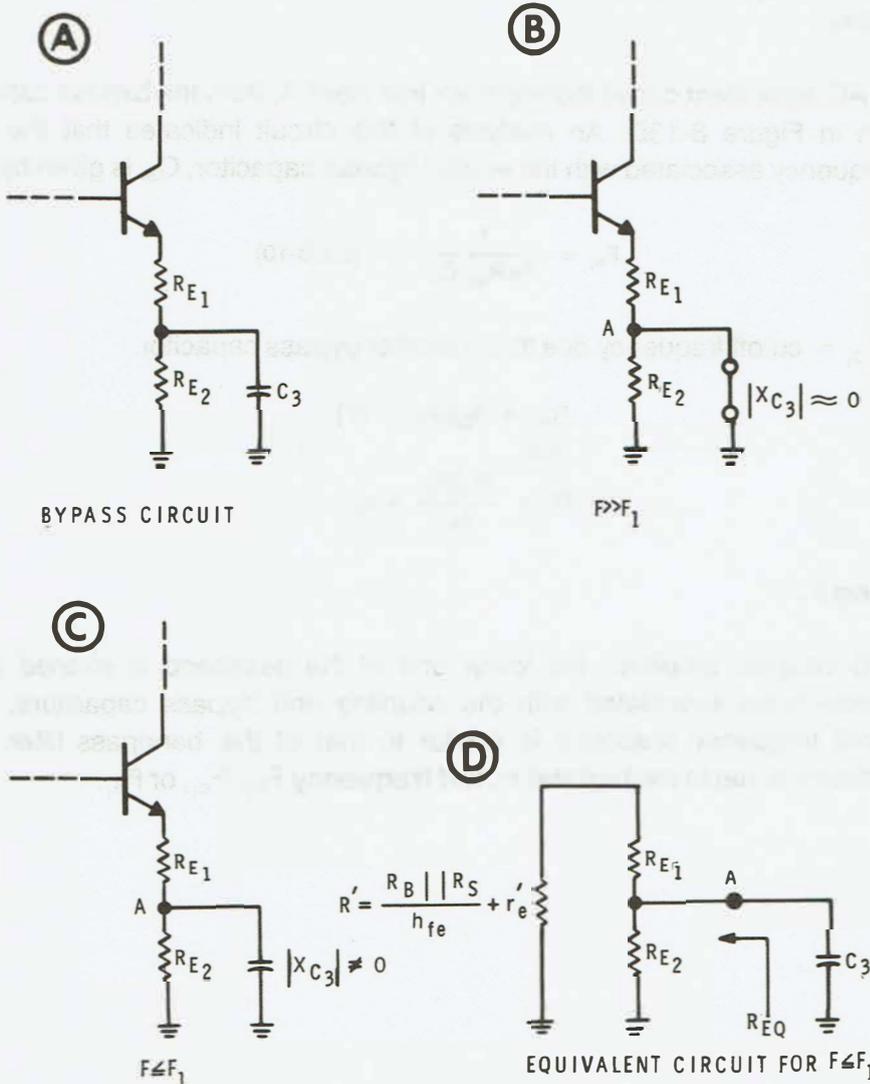


Figure 8-13

- The emitter bypass capacitor.
- A. Bypass circuit.
 - B. $F \gg F_1$.
 - C. $F \leq F_1$.
 - D. Equivalent circuit for $F \leq F_1$.

For signal frequencies less than F_1 , $|X_{C_3}|$ is no longer small compared to the value of R_{E_2} . For this reason, C_3 no longer approximates a short circuit, as shown in Figure 8-13C. Consequently, the impedance between point A and ground now equals $R_{E_2} \parallel X_{C_3}$. Since the effective impedance in the emitter branch has increased, the AC emitter current decreases. The decreased emitter current results in a decreased voltage gain. Specifically:

$$i_e = i_C = \frac{v_{IN}}{R_{E_1} + r_{e'} + Z_A}$$

$$A_V = \frac{-r_L}{R_{E_1} + r_{e'} + Z_A}$$

Where $Z_A = R_{E_2} \parallel X_{C_3}$

Comparing the low- and mid-frequency equations, it is obvious that the presence of the emitter bypass capacitor results in a decreased voltage gain at low signal frequencies.

A useful AC equivalent circuit looking back into point A, from the bypass capacitor, is shown in Figure 8-13D. An analysis of this circuit indicates that the lower cutoff frequency associated with the emitter bypass capacitor, C_3 , is given by:

$$F_{e_1} = \frac{1}{2\pi R_{eq} C_3} \quad (\text{Eq. 8-10})$$

Where F_{e_1} = cutoff frequency due to the emitter bypass capacitor.

$$R_{eq} = R_{E_2} \parallel (R_{E_1} + R')$$

and

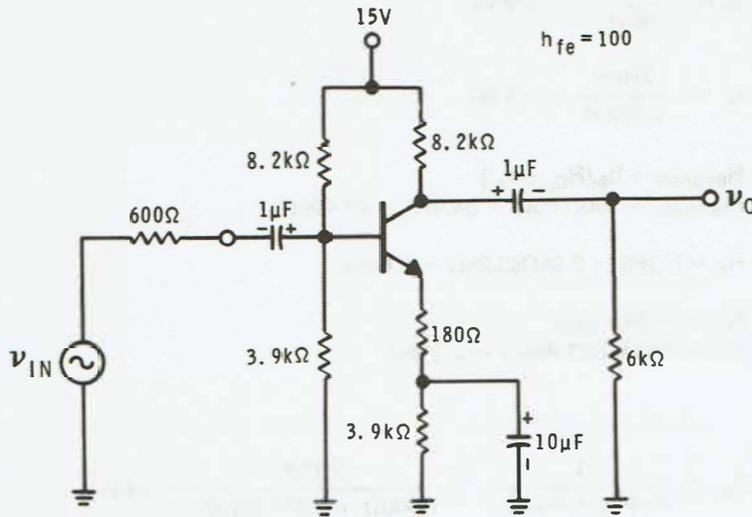
$$R' = \frac{R_B \parallel R_S}{h_{fe}} + r_{e'}$$

Predicting F_1

In an RC coupled amplifier, the lower end of the passband is shaped by the cutoff frequencies associated with the coupling and bypass capacitors. Since the overall frequency response is similar to that of the bandpass filter, F_1 is approximately equal to the **highest cutoff frequency** F_{b_1} , F_{c_1} , or F_{e_1} .

Example 8-5

Estimate the lower cutoff frequency, F_1 , for the common-emitter amplifier shown in Figure 8-14. What is the approximate voltage gain at this frequency?

**Figure 8-14**

Circuit for Example 8-5.

In order to calculate F_{b_1} , you must first calculate the value of R_{IN} . Thus:

$$V_B = \frac{15V(3.9k\Omega)}{8.2k\Omega + 3.9k\Omega} = 4.83V$$

$$V_E = 4.83V - 0.7V = 4.13V$$

$$I_E = \frac{4.13V}{3.9k\Omega} = 1.06mA$$

$$r_{e'} = \frac{37mV}{1.06mA} = 34.9\Omega$$

$$R_{IN\ BASE} = h_{fe}(R_{E_1} + r_{e'})$$

$$R_{IN\ BASE} = 100(180\Omega + 34.9\Omega) = 21.49k\Omega$$

$$R_B = R_1 \parallel R_2 = 3.9k\Omega \parallel 8.2k\Omega = 2.64k\Omega$$

$$R_{IN} = R_B \parallel R_{IN\ BASE}$$

$$R_{IN} = 2.64k\Omega \parallel 21.49k\Omega = 2.31k\Omega$$

Now:

$$F_{b_1} = \frac{1}{2\pi(R_S + R_{IN})C_1} = \frac{0.159}{(600\Omega + 2.31k\Omega)1\mu F} = 54.6Hz$$

$$F_{c_1} = \frac{1}{2\pi(R_C + R_L)C_2} = \frac{0.159}{(8.2k\Omega + 6k\Omega)1\mu F} = 11.2Hz$$

You can calculate F_{e_1} as follows:

$$R' = \frac{R_B \parallel R_S}{h_{fe}} + r_{e'}$$

$$R' = \frac{2.64k\Omega \parallel 600\Omega}{100} + 34.9\Omega$$

$$R' = \frac{488.8\Omega}{100} + 34.9\Omega \approx 39.8\Omega$$

$$(R_{E_1} + R') = 180\Omega + 39.8\Omega = 219.8\Omega$$

$$R_{eq.} = R_{E_2} \parallel (R_{E_1} + R')$$

$$R_{eq.} = 3.9k\Omega \parallel 219.8\Omega \approx 208.1\Omega$$

Now:

$$F_{e_1} = \frac{1}{2\pi R_{eq.} C_3} = \frac{0.159}{208.1\Omega(10\mu F)} = 76.4Hz$$

Since F_{e_1} is higher than F_{b_1} and F_{c_1} , the circuit's lower cutoff frequency, $F_1 \approx F_{e_1}$, or 76.4Hz.

At F_1 the voltage gain is 0.707 times the mid-frequency value. Thus:

$$A_{V_{M-F}} = \frac{-r_L}{R_{E_1} + r_{e'}} = \frac{8.2\text{k}\Omega \parallel 6\text{k}\Omega}{180\Omega + 34.9\Omega} = \frac{-3.46\text{k}\Omega}{214.9\Omega} = -16.1$$

$$A_{V_1} = 0.707 A_{V_{M-F}} = 0.707(-16.1) = -11.38$$

Example 8-6

Estimate F_1 in Figure 8-14 assuming C_3 is changed from $10\mu\text{F}$ to $100\mu\text{F}$.

The values of F_{b_1} and F_{c_1} are the same as in Example 8-5. Thus:

$$F_{b_1} = 54.6\text{Hz} \text{ and } F_{c_1} = 11.2\text{Hz}$$

Similarly, the value of R_{eq} is 208.1Ω . Therefore, the new value of F_{e_1} is:

$$F_{e_1} = \frac{1}{2\pi R_{eq} C_3} = \frac{1}{208.1\Omega(100\mu\text{F})} \approx 7.64\text{Hz}$$

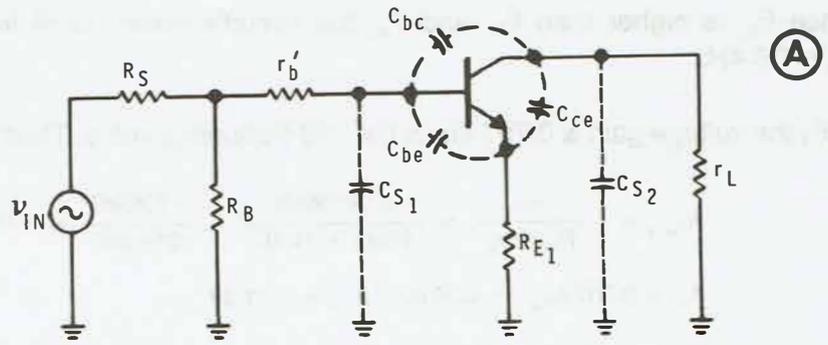
In this case, F_{b_1} is higher than either F_{c_1} or F_{e_1} . Therefore, $F_1 \approx F_{b_1} = 54.6\text{Hz}$.

High-Frequency Effects

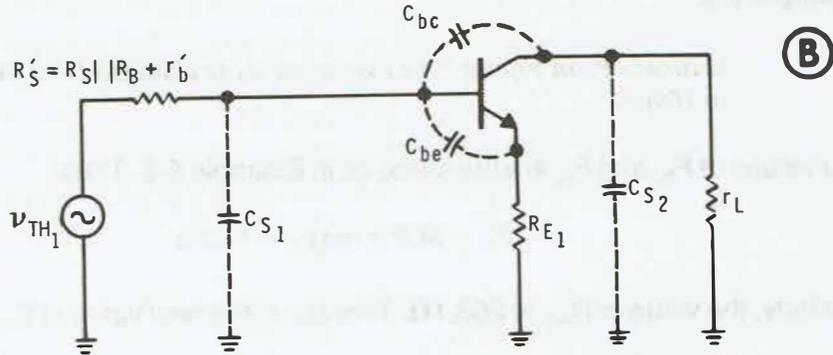
Coupling and bypass capacitors have little effect on the high frequency response of an amplifier because they approximate short circuits for frequencies greater than F_1 .

Internal characteristics and stray capacitances are always present in real circuits. Typically, these capacitances have values in the pF range. At low and mid-frequencies, these capacitances can be neglected, since their reactances are very large when compared to the resistance values in a typical amplifier. Internal device and stray capacitances are effectively open circuits in the low- and mid-frequency regions.

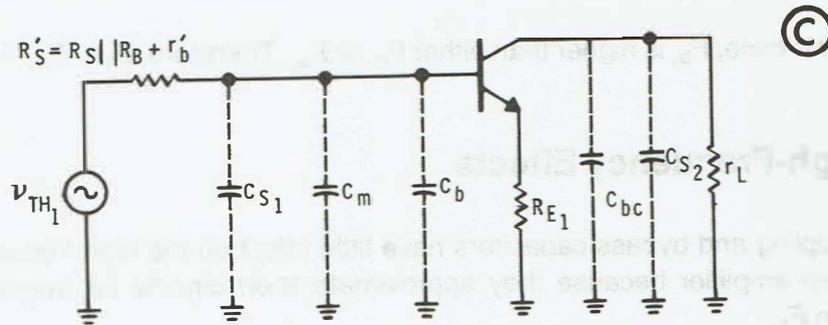
Capacitive reactance decreases as frequency increases. In the high-frequency region, the reactances of the internal device and stray capacitances have decreased to the point where they no longer approximate open circuits. Thus they are included in the high-frequency equivalent circuit.



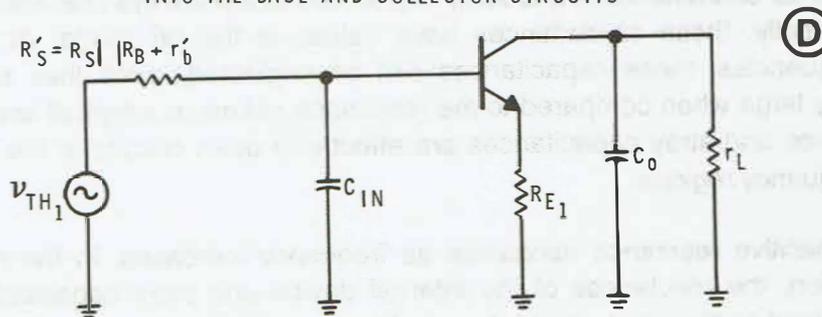
HIGH-FREQUENCY AC EQUIVALENT CIRCUIT



THEVENIZING THE INPUT CIRCUIT, AND REMOVING C_{ce}



REFLECTING APPROPRIATE CAPACITORS INTO THE BASE AND COLLECTOR CIRCUITS



COMBINING CAPACITORS

Figure 8-15

Development of a high-frequency equivalent circuit for the common-emitter voltage amplifier.

- A. High-frequency AC equivalent circuit.
- B. Thevenizing the input circuit, and removing C_{ce} .
- C. Reflecting appropriate capacitors into the base and collector circuits.
- D. Combining capacitors.

Simplified High-Frequency Model

To develop a theoretically exact high-frequency model, you would need equations that are quite complex. Furthermore, in practice, many of the parameter values in the “exact” equations are rarely known. For these reasons, we will develop a simplified high-frequency model that retains enough features of the exact model to be an equivalent circuit.

Our starting point is the high-frequency equivalent circuit shown in Figure 8-15A. Here, note that the various terminal-to-terminal BJT capacitances are included, as well as the stray capacitances, C_{s_1} , and C_{s_2} . Also note that the base spreading resistance, r_b' , is included since at high frequencies r_b' is often significant.

By Thevenizing the circuit in Figure 8-15A to the left of C_{s_1} , you obtain the circuit shown in Figure 8-15B. Since the capacitance, C_{ce} , is typically small compared to the other capacitance values, it has been removed from the circuit in Figure 8-15B.

Recall that in Unit 3, we employed Miller's theorem to simplify the analysis of collector feedback circuits. In Figure 8-15B, C_{bc} is connected between the input and output terminals, which is analogous to R_B in a collector feedback circuit. For this reason, C_{bc} can, via Miller's theorem, be “reflected” into the base and collector circuits as shown in Figure 8-15C. Here:

$$C_m = C_{bc}(A_v + 1) \quad (\text{Eq. 8-11})$$

Similarly, the capacitance reflected into the collector circuit is:

$$C = \frac{C_{bc}(A_v)}{A_v + 1} \approx C_{bc} \quad (\text{Eq. 8-12})$$

Where A_v is the **magnitude** of the common-emitter voltage gain.

Notice in Figure 8-15C that C_{be} has been replaced by C_b . With an advanced derivation, it's possible to show that C_b is approximated by:

$$C_b \approx C_{be} \left[1 - \frac{R_{E_1}}{R_{E_1} + r_e'} \right] \quad (\text{Eq. 8-13})$$

Equation 8-13 indicates that in a fully bypassed circuit, ($R_{E_1} = 0$). $C_b = C_{be}$. In many cases, C_b is neglected since C_b is typically small compared to C_{s_1} and C_m .

By combining the parallel capacitance in Figure 8-15C, you obtain the equivalent circuit shown in Figure 8-15D. Here:

$$C_{IN} = C_{s_1} + C_m + C_b \quad (\text{Eq. 8-14})$$

$$C_O = C_{bc} + C_{s_2} \quad (\text{Eq. 8-15})$$

The circuit in Figure 8-15D contains two low-pass RC filters that determine the amplifier's upper cutoff frequency, F_2 . In order to "see" these filters, it is necessary to replace the BJT with its AC model as shown in Figure 8-16A. Finally, by Thevenizing the left half of the circuit and converting the current source to a voltage source in the right side of the circuit, you obtain the base and collector low-pass RC filters shown in Figure 8-16B. The cutoff frequency of each filter is given by:

$$F_{b_2} = \frac{1}{2\pi(R_S' \parallel R_{IN(BASE)})C_{IN}} \quad (\text{Eq. 8-16})$$

Where

$$R_S' = R_S \parallel R_B + r_b'$$

$$R_{IN(BASE)} = h_{fe}(R_{E_1} + r_e')$$

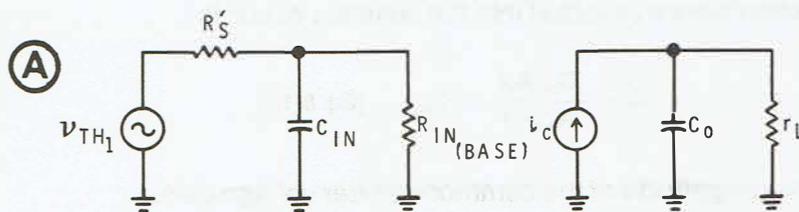
$$C_{IN} = C_{s_1} + C_m + C_b$$

$$F_{c_2} = \frac{1}{2\pi r_L C_O} \quad (\text{Eq. 8-17})$$

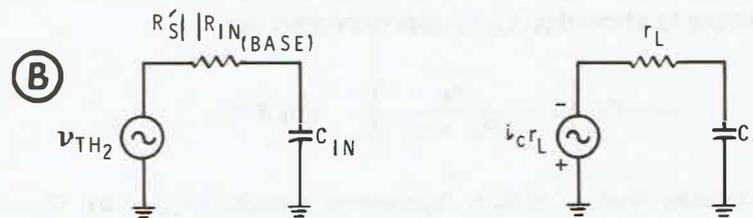
Where

$$r_L = R_C \parallel R_L$$

$$C_O = C_{bc} + C_{s_2}$$



REPLACING THE BJT IN FIGURE 8-15D WITH IT'S AC MODEL



LOW-PASS BASE AND COLLECTOR FILTERS

Figure 8-16

Low-pass filters due to internal BJT, and external stray capacitances.

- A. Replacing the BJT in Figure 8-15D with it's AC model.
- B. Low-pass base and collector filters.

PREDICTING F_2

The high end of the passband in an RC-coupled amplifier is determined by the cutoff frequencies associated with C_{IN} and C_O . Specifically, F_2 approximately equals the **lower** of the two cutoff frequencies, F_{b_2} or F_{c_2} .

Example 8-7

*The amplifier in Figure 8-14 was partially analyzed earlier.
Recall that:*

$$\begin{array}{ll} R_B = 2.64\text{k}\Omega & r_L = 3.46\text{k}\Omega \\ R_{IN\text{ BASE}} = 21.49\text{k}\Omega & r_e' = 34.9\Omega \\ R_S = 600\Omega & A_{V_{M-F}} = -16.1 \end{array}$$

Work out the approximate value of F_2 assuming:

$$\begin{array}{ll} C_{s_1} = 25\text{pF} & C_{be} = 150\text{pF} \\ C_{bc} = 6\text{pF} & C_{s_2} = 5\text{pF} \\ r_b' = 175\Omega & \end{array}$$

First calculate

$$\begin{aligned} R_S' &= R_S \parallel R_B + r_b' \\ R_S' &= 600\Omega \parallel 2.64\text{k}\Omega + 175\Omega \\ R_S' &= 488.8\Omega + 175\Omega = 663.8\Omega \\ R_S' \parallel R_{IN\text{ BASE}} &= 663.8\Omega \parallel 21.49\text{k}\Omega = 643.9\Omega \end{aligned}$$

$$\begin{aligned} C_m &= C_{bc}(A_V + 1) \\ C_m &= 6\text{pF}(16.1 + 1) = 102.6\text{pF} \end{aligned}$$

$$C_b = C_{be} \left[1 - \frac{R_{E_1}}{R_{E_1} + r_e'} \right]$$

$$C_b = 150\text{pF} \left[1 - \frac{180\Omega}{180\Omega + 34.9\Omega} \right]$$

$$C_b = 150\text{pF}(0.162) = 24.36\text{pF}$$

$$\begin{aligned} C_{IN} &= C_{s_1} + C_m + C_b \\ C_{IN} &= 25\text{pF} + 102.6\text{pF} + 24.36\text{pF} \\ C_{IN} &= 151.96\text{pF} \end{aligned}$$

Thus:

$$F_{b_2} = \frac{1}{2\pi(R_S \parallel R_{IN \text{ BASE}})C_{IN}}$$

$$F_{b_2} = \frac{0.159}{643.9\Omega(151.96\text{pF})} = 1.6\text{MHz}$$

Next calculate F_{c_2} :

$$C_O = C_{bc} + C_{s_2}$$

$$C_O = 6\text{pF} + 5\text{pF} = 11\text{pF}$$

$$F_{c_2} = \frac{1}{2\pi r_L C_O} = \frac{0.159}{3.46\text{k}\Omega(11\text{pF})} = 4.17\text{MHz}$$

Since $F_{b_2} < F_{c_2}$, $F_2 \approx F_{b_2} \approx 1.6\text{MHz}$

High-Frequency BJT Parameters

As frequency increases, the current gain of a transistor decreases. For this reason, one or more of the following parameters are normally provided on a BJT's data sheet.

ALPHA CUTOFF FREQUENCY

When the time of one cycle or period of the AC input signal approaches the time required for charge carriers to pass through a transistor, the current gain of the transistor drops rapidly. The frequency at which α decreases to 70.7% of its low frequency value is called the alpha cutoff frequency, $F_1\alpha$.

The value of $F_2\alpha$ is often determined by measuring α at a reference frequency of 1kHz and then increasing the frequency until α again drops to 70.7% of the 1kHz reference. $F_2\alpha$ is an important characteristic of common-base circuits since it indicates an upper frequency limit for common-base operation.

BETA CUTOFF FREQUENCY

At high frequencies, the current gain of a transistor in a common-emitter circuit (B) also decreases. The frequency at which B decreases to 70.7% of its low-frequency value is called the beta cutoff frequency, F_{1B} . Since B imposes an upper frequency limit for a transistor used in a common-emitter configuration, it is an important high frequency parameter.

CURRENT-GAIN BANDWIDTH PRODUCT

Another way of expressing the inherent frequency response limitation of a transistor is to provide its current-gain bandwidth product, F_T . The term F_T simply indicates the frequency where the current gain in the common-emitter mode is one. This specification is more often seen on manufacturer's data sheets than the alpha or beta cutoff frequencies.

The current-gain bandwidth product is essentially constant. Consequently, as the operating frequency decreases, the current gain increases by the amount necessary to keep F_T constant.

USEFUL FORMULAS

Since most data sheets provide values for F_T and B , the following formulas are useful for estimating F_B and F_∞ .

$$F_B = \frac{F_T}{B} \quad (\text{Eq. 8-18})$$

$$F_\infty = (B + 1)F_B \approx BF_B \quad (\text{Eq. 8-19})$$

Where $B =$ low frequency value of h_{fe}

Equation 8-19 indicates that for a given transistor F_∞ is much larger than F_B . Therefore, a common-base circuit is capable of amplifying much higher frequencies than a comparable common-emitter circuit. For this reason, many amplifiers designed specifically for high-frequency operation use the common-base configuration.

Example 8-8

The data sheet for a particular transistor lists typical values for h_{fe} and F_T of 200 and 150MHz respectively. Estimate the values of F_B and F_∞ .

$$F_B = \frac{F_T}{B} = \frac{150\text{MHz}}{200} = .75\text{MHz} = 750\text{kHz}$$

$$F_\infty = BF_B = 200(0.75\text{MHz}) = 150\text{MHz}$$

Excluding other frequency effects, the upper frequency limits of the given transistor for the common-emitter and common-base configurations respectively, are 0.75MHz and 150MHz.

DATA SHEET CAPACITANCE VALUES

The value of C_{bc} is usually listed on a data sheet as C_{ob} , C_{obo} , C_{cb} , or C_o . While the data sheet value of C_{bc} is usually specified for a particular value of V_{CB} , it serves as a useful approximation of C_{cb} for other values as well.

C_{be} is normally not listed on the data sheet. However, the following formulas can be used to estimate the value of C_{be} :

$$C_{be} = \frac{1}{2\pi F_T r_e'} \quad (\text{Eq. 8-20})$$

Example 8-9

The data sheet of a 2N3903 transistor indicates that $F_{T\text{ MIN}} = 250\text{MHz}$ for $I_C = 10\text{mA}$ and $V_{CE} = 20\text{V}$. Based on the given information, estimate the value of C_{be} .

$$r_e' = \frac{37\text{mV}}{I_E} = \frac{37\text{mV}}{10\text{mA}} = 3.7\Omega$$

$$C_{be} = \frac{1}{2\pi F_T r_e'} = \frac{0.159}{250\text{MHz}(3.7\Omega)} = 171.9\text{pF}$$

OBSERVATIONS AND COMMENTS

High frequency analysis is considerably more complicated than low and mid frequency analysis. Even with a simplified high frequency model, the equations developed for F_{b_2} and F_{c_2} are tedious to work with because so many intermediate calculations are necessary.

Since precise values for h_{fe} , r_e' , r_b' , C_{be} , and C_{bc} are rarely available, you will frequently find a significant discrepancy between the calculated and measured upper cutoff frequencies. Nevertheless, the calculated value of F_2 provides a rough, but useful, estimate for the upper frequency limit of a given amplifier.

Obviously, stray capacitance is difficult to estimate. In order to predict accurate values of C_{s_1} and C_{s_2} , it is necessary to specify the specific type of components used in the circuit, the circuit layout, lead lengths, and so forth. Furthermore, when you measure F_2 , you must consider the capacitance of the measuring instrument. An oscilloscope, for example, typically introduces an additional 20-50 pF into the test circuit. For this reason, amplifier manufacturers frequently specify the type of test equipment, cable lengths, and other considerations that should be used when measuring F_2 .

When selecting a transistor for an amplifier, it is a good idea to check the transistor's data sheet to make sure that the following inequalities are satisfied.

$$F_{\infty} \gg F_2 \quad (\text{common-base circuit})$$

$$F_B \gg F_2 \quad (\text{common-emitter and common-collector circuits})$$

Where F_2 = minimum acceptable upper cutoff frequency.

BODE PLOTS

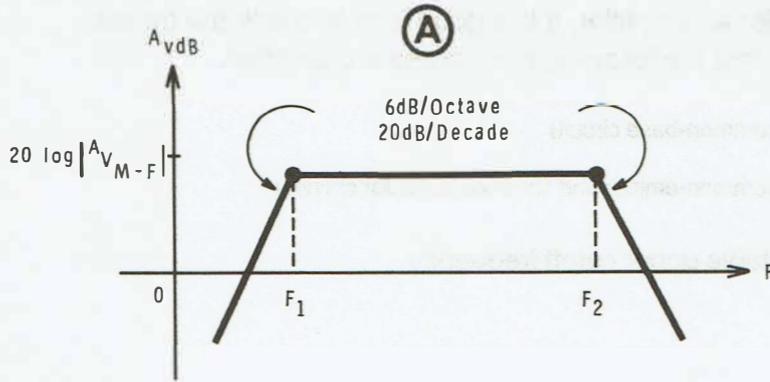
RC-coupled amplifiers contain three high-pass, and two low-pass filters. In the simplest case, the individual cutoff frequencies are far enough apart that little interaction occurs between the various filter sections. Assuming this is so, the lower, F_1 , and upper, F_2 , cutoff frequencies of the amplifier are closely approximated by:

$$F_1 \approx F_{b_1} \text{ or } F_{c_1} \text{ or } F_{e_1} \quad (\text{whichever is the highest})$$

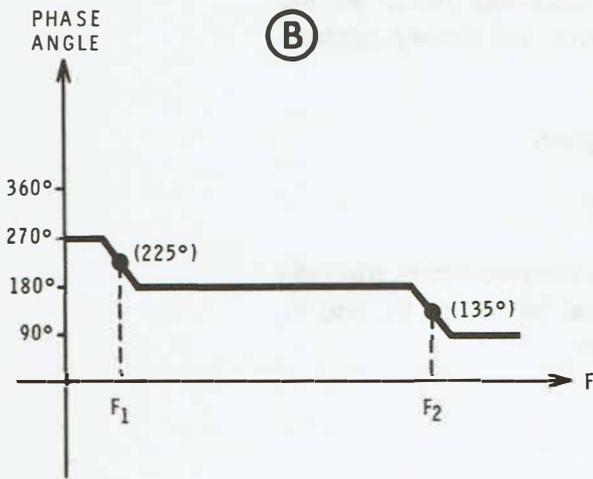
$$F_2 \approx F_{b_2} \text{ or } F_{c_2} \quad (\text{whichever is lowest})$$

If the individual cutoff frequencies are not more than two octaves apart, the individual filter sections will interact. In this case, the actual values of F_1 and F_2 are only roughly approximated by the formulas given earlier.

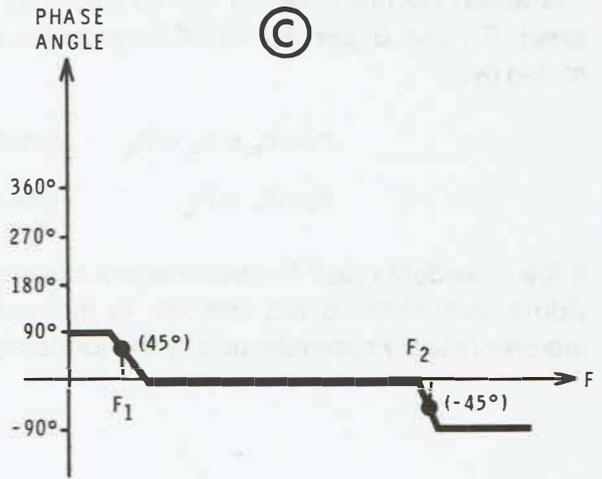
Assuming minimum interaction between the individual filter sections, a Bode plot of dB voltage gain versus frequency appears as shown in Figure 8-17A. Due to the presence of coupling and bypass capacitors, the voltage gain rolls off at 6dB/octave for frequencies less than F_1 . Similarly, for frequencies greater than F_2 , the presence of internal and stray capacitance also results in a 20dB/decade rolloff in the voltage gain. Note that the frequency response curve in Figure 8-17A is characteristic of all three BJT configurations. Furthermore, note that the overall frequency response curve is very similar to that of a bandpass filter.



BODE PLOT OF dB VOLTAGE GAIN VERSES FREQUENCY FOR ALL THREE CONFIGURATIONS.



COMMON-EMITTER CIRCUIT



COMMON-BASE AND COMMON-COLLECTOR CIRCUITS

Figure 8-17

RC coupled amplifier Bode plots. Here, it is assumed that little interaction occurs between the individual filter sections.

- A. Plot of dB voltage gain versus frequency for all three configurations.
- B. Common-emitter circuit.
- C. Common-base and common-collector circuits.

Bode plots of phase angle versus frequency are provided in Figure 8-17B, common-emitter circuit, and Figure 8-17C, common-base and common-collector circuits, respectively. In Figure 8-17B, note that in the mid-frequency region, the phase angle equals 180° . For frequencies less than F_1 , or greater than F_2 , the filters within the amplifier introduce an additional phase shift as shown in Figure 8-17B.

In the mid-frequency region, the input and output voltages in the common-base and common-collector amplifiers are in phase with each other. As was the case with the common-emitter amplifier however, signal frequencies less than F_1 , or greater than F_2 experience a phase shift. This is shown in Figure 8-17C.

RISE TIME

Figure 8-18A illustrates a voltage pulse driving a low-pass filter. From your knowledge of passive circuits, it is apparent that the output voltage appears as shown in Figure 8-18B. The equation that describes the output voltage is:

$$v_o = V(1 - e^{-t/RC}) \quad (\text{Eq. 8-21})$$

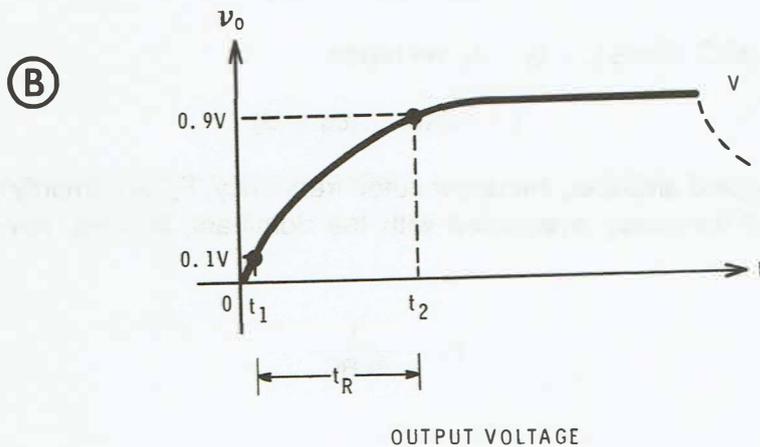
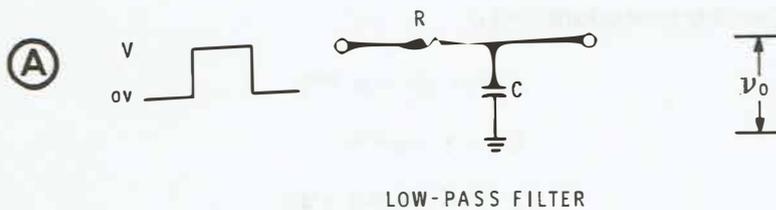


Figure 8-18

The concept of rise time.

- A. Low-pass filter.
- B. Output voltage.

In Figure 8-18B, the **rise time** is defined as the time required for the output voltage to rise from 10% to 90% of the final value, V . Thus:

$$t_r = t_2 - t_1$$

Expressing the rise time, t_r , in terms of the circuit's time constant, R times C shows a very useful relationship. To obtain the desired result proceed as follows:

At t_1 , $v_O = 0.1V$. Substituting $0.1V$ for v_O and t_1 for t into Equation 8-21, yields:

$$0.1V = V(1 - e^{-t_1/RC})$$

$$0.1 = 1 - e^{-t_1/RC}$$

$$e^{-t_1/RC} = 1 - 0.1 = 0.9$$

Taking the natural logarithm* of both sides of the equations:

$$-t_1/RC = \ln 0.9 = -0.105 \approx -0.1$$

Thus $t_1 = 0.1RC$

Following a similar procedure for t_2 :

$$0.9V = V(1 - e^{-t_2/RC})$$

$$0.9 = 1 - e^{-t_2/RC}$$

$$e^{-t_2/RC} = 1 - 0.9 = 0.1$$

$$-t_2/RC = \ln 0.1 = -2.3$$

Thus $t_2 = 2.3RC$. Since $t_r = t_2 - t_1$, we have:

$$t_r = 2.2RC \quad (\text{Eq. 8-22})$$

In an RC-coupled amplifier, the upper cutoff frequency, F_2 , is primarily determined by the cutoff frequency associated with the dominant, internal, low-pass filter. Thus:

$$F_2 = \frac{1}{2\pi RC}$$

* For a discussion of logarithms, see Heathkit/Zenith Passive Circuit Design course, EE-1001.

Where R and C are the equivalent resistance and capacitance of either the base or collector low-pass filters. Substituting $t_{r/2.2}$ for RC yields:

$$F_2 = \frac{1}{2\pi \frac{t_r}{2.2}} = \frac{0.35}{t_r} \quad (\text{Eq. 8-23})$$

Equation 8-23 indicates that you can measure the upper cutoff frequency of an RC-coupled amplifier by applying a pulse-type input, and noting the resulting rise time.

Example 8-10

A voltage pulse is applied to the input of an RC-coupled amplifier. The output voltage is noted to have a rise time of $0.175\mu\text{s}$. Estimate the amplifier's upper cutoff frequency, F_2 .

$$F_2 = \frac{0.35}{t_r} = \frac{0.35}{0.175\mu\text{s}} = 2\text{MHz}$$

SAG OR TILT

Figure 8-19A illustrates a voltage pulse driving a high-pass filter. In this case, the voltage across the resistor is a decaying exponential voltage, described by:

$$v_o = V e^{-t/RC} \quad (\text{Eq. 8-24})$$

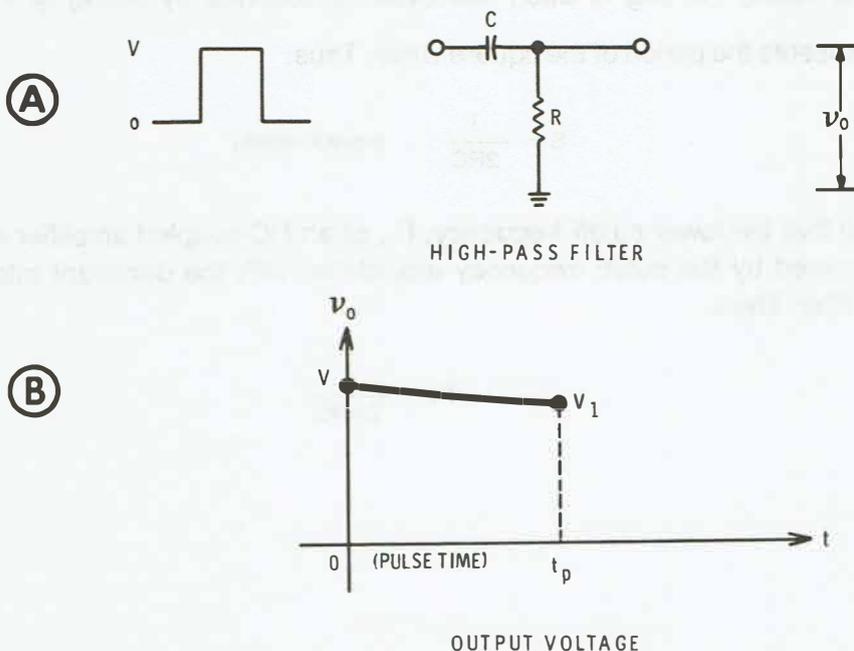


Figure 8-19

The concept of sag or tilt.
 A. High-pass filter.
 B. Output voltage.

If the filter's time constant is reasonably long compared to the width of the pulse, the output voltage has the general shape shown in Figure 8-19B. Note that the output voltage exhibits a tilt or "sag" when compared to the input voltage. The amount of sag is defined as follows:

$$S = \frac{V - V_1}{V} \quad (\text{Eq. 8-25})$$

Assuming the difference between V and V_1 is not excessive, Equation 8-24 can be approximated by:

$$v_o = V \left[1 - \frac{t}{RC} \right] \quad (\text{Eq. 8-26})$$

In Figure 8-19B we note that at time T_p , $v_o = V_1$. Thus:

$$V_1 = V \left[1 - \frac{t_p}{RC} \right] \quad (\text{Eq. 8-27})$$

Substituting Equation 8-27 into Equation 8-25 yields:

$$S = \frac{V - V \left[1 - \frac{t_p}{RC} \right]}{V} = \frac{t_p}{RC} \quad (\text{pulse})$$

Assuming the high-pass filter in Figure 8-19A is driven by a square wave rather than a pulse, the sag of each half cycle is obtained by letting $t_p = \frac{T}{2}$ where T represents the period of the square wave. Thus:

$$S = \frac{T}{2RC} \quad (\text{square-wave})$$

Recall that the lower cutoff frequency, F_1 , of an RC-coupled amplifier is primarily determined by the cutoff frequency associated with the dominant internal high-pass filter. Thus:

$$F_1 = \frac{1}{2\pi RC}$$

Where R and C are the equivalent resistance and capacitance of either the base, collector, or emitter high-pass filters. Substituting $\frac{T}{2S}$ for RC yields:

$$F_1 = \frac{1}{2\pi \frac{T}{2S}} = \frac{S}{\pi T}$$

Similarly, substituting $\frac{1}{F}$ for T and dividing by π you obtain:

$$F_1 = 0.318 S F_{IN} \quad (\text{Eq. 8-28})$$

Where $S = \text{sag}$
 $F_1 = \text{lower cutoff frequency}$
 $F_{IN} = \text{frequency of the square wave}$

Equation 8-28 indicates that you can measure the lower cutoff frequency of an RC-coupled amplifier by applying a square-wave input and noting the resulting sag.

Example 8-11

The input and output waveforms for an RC-coupled amplifier are shown in Figure 8-20. Estimate the amplifier's lower cutoff frequency, F_1 .

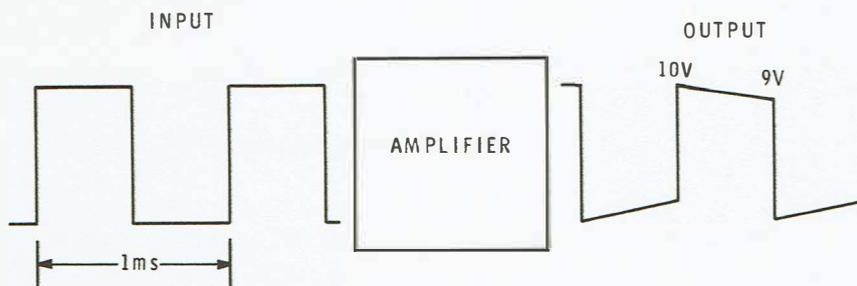


Figure 8-20

Circuit for Example 8-11.

Since the period of the input signal is 1 ms:

$$F = \frac{1}{T} = \frac{1}{1\text{ms}} = 1\text{kHz}$$

The sag in the output voltage is:

$$S = \frac{V - V_1}{V} = \frac{10\text{V} - 9\text{V}}{10} = 0.1$$

Thus:

$$F_1 = 0.318 S F_{\text{IN}}$$

$$F_1 = 0.318(0.1)(1\text{kHz}) = 31.8\text{Hz}$$

SQUARE-WAVE TESTING

By adjusting the frequency of a square-wave input signal, it is possible to quickly estimate the amplifier's F_1 and F_2 frequencies. In addition, you can quickly determine the effect of varying component values by simply observing the output voltage. Checking an amplifier with a square wave is a very useful experiment.

Self-Test Review

13. The lower cutoff frequency of an RC-coupled amplifier is approximately equal to F_{b_1} , or F_{c_1} , or F_{e_1} , whichever is _____.
larger/smaller
14. $F_2 \approx$ _____ MHz, assuming $F_{b_1} = 2\text{MHz}$ and $F_{e_2} = 4.5\text{MHz}$.
15. For a particular BJT, $\alpha = 0.99$, $B = 99$, and $F_T = 100\text{MHz}$. The beta cutoff frequency is therefore approximately _____ MHz.
16. A data sheet lists $F_T = 300\text{MHz}$ at $I_C = 20\text{mA}$. Similarly, $C_{b_0} = 30\text{pF}$ at $I_E = 20\text{mA}$. Consequently, $C_{b_e} \approx$ _____ pF and $C_{b_c} \approx$ _____ pF.
17. Assuming minimum interaction between the various internal filters of an RC-coupled amplifier, for frequencies less than F_1 or greater than F_2 , the voltage gain rolls off at _____ dB per decade.
18. By applying a square-wave input to an RC-coupled amplifier, you find the rise time to be $0.35\mu\text{s}$. Therefore, the amplifier's upper cutoff frequency is approximately _____ MHz.
19. A 2kHz square wave produces a tilt in the output voltage of an RC-coupled amplifier of 15%. Therefore, the amplifier's lower cutoff frequency is approximately _____ Hz.
20. Of the following capacitances, C_{b_e} , C_{b_c} , and C_{c_e} , _____ contributes most to the total input capacitance in a high-gain amplifier.
21. In a common-emitter amplifier, F_B should be _____ than the desired F_2 .
larger/smaller
22. Internal BJT and stray capacitance have _____ effect on the amplifier's lower cutoff frequency.
a significant/little

Answers

- | | |
|-------------------|--------------|
| 13. larger | 18. 1MHz |
| 14. 2MHz | 19. 95.4Hz |
| 15. 1.01MHz | 20. C_{bc} |
| 16. 286.5pF, 30pF | 21. larger |
| 17. -20dB | 22. little |

Appropriate solutions follow:

$$15. F_B = \frac{F_T}{B} = \frac{100\text{MHz}}{99} = 1.01\text{MHz.}$$

$$16. r_e' = \frac{37\text{mV}}{I_E} = \frac{37\text{mV}}{20\text{mA}} = 1.85\Omega$$

$$C_{be} = \frac{1}{2\pi F_T r_e'} = \frac{0.159}{300\text{MHz}(1.85\Omega)} = 286.5\text{pF}$$

$$C_{bc} = C_{obo} = 30\text{pF}$$

17. Refer to Figure 8-17A

$$18. F_2 = \frac{0.35}{t_r} = \frac{0.35}{0.35\mu\text{s}} = 1\text{MHz}$$

$$19. S = 15\% = 0.15$$

$$F_1 = 0.318 S F_{IN}$$

$$F_1 = 0.318(0.15)(2\text{kHz}) = 95.4\text{Hz}$$

SUMMARY

All RC-coupled amplifiers contain numerous capacitances. The various capacitors in conjunction with circuit resistances form three low-pass and two high-pass AC filters. Consequently, the overall frequency response characteristic is essentially that of an active bandpass filter.

The “visible capacitors” consist of two coupling and one bypass capacitor. These capacitors form high-pass filters which shape the low-frequency portion of the overall response curve. For this reason, the lower cutoff frequency approximately equals F_{b_1} , or F_{c_1} , or F_{e_1} , whichever is higher. Formulas for these individual cutoff frequencies are provided in the unit.

The two low-pass filters comprised of internal BJT and external parasitic capacitances shape the high-frequency portion of the overall response curve. Consequently, the upper cutoff frequency approximately equals F_{b_2} or F_{c_2} , whichever is lower. In practice, it is difficult to accurately predict F_2 due to the uncertainty in actual parameter values.

Square waves are frequently used to quickly evaluate the frequency response characteristics of an amplifier. By measuring the rise time of the output voltage, you can calculate F_2 from:

$$F_2 = \frac{0.35}{t_r}$$

Similarly, by adjusting the frequency of the square wave to obtain an output that sags, you can calculate F_1 from:

$$F_1 = 0.318 S F_{IN}$$

In addition, by noting the shape of the square-wave output voltage as you change component values, you can immediately see how each change effects the output. For these reasons, square-wave testing is very useful.

SUMMARY

All FOI requests are processed through the Freedom of Information Act. The Freedom of Information Act is a federal law that gives citizens the right to know what their government is doing. It was passed in 1967 and has since been amended several times. The Act is designed to ensure that the government is open and accountable to the people. It allows citizens to request access to government records, and it provides a process for appealing if a request is denied. The Act is a key part of the democratic process, and it is essential for a free and open society.

The right to know is a fundamental principle of democracy. It allows citizens to hold their government accountable and to make informed decisions about public policy. The Freedom of Information Act is a key tool for exercising this right. It provides a legal framework for requesting and receiving government records. The Act is a cornerstone of the American system of government, and it is essential for a free and open society.

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UNIT EXAMINATION

The following multiple choice examination is designed to test your understanding of the material presented in this unit. Place a check beside the multiple choice answer (A, B, C, or D) that you feel is most correct. When you have completed the examination, compare your answers with the correct ones that appear after the exam.

1. In a common-emitter amplifier, when $F = F_1$, the phase angle equals:
 - A. 225° .
 - B. 180° .
 - C. 135° .
 - D. 45° .

2. Amplifier A has an upper cutoff frequency of 2MHz. Amplifier B has a rise time of $0.1\mu\text{s}$ when tested with a square-wave. Therefore:
 - A. Amplifier A has a better high frequency response.
 - B. Amplifier B has a better high frequency response.
 - C. Amplifier A has a better low frequency response.
 - D. The sag of each amplifier is approximately equal.

3. For a certain amplifier $F_{b_2} = 1\text{MHz}$ and $F_{c_2} = 6\text{MHz}$. Therefore:
 - A. $F_2 \approx 6\text{MHz}$.
 - B. $F_2 \approx 1\text{MHz}$.
 - C. $F_2 \approx 7\text{MHz}$.
 - D. The sag is excessive.

4. A certain amplifier has $F_{b_1} = 20\text{Hz}$, $F_{c_1} = 80\text{Hz}$, and $F_{e_1} = 320\text{Hz}$. The amplifier's lower cutoff frequency is therefore, approximately:
 - A. 20Hz.
 - B. 80Hz.
 - C. 320Hz.
 - D. 140Hz.

5. The frequency at which the current gain of a BJT in a common-emitter circuit is unity is called:
- A. The alpha cutoff frequency.
 - B. The beta cutoff frequency.
 - C. The current-gain bandwidth product.
 - D. The upper cutoff frequency.
6. Assuming $F_T = 300\text{MHz}$ and $\alpha = 0.98$, then F_B equals:
- A. $0.98 (300\text{MHz})$.
 - B. $300\text{MHz}/0.98$.
 - C. 300MHz .
 - D. 6.12MHz .
7. For frequencies below F_1 or above F_2 , the voltage gain of an RC-coupled amplifier rolls off at:
- A. 20dB/decade .
 - B. 10dB/decade .
 - C. 6dB/decade .
 - D. 20dB/octave .

The following information applies to questions 8 through 12.

A fully bypassed common-emitter amplifier has:

$$\begin{array}{ll} A_{v_{M-F}} = -100 & C_{ob} = 5\text{pF} \\ F_T = 350\text{MHz} & C_1 = 10\mu\text{F} \\ C_{s_1} = 40\text{pF} & R_{IN} = 2\text{k}\Omega \\ C_{s_2} = 30\text{pF} & R_S = 600\Omega \end{array}$$

8. C_{be} is approximately:
- A. 5pF .
 - B. 312pF .
 - C. 98.6pF .
 - D. 61.4pF .

9. C_b is approximately:

- A. 61.4pF.
- B. 312pF.
- C. 5pF.
- D. 98.6pF.

10. The total input capacitance is approximately:

- A. 40pF.
- B. 501pF.
- C. 606.6pF.
- D. 1 μ F.

11. The total output capacitance is approximately:

- A. 5pF.
- B. 35pF.
- C. 501pF.
- D. 22.9pF.

12. Assuming the high-pass base filter is dominant, the lower cutoff frequency is approximately:

- A. 6.1Hz.
- B. 33.7Hz.
- C. 60Hz.
- D. 127Hz.

10. The number of...

- A. 10
- B. 15
- C. 20
- D. 25

11. The number of...

- A. 10
- B. 15
- C. 20
- D. 25

12. The number of...

- A. 10
- B. 15
- C. 20
- D. 25

13. The number of...

- A. 10
- B. 15
- C. 20
- D. 25

EXAMINATION ANSWERS

1. A — Referring to the Bode plot in Figure 8-17B, you can see that the phase angle equals 225° when $F = F_1$.

2. B — For amplifier B:

$$F_2 = \frac{0.35}{t_r} = \frac{0.35}{0.1\mu\text{s}} = 3.5\text{MHz}$$

Since $F_{B_2} > F_{A_2}$ amplifier B has a better high-frequency response.

3. B — $F_2 = F_{b_2}$ or F_{c_2} whichever is lower. Therefore $F_2 \approx 1\text{MHz}$.

4. C — $F_1 = F_{b_1}$, F_{c_1} , or F_{e_1} whichever is larger. Therefore $F_1 \approx 320\text{Hz}$.

5. C — The current gain bandwidth product is the frequency where the current gain of a BJT in a common-emitter circuit is unity.

6. D — $B = \frac{\alpha}{1 - \alpha} = \frac{0.98}{1 - 0.98} = 49$

$$F_B = \frac{F_T}{B} = \frac{300\text{MHz}}{49} = 6.12\text{MHz}$$

7. A — In an RC-coupled amplifier, the voltage gain rolls off at 6dB/octave and is equivalent to 20dB/decade.

8. D — $r_e' = \frac{37\text{mV}}{I_E} = \frac{37\text{mV}}{5\text{mA}} = 7.4\Omega$

$$C_{be} = \frac{1}{2\pi F_T r_e'}$$

$$C_{be} = \frac{0.159}{350\text{MHz}(7.4\Omega)} = 61.4\text{pF}$$

9. A — $C_b = C_{be}$ for a fully bypassed emitter capacitor. This is evident from Equation 8-13:

$$C_b = C_{be} \left[1 - \frac{R_{E_1}}{R_{E_1} + r_e'} \right]$$

Note that $\frac{1 - R_{E_1}}{R_{E_1} + r_e'}$

equals 1 when $R_{E_1} = 0$.

Thus $C_b = 61.4\text{pF}$

10. C — First calculate the Miller capacitance.

$$C_m = (A_v + 1)C_{bc}$$

$$\text{Since } C_{bc} = C_{ob} = 5\text{pF, and } |A_{v_{M-F}}| = 100$$

$$C_m = (100 + 1)5\text{pF} = 505\text{pF}$$

$$C_{IN} = C_{s_1} + C_m + C_b$$

$$C_{IN} = 40\text{pF} + 505\text{pF} + 61.4\text{pF}$$

$$C_{IN} = 606.4\text{pF}$$

11. B — $C_o = C_{bc} + C_{s_2}$
 $C_o = 5\text{pF} + 30\text{pF} = 35\text{pF}$

12. A — $F_{b_1} = \frac{1}{2\pi(R_S + R_{IN})C_1}$
 $F_{b_1} = \frac{0.159}{(600\Omega + 2\text{k}\Omega)10\mu\text{F}} = 6.1\text{Hz} = F_1$

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UNIT 9

EXPERIMENTS

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INTRODUCTION

The experiments that follow have been designed to complement the material presented in Units 1 through 8. Before you build the experimental circuits, you should first read each experiment to make sure you understand the purpose of each step.

Important Notice

Newer Heathkit Electronic Design Experimenters have a 3-terminal power plug, rather than the conventional 2-terminal power plug. If you are using one of these newer Trainers, and the test equipment you are using (oscilloscope, voltmeter, etc.) also has a 3-terminal power plug, you must install a 3-wire to 2-wire adapter on the **Trainer** power plug. Without this adapter, the Trainer fuse may blow or you may obtain invalid results from some of the experiments. These adapters are inexpensive and readily available at most stores.

This adapter is necessary **only** when you are making measurements not referenced to ground, using test equipment that has a 3-terminal power plug.

CAUTION

Make sure all pieces of equipment used in your experiments are connected to the same power source.

EXPERIMENT 1

BJT DC CHARACTERISTICS

Objectives:

To examine a typical BJT data sheet.

To experimentally determine values of B and α for a type MPS-A20 transistor.

To plot the output (collector) curves for a type MPS-A20 transistor.

To introduce the concepts of DC saturation and cutoff.

Introduction

The significant electrical characteristics of a particular BJT are summarized on the manufacturer's data sheet for that BJT. In this experiment, you will begin to examine a typical BJT data sheet. Initially, we will concentrate on those parameters introduced in Unit 1. As your knowledge of BJTs expands, so will your understanding of the various other parameters and specifications typically included on the BJT data sheet.

Two of the most important DC parameters are α and B . Recall that these parameters are usually defined as follows:

$$\alpha = \frac{I_C}{I_E} \quad \text{and} \quad B = \frac{I_C}{I_B}.$$

On most data sheets, the value of B is indicated by the symbol h_{FE} . Once you know the value of B , you can calculate the corresponding value of α from the formula:

$$\alpha = \frac{B}{B + 1}.$$

Normally, the value of α is not provided on a BJT's data sheet. However, if it is, the symbol h_{FB} is used to indicate α .

In this experiment, you will take the necessary measurements to plot the transistor's output curves for the common-emitter configuration. Recall that these curves indicate the relationship between the transistor's base current, collector current, and collector-to-emitter voltage.

Finally, you will be introduced to the concepts of DC saturation and cutoff. These concepts will prove useful when the topics of biasing schemes and amplifiers are discussed in later units.

Material Required

Heathkit Engineering Design Trainer ET-1000

Multimeter with test leads.

Oscilloscope

3 — NPN type MPS-A20 transistors (417-801)

1 — 1k Ω , 1/4-watt, 5% resistor

1 — 5.6k Ω , 1/4-watt, 5% resistor

1 — 10k Ω , 1/4-watt, 5% resistor

1 — 82k Ω , 1/4-watt, 5% resistor

Procedure

1. Examine the data sheets for the MPS-A20 transistor provided in the Appendix at the end of Unit 9. Some calculations may be required.

- (a) Record the minimum and maximum values of α for $I_C = 5\text{mA}$ and $V_{CE} = 10\text{V}$.

$$\alpha_{(\text{MIN})} = \underline{\hspace{2cm}} \quad \alpha_{(\text{MAX})} = \underline{\hspace{2cm}}$$

- (b) Assuming $h_{FE} = 200$ for $I_C = 5\text{mA}$, $V_{CE} = 10\text{V}$, and $T_A = 25^\circ\text{C}$ what value of h_{FE} would you expect if I_C was increased to 100mA?

$$h_{FE} = \underline{\hspace{2cm}}$$

- (c) What is the largest value of I_{CEO} you would expect to encounter?

$$I_{CEO(\text{MAX})} = \underline{\hspace{2cm}}$$

- (d) What is the maximum power the transistor can dissipate if the ambient temperature is 25°C?; 40°C?

$$P_{(\text{MAX})} = \underline{\hspace{2cm}} \text{ at } 25^\circ\text{C}.$$

$$P_{(\text{MAX})} = \underline{\hspace{2cm}} \text{ at } 40^\circ\text{C}.$$

Discussion

Perhaps you experienced some difficulty locating the requested information. Frequently, you must “derive” the information you want from the information provided on a particular data sheet. Your ability to do this will increase as you become more familiar with typical data sheets. In any event, the requested information can be deduced as follows:

- (a) Values of α or h_{FB} are not given directly. However, under “Electrical Characteristics,” note that minimum and maximum values of h_{FE} are provided. Since $h_{FE} = B$, you can calculate the corresponding values of α . Specifically:

$$B_{(MIN)} = 40, \alpha_{(MIN)} = \frac{B}{B + 1} \approx 0.976.$$

$$B_{(MAX)} = 400, \alpha_{(MAX)} = \frac{400}{401} \approx 0.998.$$

- (b) For $I_C = 5\text{mA}$, $V_{CE} = 10\text{V}$, and $T_A = 25^\circ\text{C}$, B can have any value between 40 and 400. Here, we are assuming that for a particular transistor, $B = 200$ for the specified conditions.

The value of B varies with the value of collector current as shown in Figure 3, NORMALIZED DC CURRENT GAIN, on the data sheet. Note that the normalized value of h_{FE} corresponding to $I_C = 100\text{mA}$ is 0.6. This means that the value of h_{FE} when $I_C = 100\text{mA}$ is 0.6 times the value of h_{FE} when $I_C = 5\text{mA}$. Thus:

$$h_{FE} = 0.6(200) = 120.$$

- (c) The maximum value of I_{CBO} listed in the Electrical Characteristics is 100nA . Similarly, the maximum value of h_{FE} is 400. Thus:

$$I_{CEO(MAX)} = (B_{(MAX)} + 1)I_{CBO(MAX)}.$$

$$I_{CEO(MAX)} = 401(100\text{nA}) = 40.1\mu\text{A}.$$

This represents the “worst case” value of I_{CEO} , since it is assumed that B and I_{CBO} are maximum. In a sample of MPS-A20 transistors, typical values of I_{CEO} would be much smaller.

- (d) Under maximum ratings $P_D = 350\text{mW}$ at an ambient temperature of 25°C . Note that above 25°C , the total power dissipation must be derated by $2.8\text{mW}/^\circ\text{C}$. Therefore, when the ambient temperature is 40°C :

$$P_D = P_{25^\circ\text{C}} - D \Delta T.$$

$$P_D = 350\text{mW} - \frac{2.8\text{mW}}{^\circ\text{C}} (15^\circ\text{C}).$$

$$P_D = 350\text{mW} - 42\text{mW} = 308\text{mW}.$$

On the data sheet, the subscript A indicates the ambient, surrounding, temperature. Similarly, the subscript C indicates the case temperature. Note that calculations based on the case temperature, T_C do not have the same values of P_D and derating factor, as those based on ambient temperature.

Procedure (Continued)

- With the ET-1000 Trainer turned off, construct the circuit shown in Figure E1-1A. Use the $100\text{k}\Omega$ and $1\text{k}\Omega$ potentiometers on the Trainer for R_1 and R_2 . Looking at the flat side of the transistor, the leads are identified as shown in Figure 1-1B.

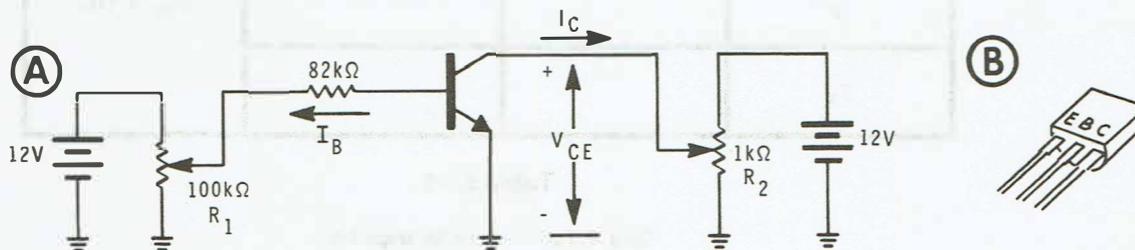


Figure E1-1

Experimental circuit for steps 2-7.

3. Adjust R_1 and R_2 to approximately mid-range, and then turn on the power. With the power on, make the following adjustments:
 - (a) Adjust R_1 to get a collector current of 5mA.
 - (b) Now adjust R_2 to get a collector-to-emitter voltage of 10V. Measure V_{CE} with the oscilloscope.
 - (c) If necessary, readjust R_1 to get a collector current of 5mA.
4. Measure the base current, I_B . Your measured value will typically be within the range of $12.5\mu\text{A}$ to $125\mu\text{A}$. Record your measured value of I_B next to T_1 in Table E1-1. Turn the ET-1000 Trainer off.
5. Repeat steps 2 and 4 for two additional MPS-A20 transistors. Record the measured base currents next to T_2 and T_3 respectively in Table E1-1.

Transistor	I_B (Measured)	h_{FE} (Calculated)	Conditions
T_1			$I_C = 5\text{mA}$
T_2			$V_{CE} = 10\text{V}$
T_3			

Table E1-1

Data and calculations for steps 4-6.

Procedure (Continued)

8. With the ET-1000 Trainer turned off, construct the circuit shown in Figure E1-2. Adjust R_1 and R_2 to approximately mid-range.
9. Turn the power on, and make the following adjustments:
 - (a) Adjust R_1 until the voltage across $R_B = 0.1V$. This sets the base current to $10\mu A$.
 - (b) Adjust R_2 to get a collector-to-emitter voltage of $6V$. Measure V_{CE} with the oscilloscope.

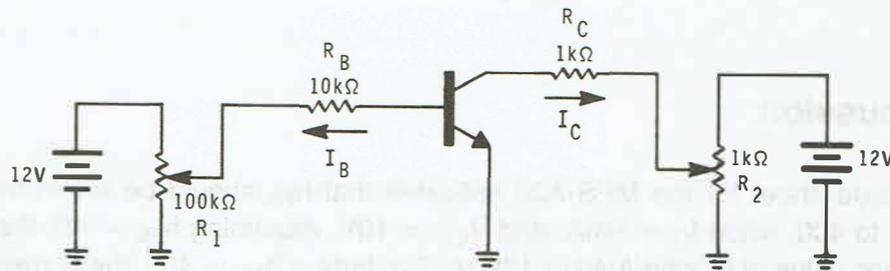


Figure E1-2

Experimental circuit for steps 8-16.

10. Now use your multimeter to measure the voltage across R_C . Since $R_C = 1k\Omega$, the collector current equals the voltage across R_C divided by $1k\Omega$. Record the measured value of I_C below the V_{CE} value of $6V$ in Table E1-2.
11. Complete Table E1-2 by adjusting V_{CE} to the remaining values indicated while recording the corresponding values of I_C .

$I_B = 10\mu A$									
V_{CE} (V)	0.1	0.2	0.6	1	2	3	4	5	6
I_C (mA)									

Table E1-2

Data for steps 9-11.

12. Adjust R_1 until the voltage across $R_B = 0.2V$. This sets the base current to $20\mu A$. Now adjust R_2 to obtain a collector-to-emitter voltage of $6V$.
13. Record the measured values of I_C corresponding to the values of V_{CE} in Table E1-3.

$I_B = 20\mu A$									
V_{CE} (V)	0.1	0.2	0.6	1	2	3	4	5	6
I_C (mA)									

Table E1-3

Data for steps 12-13.

14. Adjust R_1 until the voltage across $R_B = 0.3V$. This sets the base current to $30\mu A$. Now adjust R_2 to obtain a collector-to-emitter voltage of $6V$.
15. Record the measured values of I_C corresponding to the values of V_{CE} in Table E1-4.

$I_B = 30\mu A$									
V_{CE} (V)	0.1	0.2	0.6	1	2	3	4	5	6
I_C (mA)									

Table E1-4

Data for steps 14-15.

16. Plot the values of I_C and V_{CE} in Tables E1-2, E1-3, and E1-4 on the graph paper provided in Figure E1-3. Label the curves $I_B = 10\mu\text{A}$, $20\mu\text{A}$, and $30\mu\text{A}$ respectively. In Figure E1-3, note the expanded scale for values of V_{CE} less than 1V.

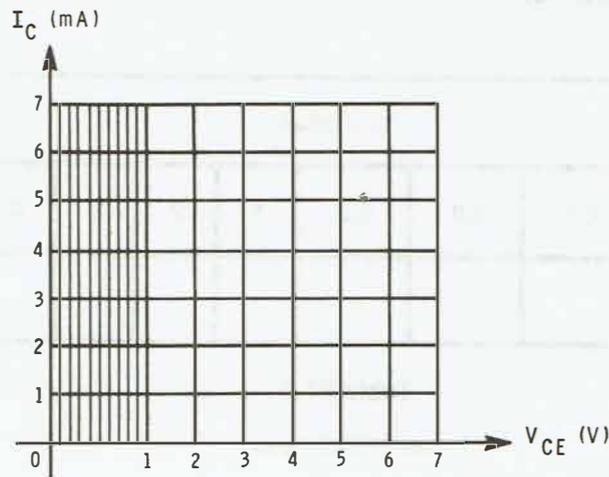


Figure E1-3

Graph for recording V_{CE} and I_C values for step 16.

Discussion

In this portion of the experiment, for values of I_B equal to $10\mu\text{A}$, $20\mu\text{A}$, and $30\mu\text{A}$ respectively, you measured values of I_C corresponding to values of V_{CE} between 0.1V and 6V. However, since the maximum value of 6V for V_{CE} , was less than the collector-emitter breakdown voltage, your curves illustrate the characteristics of a transistor well below the breakdown region.

For values of V_{CE} greater than 1V, your curves should show that I_C remains almost constant as V_{CE} is increased to 6V. This indicates that, in this region of operation, the transistor acts like a constant current source, for a specific I_B value, when viewed from the collector-emitter terminals.

Examine the portion of your curves for values of V_{CE} less than 1V. The value of I_C is primarily determined by the value of V_{CE} and not by the value of I_B . The portion of each curve where I_C increases rapidly with a small increase in V_{CE} before the knee of the curve, is referred to as the **saturation region**. Except for switching applications, the transistor is generally not operated within this region. When a transistor is operated in the saturation region, V_{CE} is very small, typically a few tenths of a volt.

Recall that when $I_B = 0$, $I_C = I_{CEO}$ in the common-emitter configuration. Since I_{CEO} is usually very small, the collector current is approximately zero. In this case, the transistor is said to be operating in the **cutoff region**. As was the case with the saturation region, the transistor is generally not operated within the cutoff region.

Figure E1-4 illustrates the three possible regions of operation. Note that the region between cutoff and saturation is referred to as the **active region**. For most applications, BJT's are biased to operate within the active region.

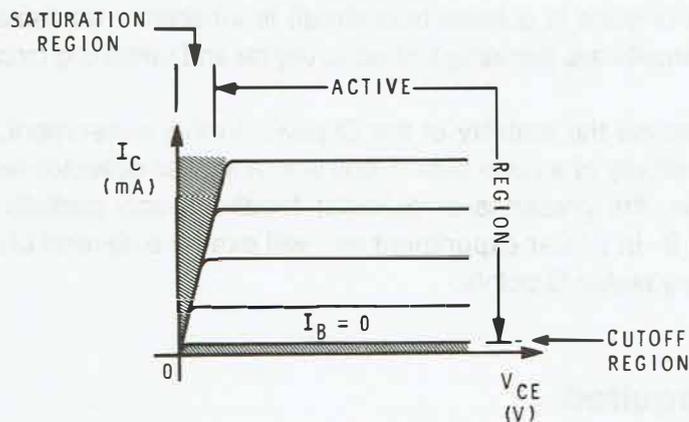


Figure E1-4

Cutoff, active, and saturation regions of the common emitter output curves.

EXPERIMENT 2

BASE BIAS AND COLLECTOR FEEDBACK CIRCUITS

Objectives:

To design an LED driver circuit.

To design a base bias circuit.

To design a collector-feedback bias circuit.

To compare the B sensitivity of the base bias, and collector-feedback circuits.

Introduction

In base bias circuits, collector current is directly proportional to B . B varies widely from one transistor to the next, and also varies significantly with temperature. Therefore, the Q point in a base bias circuit is inherently unstable. Applications for base bias circuits are primarily limited to digital and switching circuits.

Feedback improves the stability of the Q point. In this experiment, you will compare the B sensitivity of a base bias circuit with a similar collector-feedback circuit. As you will see, the presence of collector feedback only partially compensates for changes in B . In a later experiment you will examine several biasing schemes that provide very stable Q points.

Material Required

Heathkit Engineering Design Trainer ET-1000

Multimeter with test leads

Oscilloscope

3 — NPN type MPS-A20 transistors (417-801)

1 — 680Ω , 1/4-watt, 5% resistor

1 — $3.9k\Omega$, 1/4-watt, 5% resistor

1 — $5.6k\Omega$, 1/4-watt, 5% resistor

1 — $680k\Omega$, 1/4-watt, 5% resistor

1 — $1.5M\Omega$, 1/4-watt, 5% resistor

1 — LED (412-640)

Procedure

- The LED in Figure E2-1 will provide adequate brilliance if the current through it is approximately 15mA. Calculate the required values for R_S and R_B assuming the voltage drop across the LED is approximately 2V.

$$R_S = \text{_____} \Omega, \quad R_B = \text{_____} \text{ k}\Omega.$$

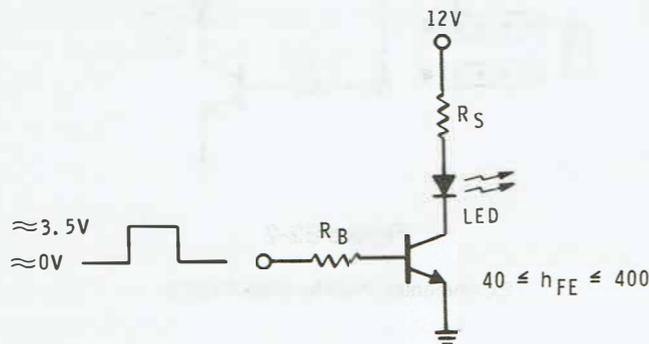


Figure E2-1

Experimental circuit for step 1.

Discussion

Your calculations should be similar to the following:

$$R_S = \frac{V_{CC} - V_{LED}}{I_{LED}} = \frac{12V - 2V}{15mA} = 0.67k\Omega = 670\Omega.$$

To ensure adequate overdrive, I_B should equal $2I_{B(SAT)}$ Thus:

$$I_B = 2I_{B(SAT)} = \frac{2I_{C(SAT)}}{h_{FE(MIN)}} = \frac{2(15mA)}{40} = 0.75mA.$$

$$R_B = \frac{V_1 - V_{BE}}{I_B} = \frac{3.5V - 0.7V}{0.75mA} = 3.7k\Omega.$$

Therefore, standard value 680 Ω and 3.9k Ω resistors would be acceptable for this design.

Procedure (Continued)

- Construct the circuit shown in Figure E2-2. Note that logic switch \bar{A} on the ET-1000 Trainer is used to provide the input voltage to the LED driver.

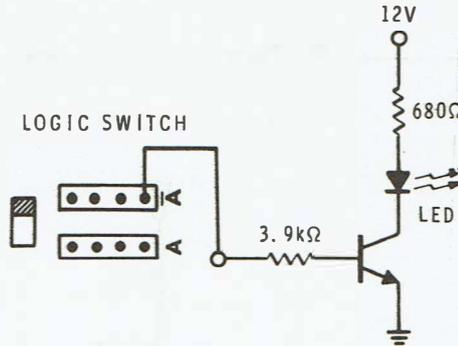


Figure E2-2

Experimental circuit for steps 2 and 3.

- Use the oscilloscope to measure the output voltage from the logic switch for both switch positions. Also note the status of the LED (ON or OFF) for both switch positions.

SWITCH POSITION	OUTPUT VOLTAGE	LED
\bar{A}	_____	_____
A	_____	_____

Discussion

The output voltage from the logic switch should be approximately 3.5V with the switch in the \bar{A} position, and the driver circuit connected to \bar{A} . In this case, sufficient base current flows to saturate the transistor. Consequently, the LED should be ON.

When the logic switch is held in the A position, the switch output voltage is a few tenths of a volt or less. In this case, essentially no base current flows and the transistor is cutoff. The collector current is essentially zero, and the LED is OFF.

LED drivers can be used as simple indicator lights, or as logic monitors in digital systems. Many other applications are also possible.

Procedure (Continued)

4. When a parameter varies over a wide range, circuit designers often use the geometric average of the parameter for purposes of calculation. This is defined as the square root of the product of the parameter's minimum and maximum values. Calculate the geometric average for h_{FE} in Figure E2-3.

$$h_{FE} = \text{_____} \text{ (geometric average).}$$

5. Using the value of h_{FE} obtained in step 4, calculate the values required for R_C and R_B in Figure E2-3.

$$R_C = \text{_____} \text{ k}\Omega, \quad R_B = \text{_____} \text{ k}\Omega.$$

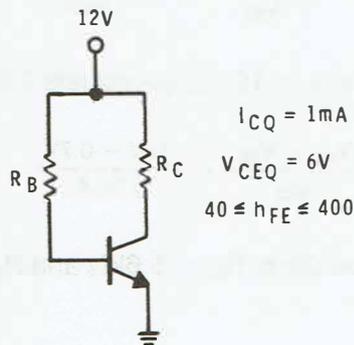


Figure E2-3

Base bias circuit.

6. Using the value of h_{FE} obtained in step 4, calculate the values required for R_C and R_B in Figure E2-4.

$$R_C = \text{_____} \text{ k}\Omega, \quad R_B = \text{_____} \text{ k}\Omega.$$

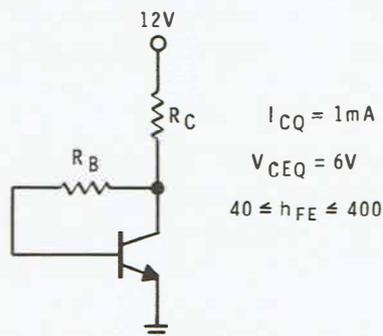


Figure E2-4

Collector feedback circuit.

Discussion

Your calculations for steps 4 through 6 should be similar to the following:

Step 4.

Since $h_{FE(MIN)} = 40$ and $h_{FE(MAX)} = 400$, the geometric average is:

$$h_{FE} = \sqrt{40(400)} = 126.5.$$

Step 5.

Referring to the base bias summary guide:

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{12V - 6V}{1mA} = 6k\Omega.$$

Assuming $I_{CQ} = 1mA$ and $h_{FE} = 126.5$, I_{BQ} equals $1mA/126.5$ or $7.9\mu A$. Thus:

$$R_B = \frac{V_{CC} - V_{BE}}{I_{BQ}} = \frac{12V - 0.7V}{7.9\mu A} = 1.43M\Omega.$$

Selecting standard value resistors, $R_C = 5.6k\Omega$ and $R_B = 1.5M\Omega$.

Step 6.

In the collector feedback summary guide, note that R_C and I_{BQ} are calculated as in step 5. In this case, the required value of R_B is:

$$R_B = \frac{V_{CEQ} - V_{BE}}{I_{BQ}} = \frac{6V - 0.7V}{7.9\mu A} = 670k\Omega.$$

Using standard resistance values, $R_C = 5.6k\Omega$ and $R_B = 0.68M\Omega$.

Procedure (Continued)

- Construct the circuit shown in Figure E2-3. Here, $R_C = 5.6\text{k}\Omega$ and $R_B = 1.5\text{M}\Omega$. You will use your meter to measure collector current and the oscilloscope to measure collector-to-emitter voltage.
- Turn the power on, and record the measured values of I_{CQ} and V_{CEQ} in the T_1 row of Table E2-1. Once you have recorded the measured values, turn the power off.
- Remove the transistor and mark it T_1 , then replace it with a second MPS-A20 transistor. Turn the power on and record the values of I_{CQ} and V_{CEQ} in the T_2 row of Table E2-1. Now turn the power off, remove the transistor and mark it T_2 . Make sure you know which transistor is T_1 and which transistor is T_2 .
- Place the third transistor, T_3 , in the circuit. Turn the power on, and record the measured values of I_{CQ} and V_{CEQ} in the T_3 row of Table E2-1. Turn the power off, and remove the transistor. Again, keep track of which transistor corresponds to rows T_1 , T_2 , and T_3 .

Transistor	I_{CQ} (mA)	V_{CEQ} (V)
T_1		
T_2		
T_3		

Table E2-1

Data for the base bias circuit.

11. Using the first transistor, T_1 , construct the circuit shown in Figure E2-4. In this case, $R_C = 5.6\text{k}\Omega$ and $R_B = 0.68\text{M}\Omega$. Turn the power on and record the measured values of I_{CQ} and V_{CEQ} in the T_1 row of Table E2-2. Once you have recorded the measured values of I_{CQ} and V_{CEQ} , shut the power off.
12. Repeat step 11 for the second, T_2 and third, T_3 transistors.

Transistor	I_{CQ} (mA)	V_{CEQ} (V)
T_1		
T_2		
T_3		

Table E2-2

Data for the collector feedback bias circuit.

Discussion

In this portion of the experiment two circuits were designed to provide a Q point at $I_{CQ} = 1\text{mA}$ and $V_{CEQ} = 6\text{V}$. Prior to designing the circuits, the actual value of B for each transistor was not known. For this reason, the geometric average of B , or h_{FE} , was used to compute appropriate values of R_B for each circuit.

Since B typically varies from one transistor to another, it is not likely that all three of your transistors have a B value close to the geometric average of h_{FE} . For this reason, you most likely observed changes in the values of I_{CQ} and V_{CEQ} when different transistors were substituted in each circuit.

Since collector feedback partially compensates for changes in B the changes in I_{CQ} and V_{CEQ} in Table E2-2 should be smaller than the corresponding changes in Table E2-1. In the final part of this experiment you will observe the effects of B variations due to changes in temperature.

Procedure (Continued)

13. Examine Table E2-1 and select the transistor whose I_{CQ} and V_{CEQ} values were closest to the desired values of 1 mA and 6V respectively.
14. Using the transistor identified in step 13, construct the base bias circuit in Figure E2-3. Here, $R_C = 5.6k\Omega$ and $R_B = 1.5M\Omega$. You will apply heat to the transistor and observe the change in V_{CE} . However, **before** you actually perform this step, be sure to read the instructions, carefully, so you will know exactly what to do.
15. Record the initial value of V_{CE} .

$$V_{CE} = \text{_____} \text{V.}$$

16. You may use a 20- to 40-watt soldering iron as a source of heat. Make sure the tip of the iron is clean, and that the iron is up to the proper operating temperature. Touch the tip of the iron to the flat side of the transistor and hold it there for exactly 20 seconds. Note the value of V_{CE} at the end of the 20-second period, at the instant you remove the soldering iron.

$$\text{After 20 seconds: } V_{CE} = \text{_____} \text{V.}$$

17. Calculate the percent change in V_{CE} by using the following formula:

$$\% \text{ change} = \frac{V_{CE}(\text{step 15}) - V_{CE}(\text{step 16})}{V_{CE}(\text{step 16})} \times 100.$$

$$\% \text{ change} = \text{_____} \text{ percent.}$$

18. Wait five minutes to allow the transistor to return to room temperature.
19. Construct the collector feedback circuit in Figure E2-4. Here $R_C = 5.6k\Omega$ and $R_B = 0.68M\Omega$. Record the initial value of V_{CE} .

$$V_{CE} = \text{_____} \text{V.}$$

20. Repeat step 16 for the collector feedback circuit. Record the value of V_{CE} after 20 seconds as you did before.

$$\text{After 20 seconds } V_{CE} = \text{_____} \text{V.}$$

21. Calculate the percent change in V_{CE} for the collector feedback circuit.

$$\% \text{ change} = \frac{V_{CE}(\text{step 19}) - V_{CE}(\text{step 20})}{V_{CE}(\text{step 20})} \times 100.$$

$$\% \text{ change} = \text{_____} \text{ percent.}$$

Discussion

Heating the transistor caused the value of B to increase. Since $I_C = B I_B$, I_C also increased when the transistor was heated. In both circuits, the collector-to-emitter voltage, V_{CE} , equals $V_{CC} - I_C R_C$. Consequently, a higher temperature results in a lower V_{CE} value (as you observed in the experiment). This was due to the increase in collector current.

You should have found that the percent of change in V_{CE} calculated in step 21 was less than the percent of change calculated in step 17. This was because the collector feedback circuit partially compensated for the increase in B . Obviously, excessive temperatures should be avoided, so that the collector current does not exceed the maximum safe value.

EXPERIMENT 3

VOLTAGE DIVIDER AND EMITTER BIAS CIRCUITS

Objectives:

To design a voltage divider bias circuit.

To design an emitter bias circuit.

To illustrate the stability of the Q point in each circuit.

To analyze, and experimentally verify the operation of complementary PNP circuits.

Introduction

Linear transistor circuits require stable operating points. Consequently, a biasing scheme must be selected that establishes, and maintains the desired operating point despite unit-to-unit parameter variations, changes in temperature, and parameter variations with time.

Since voltage divider and emitter bias circuits provide very stable operating points, they are the preferred biasing schemes for linear operation. In this experiment, you will investigate the characteristics of these very popular circuits.

Material Required

Heathkit Engineering Design Trainer ET-1000

Multimeter with test leads

Oscilloscope

1 — PNP type 2N3906 transistor (417-874)

1 — NPN type 2N3904 transistor (417-875)

1 — 2.2k Ω , 1/4-watt, 5% resistor

1 — 6.8k Ω , 1/4-watt, 5% resistor

1 — 3.3M Ω , 1/4-watt, 5% resistor

1 — 6.8M Ω , 1/4-watt, 5% resistor

2 — 3.3k Ω , 1/4-watt, 5% resistor

2 — 12k Ω , 1/4-watt, 5% resistor

Procedure

1. In Figure E3-1, $V_{EQ} = 30$ percent of V_{CC} . Calculate the values required for the biasing resistors:

$R_E = \underline{\hspace{2cm}} \text{ k}\Omega, R_C = \underline{\hspace{2cm}} \text{ k}\Omega,$

$R_2 = R_E = \underline{\hspace{2cm}} \text{ k}\Omega, R_1 = \underline{\hspace{2cm}} \text{ k}\Omega.$

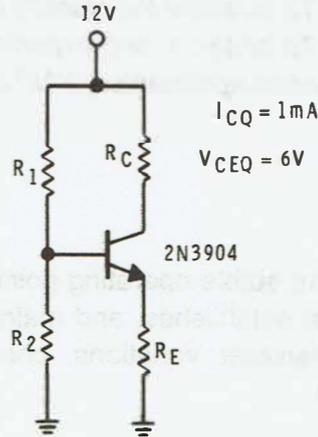


Figure E3-1

Voltage divider bias circuit.

2. Calculate the resistors required for the circuit in Figure E3-2.

$R_B = R_E = \underline{\hspace{2cm}} \text{ k}\Omega \text{ and } R_C = \underline{\hspace{2cm}} \text{ k}\Omega.$

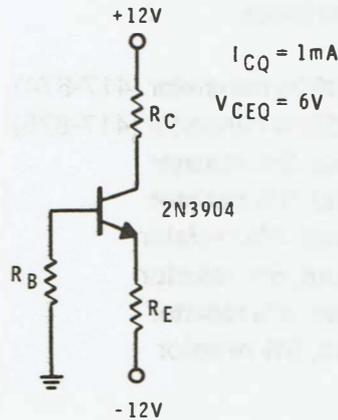


Figure E3-2

Emitter bias circuit.

Discussion

Your calculations should be similar to the following:

Step 1.

Referring to the voltage divider summary guide:

$$V_{EQ} = 0.3(12V) = 3.6V$$

$$R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{3.6V}{1mA} = 3.6k\Omega.$$

$$R_C = \frac{V_{CC} - (V_{EQ} + V_{CEQ})}{I_{CQ}} = \frac{12V - (3.6V + 6V)}{1mA} = 2.4k\Omega.$$

$$R_2 = R_E = 3.6k\Omega.$$

$$R_1 = \frac{R_2(V_{CC} - V_{BQ})}{V_{BQ}}.$$

Since $V_{EQ} = 3.6V$, $V_{BQ} = 0.7V + 3.6V = 4.3V$. Thus:

$$R_1 = \frac{3.6k\Omega(12V - 4.3V)}{4.3V} = 6.45k\Omega.$$

Selecting standard value resistors for the design, you have:

$$R_E = 3.3k\Omega, \quad R_C = 2.2k\Omega.$$

$$R_2 = 3.3k\Omega, \quad R_1 = 6.8k\Omega.$$

Step 2.

Referring to the emitter bias summary guide:

$$R_E = \frac{V_{EE} - V_{BE}}{I_{CQ}} = \frac{12V - 0.7V}{1mA} = 11.3k\Omega = R_B.$$

$$R_C = \frac{(V_{CC} + V_{EE}) - (V_{CEQ} + I_{CQ}R_E)}{I_{CQ}}.$$

$$R_C = \frac{(12V + 12V) - [6V + 1mA(11.3k\Omega)]}{1mA} = 6.7k\Omega.$$

Selecting standard value resistors, you have:

$$R_E = R_B = 12\text{k}\Omega \text{ and } R_C = 6.8\text{k}\Omega.$$

Procedure (Continued)

- Construct the circuit shown in Figure E3-1. Here, $R_E = 3.3\text{k}\Omega$, $R_C = 2.2\text{k}\Omega$, $R_2 = 3.3\text{k}\Omega$, and $R_1 = 6.8\text{k}\Omega$. You will use your oscilloscope to make voltage measurements and your multimeter to measure the collector current, I_C .
- Turn the power on and record the measured values of I_{CQ} , V_B , V_C , and V_E in Table E3-1.

Quantity	Measured Value
I_{CQ}	mA
V_B	V
V_C	V
V_E	V

Table E3-1

Measured values for the voltage divider circuit when
 $R_1 = 6.8\text{k}\Omega$ and $R_2 = 3.3\text{k}\Omega$.

- From the data in Table E3-1 calculate the value of the collector-to-emitter voltage, V_{CE} .

$$V_{CE} = V_C - V_E = \text{_____} \text{ V.}$$

- Turn the power off. Replace R_1 with a $6.8\text{M}\Omega$ resistor and R_2 with a $3.3\text{M}\Omega$ resistor.

7. Turn the power on, and repeat step 4. Record the measured values in Table E3-2.

Quantity	Measured Value
I_{CQ}	mA
V_B	V
V_C	V
V_E	V

Table E3-2

Measured values for the voltage divider circuit when
 $R_1 = 6.8M\Omega$ and $R_2 = 3.3M\Omega$.

8. Calculate the values of $I_{C(SAT)}$ and $V_{CE(CUT)}$ for the voltage divider circuit. Use actual component values for these calculations.

$I_{C(SAT)} = \underline{\hspace{2cm}}$ mA and $V_{CE(CUT)} = \underline{\hspace{2cm}}$ V.

9. Using the values calculated in step 8, sketch the circuit's DC load line in Figure E3-3. Indicate the location of the operating point, Q_1 , based on the data from Table E3-1. Also, indicate the location of the operating point, Q_2 , based on the data from Table E3-2.

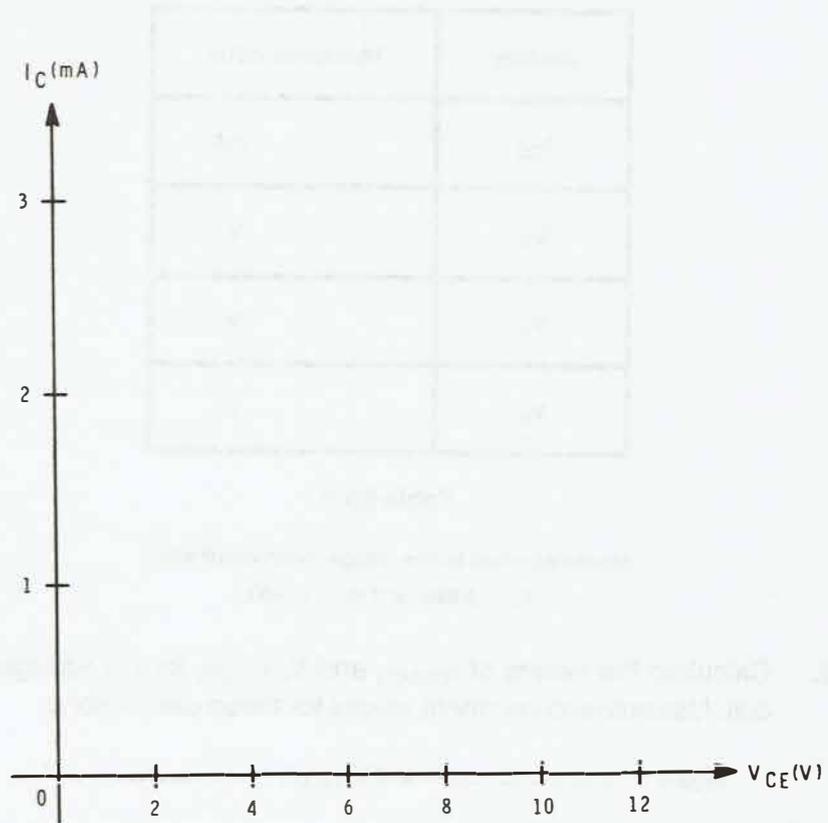


Figure E3-3

DC load line for step 9.

Discussion

This voltage divider circuit was designed to provide the following values:

$$I_{CQ} = 1\text{mA.}$$

$$V_{CEQ} = 6\text{V.}$$

$$V_{EQ} = 3.6\text{V.}$$

$$V_{BQ} = 4.3\text{V.}$$

Also, since $V_C = V_{CC} - I_C R_C$, the quiescent collector voltage is $12\text{V} - 1\text{mA}$ ($2.2\text{k}\Omega$) or 9.8V . Consequently, your data in Table E3-1 and the value of V_{CEQ} obtained in step 5 should be close to the calculated values.

In step 7, $R_1 = 6.8\text{M}\Omega$ and $R_2 = 3.3\text{M}\Omega$. Note that the ratio of R_1 to R_2 is the same as in the original circuit. However, the measured values were very different from those obtained in step 4.

Recall that in our analysis of the voltage divider circuit, we assumed the voltage divider to be unloaded. Specifically, we assumed that the equivalent resistance between the base of the transistor and ground was large when compared to the value of R_2 . Also recall that we recommended you select the value of R_2 so that:

$$R_2 \leq 10R_E.$$

In this case, the inequality just cited clearly is not satisfied, since $3.3\text{M}\Omega$ is **not** equal to or less than $3.3\text{k}\Omega$. For this reason, the voltage divider is loaded down by the relatively small equivalent resistance between the base of the transistor and ground. As a result, the base voltage is considerably less than the 4.3V design value. Naturally, a smaller base voltage results in a smaller emitter voltage, and therefore smaller emitter and collector currents.

In step 8, you calculated the values of $I_{C(\text{SAT})}$ and $V_{CE(\text{CUT})}$. Specifically:

$$I_{C(\text{SAT})} = \frac{V_{CC}}{R_C + R_E} = \frac{12\text{V}}{2.2\text{k}\Omega + 3.3\text{k}\Omega} = 2.18\text{mA.}$$

$$V_{CE(\text{CUT})} = V_{CC} = 12\text{V.}$$

Consequently, your load line, in Figure E3-3 should connect these two points. The operating point, Q_1 , should be near the center of the load line. Also, since the loading of the voltage divider is excessive, the second operating point, Q_2 , should be near the cutoff point.

Procedure (Continued)

10. Construct the voltage divider circuit using $R_E = 3.3\text{k}\Omega$, $R_C = 2.2\text{k}\Omega$, $R_2 = 3.3\text{k}\Omega$, and $R_1 = 6.8\text{k}\Omega$. Turn the power on, and note the value of V_{CE} .

$$V_{CE} = \text{_____V.}$$

11. As you did in Experiment 2, perform the 20-second heating test. If necessary, refer to step 16 of Experiment 2 for the appropriate instructions. Note the value of V_{CE} at the end of the 20-second period. After 20 seconds, $V_{CE} = \text{_____V}$. Turn the power off and wait for the transistor to return to room temperature.

12. Construct the emitter bias circuit in Figure E3-2. Here:

$$R_E = R_B = 12\text{k}\Omega \text{ and } R_C = 6.8\text{k}\Omega.$$

13. Turn the power on and record the measured values of I_{CQ} , V_B , V_C , and V_E in Table E3-3.

Quantity	Measured Value
I_{CQ}	mA
V_B	V
V_C	V
V_E	V

Table E3-3

Measured values for the emitter bias circuit.

14. Calculate the value of V_{CE} using the data in Table E3-3.

$$V_{CE} = V_C - V_E = \text{_____V.}$$

15. Again perform the 20-second heating test. Note the value of V_{CE} before and after the 20-second heating period.

$$V_{CE} \text{ initial} = \text{_____ V.}$$

$$V_{CE} \text{ after 20 seconds} = \text{_____ V.}$$

Turn the power off and wait for the transistor to return to room temperature.

Discussion

Heating the transistors caused the value of B to increase. However, the properly designed voltage divider and emitter feedback circuits provided a Q point that was largely immune to B variations. You should have observed very little change in V_{CE} in steps 11 and 14.

The emitter bias circuit was designed to provide a Q point at:

$$I_{CQ} = 1\text{mA and } V_{CEQ} = 6\text{V.}$$

Using these values, you can calculate V_C as follows:

$$V_C = V_{CC} - I_C R_C = 12\text{V} - 1\text{mA}(6.8\text{k}\Omega) = 5.2\text{V.}$$

Recall that in an NPN emitter bias circuit, V_E is negative and typically has a magnitude less than 1V. A reasonable approximation is to assume $V_E \approx -0.7\text{V}$. Since $V_B = V_{BE} + V_E$, and $V_{BE} \approx 0.7\text{V}$ the base voltage in an emitter bias circuit is approximately 0V.

For these reasons, your data in Table E3-3 and the value of V_{CE} obtained in step 14 should agree with the values just stated.

Procedure (Continued)

16. Figure E3-4 illustrates the complementary PNP circuit for the voltage divider circuit designed earlier. Consequently, $I_{CQ} \approx 1\text{mA}$ and $V_{CEQ} \approx -6\text{V}$. Calculate the terminal-to-ground voltages. Record the calculated values in the appropriate column in Table E3-4.

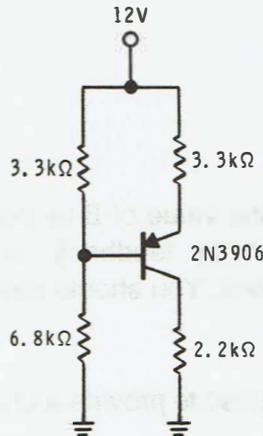


Figure E3-4

Complementary PNP voltage divider circuit.

17. Construct the circuit shown in Figure E3-4. Make sure you use the PNP 2N3906 transistor when you build the circuit. Enter your measured values of V_B , V_C , and V_E in Table E3-4.

Voltage	Calculated Value	Measured Value
V_B	V	V
V_C	V	V
V_E	V	V

Table E3-4

Calculated and measured values for steps 16 and 17.

18. Figure E3-5 illustrates the complementary PNP circuit for the emitter bias circuit previously designed. As before, $I_{CQ} \approx 1\text{mA}$ and $V_{CEQ} \approx -6\text{V}$. Calculate the terminal-to-ground voltages. Record the calculated values in the appropriate column in Table E3-5.

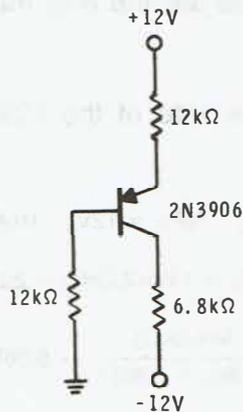


Figure E3-5

Complementary PNP emitter bias circuit.

19. Construct the circuit shown in Figure E3-5. Record your measured values of V_B , V_C , and V_E in Table E3-5.

Voltage	Calculated Value	Measured Value
V_B	V	V
V_C	V	V
V_E	V	V

Table E3-5

Calculated and measured values for steps 18 and 19.

Discussion

In the complementary PNP circuits, the magnitudes of the terminal currents and terminal-to-terminal voltages are essentially the same as those in the original NPN circuits. Note that the current directions and voltage polarities have been reversed. Reversed polarities are the only major differences between NPN and PNP circuits.

In Figure E3-4 the negative side of the 12V supply voltage is the reference, or ground point. Therefore:

$$V_E = V_{CC} - I_E R_E = 12V - 1mA(3.3k\Omega) = 8.7V.$$

$$V_C = I_C R_C = 1mA(2.2k\Omega) = 2.2V.$$

$$V_B = \frac{V(6.8k\Omega)}{3.3k\Omega + 6.8k\Omega} = 8.08V.$$

Your calculations for step 16 should be similar to these calculations. In addition, your measured values in step 17 should generally agree with these calculations.

In Figure E3-5, the collector-to-ground voltage, V_E is:

$$V_C = I_C R_C - V_{CC} = 1mA(6.8k\Omega) - 12V = -5.2V.$$

In a PNP emitter bias circuit, V_E is positive and approximately equal to 0.7V. Also, since V_{BE} is negative, the base-to-ground voltage is approximately 0V. Your calculated values in step 18, and measured values in step 19 should be close to the values just stated.

EXPERIMENT 4

× 10 COMMON-EMITTER VOLTAGE AMPLIFIER

Objective: *To design and experimentally verify the operation of a typical × 10 common-emitter voltage amplifier.*

Introduction

In this experiment, you are to design a common-emitter voltage amplifier according to the following specifications.

Voltage gain = 10. The voltage gain should not vary greatly with variations in h_{FE} and r_e' .

Load resistance = $2.2k\Omega$

Lowest signal frequency = 100Hz.

Supply voltage = 20V.

Quiescent collector current = 3mA.

Since the voltage gain must be stable with respect to variations in h_{FE} and r_e' , and since a single supply is specified, a voltage divider biasing scheme is selected for the design.

Material Required

Heathkit Engineering Design Trainer ET-1000

Multimeter with test leads

Oscilloscope

1 — NPN type 2N3904 transistor (417-875)

1 — 120Ω , 1/4-watt, 5% resistor

1 — $1k\Omega$, 1/4-watt, 5% resistor

1 — $2.2k\Omega$, 1/4-watt, 5% resistor

1 — $3.3k\Omega$, 1/4-watt, 5% resistor

1 — $3.9k\Omega$, 1/4-watt, 5% resistor

2 — $1.5k\Omega$, 1/4-watt, 5% resistors

3 — $47\mu F$, 50V, electrolytic capacitors

Procedure

Refer to the voltage divider circuit in the design guide provided in Unit 3. Following the steps in the design guide, proceed as follows.

1. $I_{CQ} = 3\text{mA}$.

2. $r_e' = \frac{37\text{mV}}{I_{CQ}} = \frac{37\text{mV}}{3\text{mA}} = \underline{\hspace{2cm}} \Omega$.

3. $R_{E_1} = 10r_e' = \underline{\hspace{2cm}} \Omega$.

4. $r_L = A_V(R_{E_1} + r_e') = \underline{\hspace{2cm}} \text{k}\Omega$.

5. $R_C = \frac{R_L r_L}{R_L - r_L} = \underline{\hspace{2cm}} \text{k}\Omega$.

6. $V_{CEQ} = I_{CQ}(R_{E_1} + r_L) = \underline{\hspace{2cm}} \text{V}$.

7. $V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CEQ}] = \underline{\hspace{2cm}} \text{V}$.

8. $R_E = V_{EQ}/I_{CQ} = \underline{\hspace{2cm}} \text{k}\Omega$.

9. $R_{E_2} = R_E - R_{E_1} = \underline{\hspace{2cm}} \text{k}\Omega$.

10. Select $R_2 = 1.5\text{k}\Omega$.

11. $R_1 = \frac{R_2(V_{CC} - V_{BQ})}{V_{BQ}} = \underline{\hspace{2cm}} \text{k}\Omega$.

12. Assume $h_{fe} = 100$.

$$R_{IN(\text{BASE})} = h_{fe}(R_{E_1} + r_e') = \underline{\hspace{2cm}} \text{k}\Omega$$

$$R_B = R_1 \parallel R_2 = \underline{\hspace{2cm}} \text{k}\Omega$$

$$R_{IN} = R_B \parallel R_{IN(\text{BASE})} = \underline{\hspace{2cm}} \text{k}\Omega$$

$$C_1 = \frac{3.18}{F_1 R_{IN}} = \underline{\hspace{2cm}} \mu\text{F}$$

$$C_2 = \frac{3.18}{F_1 R_C} = \underline{\hspace{2cm}} \mu\text{F}$$

$$C_3 = \frac{3.18}{F_1 R_{E_2}} = \underline{\hspace{2cm}} \mu\text{F}$$

Discussion

Steps 1 through 12 outline the design process. Your calculations should be similar to the following:

$$1. \quad I_{CQ} = 3\text{mA}.$$

$$2. \quad r_e' = \frac{37\text{mV}}{I_{CQ}} = \frac{37\text{mV}}{3\text{mA}} = 12.3\Omega.$$

$$3. \quad R_{E_1} = 10r_e' = 10(12.3\Omega) = 123\Omega.$$

$$4. \quad r_L = A_V(R_{E_1} + r_e') = 10(123\Omega + 12.3\Omega) = 1.35\text{k}\Omega.$$

$$5. \quad R_C = \frac{R_L r_L}{R_L - r_L} = \frac{2.2\text{k}\Omega(1.35\text{k}\Omega)}{2.2\text{k}\Omega - 1.35\text{k}\Omega} = 3.49\text{k}\Omega.$$

$$6. \quad V_{CEQ} = I_{CQ}(R_{E_1} + r_L) = 3\text{mA}(123\Omega + 1.35\text{k}\Omega) = 4.42\text{V}.$$

$$\begin{aligned} 7. \quad V_{EQ} &= V_{CC} - [I_{CQ}R_C + V_{CEQ}] \\ &= 20\text{V} - [3\text{mA}(3.49\text{k}\Omega) + 4.42\text{V}] \\ &= 20\text{V} - 14.89\text{V} \\ &= 5.11\text{V}. \end{aligned}$$

$$8. \quad R_E = V_{EQ}/I_{CQ} = 5.11\text{V}/3\text{mA} = 1.7\text{k}\Omega.$$

$$9. \quad R_{E_2} = R_E - R_{E_1} = 1.7\text{k}\Omega - 123\Omega = 1.58\text{k}\Omega.$$

10. $R_2 \leq 10R_E$. Since $R_E = 1.7\text{k}\Omega$ a standard value $1.5\text{k}\Omega$ resistor is a reasonable choice for R_2 .

$$11. \quad \text{With } V_{EQ} = 5.11\text{V}, V_{BQ} = 5.11\text{V} + 0.7\text{V} = 5.81\text{V}.$$

$$R_1 = \frac{R_2[V_{CC} - V_{BQ}]}{V_{BQ}} = 1.5\text{k}\Omega \frac{[20\text{V} - 5.81\text{V}]}{5.81\text{V}} = 3.66\text{k}\Omega.$$

12. For most general purpose BJT's, it is reasonable, for the purpose of initial calculation, to assume $h_{fe} = 100$. Thus:

$$R_{IN(BASE)} = h_{fe}(R_{E_1} + r_e') = 100(123\Omega + 12.3\Omega) = 13.53\text{k}\Omega.$$

$$R_B = R_1 \parallel R_2 = 3.66\text{k}\Omega \parallel 1.5\text{k}\Omega = 1.06\text{k}\Omega.$$

$$R_{IN} = R_B \parallel R_{IN(BASE)} = 1.06\text{k}\Omega \parallel 13.53\text{k}\Omega = 983\Omega.$$

The minimum capacitor values are:

$$C_1 = \frac{3.18}{F_1 R_{IN}} = \frac{3.18}{100(983)} = 32.3\mu\text{F}.$$

$$C_2 = \frac{3.18}{F_1 R_L} = \frac{3.18}{100(2.2\text{k}\Omega)} = 14.45\mu\text{F}.$$

$$C_3 = \frac{3.18}{F_1 R_{E_2}} = \frac{3.18}{100(1.58\text{k}\Omega)} = 20.1\mu\text{F}.$$

In addition, the capacitor voltage ratings should exceed the following values:

$$V_{C_1} > V_{BQ} \text{ Thus } V_{C_1} > 5.81\text{V}.$$

$$V_{C_2} > V_{CQ} \text{ Thus } V_{C_2} > 20 - 3\text{mA}(3.49\text{k}\Omega).$$

$$V_{C_2} > 9.53\text{V}.$$

$$V_{C_3} > V_{EQ} \text{ Thus } V_{C_3} > 5.11\text{V}.$$

It is a good idea to select capacitors that are larger than the minimum values. We selected three $47\mu\text{F}$, 50V electrolytic capacitors for this design.

The following table summarizes the calculated resistor values, and the standard value resistors selected for the actual circuit.

Resistor	Calculated Value	Standard Value
R_1	$3.66\text{k}\Omega$	$3.9\text{k}\Omega$
R_2	$1.5\text{k}\Omega$	$1.5\text{k}\Omega$
R_C	$3.49\text{k}\Omega$	$3.3\text{k}\Omega$
R_{B_1}	123Ω	120Ω
R_{E_2}	$1.58\text{k}\Omega$	$1.5\text{k}\Omega$

Table E4-1

Calculated and standard resistor values.

Procedure (Continued)

13. With the power off, construct the circuit shown in Figure E4-1. Be sure to observe the correct polarity when placing the electrolytic capacitors in the circuit. Also, note that the $100\text{k}\Omega$ potentiometer on the ET-1000 Trainer is used as a variable voltage divider.

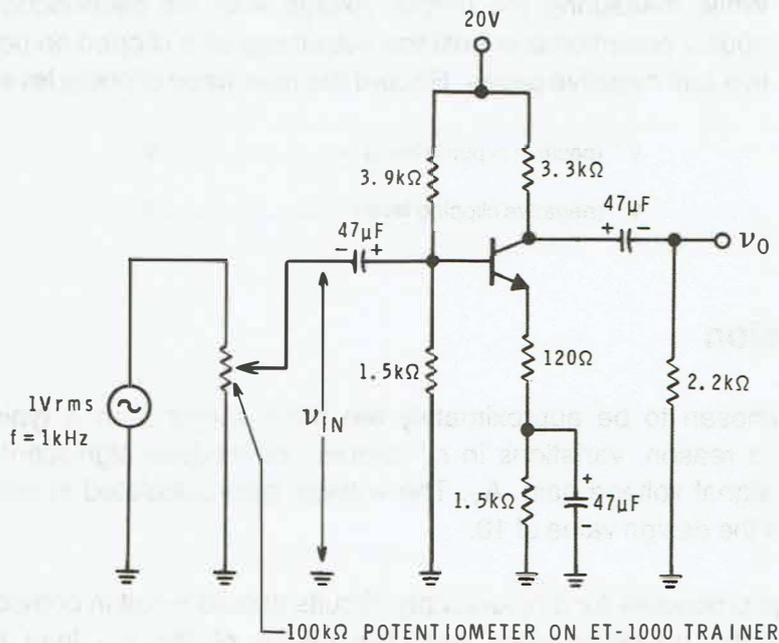


Figure E4-1

$\times 10$ common-emitter voltage amplifier.

14. Turn the power on, and adjust the supply voltage to $+20\text{V}$.
15. Adjust the $100\text{k}\Omega$ potentiometer to obtain an input voltage, v_{IN} of 0.1V peak. The frequency of the input signal should be 1kHz .
16. Use the oscilloscope to measure the peak output voltage. If you have a dual-trace oscilloscope, you can simultaneously measure the input and output voltage. In this case, you should observe a 180° phase difference between the input and output signals.

$v_{\text{O}} = \text{_____ V peak.}$

17. Calculate the measured value of the voltage gain.

$$A_v = \frac{v_o(\text{step 16})}{0.1\text{V}} = \underline{\hspace{2cm}}$$

This value, should be reasonably close to 10, since this is the value the amplifier was designed for.

18. While measuring the output voltage with the oscilloscope, vary the $100\text{k}\Omega$ potentiometer until the output signal is clipped on both the positive and negative peaks. Record the measured clipping levels.

$$V^+ \text{ (positive clipping level)} = \underline{\hspace{2cm}} \text{ V.}$$

$$V^- \text{ (negative clipping level)} = \underline{\hspace{2cm}} \text{ V.}$$

Discussion

R_{E1} was chosen to be approximately ten times larger than a typical value of r_e' . For this reason, variations in r_e' should not produce significant changes in the small signal voltage gain, A_v . The voltage gain calculated in step 17 should be close to the design value of 10.

The design procedure for single-supply circuits should result in component values that place the operating point near the center of the AC load line. Ideally, $V^+ = V^- = V_{CEQ}$ or 4.42V for the circuit designed in steps 1 through 12.

Due to component tolerance, the values of V^+ and V^- measured in step 18 probably differ from the ideal $\pm 4.42\text{V}$ values. Nevertheless, you should have observed that the positive and negative clipping levels in step 18 were approximately equal. Also, the actual clipping levels will typically be within $\pm 1\text{V}$ of the ideal values.

By carefully observing the output waveform as you increase v_{IN} , you should note that one or both output peaks tend to "round off" as the clipping levels are approached. This rounding of the output peaks indicates the presence of nonlinear distortion. For small signal operation, the swing in the output voltage is usually restricted to values well below the clipping levels. In this way, the effects of nonlinear distortion are minimized.

Procedure (Continued)

19. The data sheet for a 2N3904 lists the minimum and maximum values of h_{fe} as 100 and 400 respectively. These values are given for: $I_C = 1\text{mA}$, $V_{CE} = 10\text{V}$, and $f = 1\text{kHz}$. Even though I_{CQ} and V_{CEQ} are different from these values, you can use the data sheet values as approximations of the probable spread in h_{fe} .

Using the component values in Figure E4-1, calculate the minimum and maximum values you would expect for R_{IN} .

$$R_{IN(MIN)} = \text{_____} \text{ k}\Omega, \quad R_{IN(MAX)} = \text{_____} \text{ k}\Omega.$$

20. Insert a $1\text{k}\Omega$ resistor in series with the amplifier input lead as shown in Figure E4-2. Note that the amplifier acts like a resistance equal to R_{IN} when viewed from the signal source.

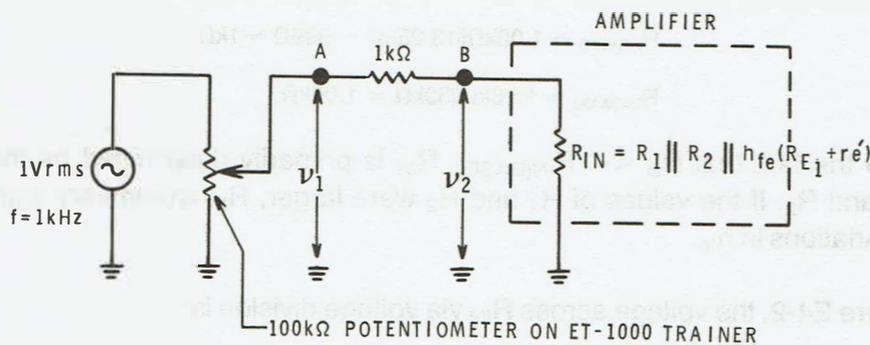


Figure E4-2

By measuring v_1 and v_2 you can determine the amplifier's input resistance, R_{IN} .

21. Adjust the $100\text{k}\Omega$ potentiometer so that $v_1 = 0.2\text{V}$ peak. Now measure the voltage from point B to ground.

$$v_1 = v_A = .2\text{V peak.}$$

$$v_2 = v_B = \text{_____} \text{ V peak.}$$

22. Use the following formula to calculate the amplifier's input resistance.

$$R_{IN} = \frac{v_2 R}{v_1 - v_2} = \text{_____} \text{ k}\Omega.$$

Discussion

Your calculations for step 19 should be similar to the following:

$$R_B = R_1 \parallel R_2 = 3.9\text{k}\Omega \parallel 1.5\text{k}\Omega = 1.08\text{k}\Omega.$$

$$R_{E_1} + r_{e'} = 120\Omega + 12.5\Omega = 132.5\Omega.$$

When $h_{fe} = 100$:

$$R_{IN(BASE)} = 100(132.5\Omega) = 13.25\text{k}\Omega.$$

When $h_{fe} = 400$:

$$R_{IN(BASE)} = 400(132.5\Omega) = 53\text{k}\Omega.$$

Since $R_{IN} = R_B \parallel R_{IN(BASE)}$:

$$R_{IN(MIN)} = 1.08\text{k}\Omega \parallel 13.25\text{k}\Omega = 999\Omega \approx 1\text{k}\Omega.$$

$$R_{IN(MAX)} = 1.08\text{k}\Omega \parallel 53\text{k}\Omega = 1.06\text{k}\Omega.$$

Due to the fact that $R_B \ll R_{IN(BASE)}$, R_{IN} is primarily determined by the values of R_1 and R_2 . If the values of R_1 and R_2 were larger, R_{IN} would vary significantly with variations in h_{fe} .

In Figure E4-2, the voltage across R_{IN} via voltage division is:

$$v_2 = v_1 \left(\frac{R_{IN}}{R + R_{IN}} \right).$$

If you solve this expression for R_{IN} , you obtain the formula given in step 22. This is a simple, but useful, formula that can be used to calculate an amplifier's input resistance from experimental data.

Based on the calculations in step 19, you should have obtained a value for R_{IN} of approximately $1\text{k}\Omega$ in step 22.

Procedure (Continued)

23. Remove the $1\text{k}\Omega$ resistor used in step 20. Adjust the $100\text{k}\Omega$ potentiometer to obtain an input voltage of 0.2V peak-to-peak. Remove the $2.2\text{k}\Omega$ load resistor, R_L , and then measure the peak-to-peak output voltage.

$$v_O = \text{_____ V peak-to-peak} = v_{TH}$$

24. Reconnect the $2.2\text{k}\Omega$ load resistor. Then measure the peak-to-peak output voltage.

$$v_O = \text{_____ V peak-to-peak} = v_L$$

25. Use the following formula to calculate the amplifier's output resistance.

$$R_O = \frac{(v_{TH} - v_L)R_L}{v_L} = \text{_____ k}\Omega$$

Discussion

When viewed from the load terminals an amplifier can be modeled by a Thevenin equivalent circuit. When $R_L = \infty$ the output voltage equals v_{TH} as shown in Figure E4-3A.

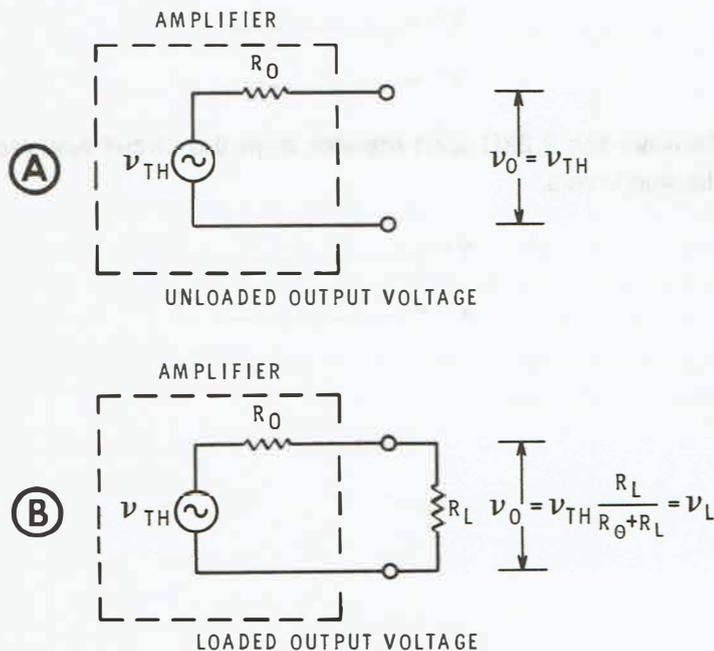


Figure E4-3

By measuring v_O with and without a load resistor, R_L , you can determine the amplifier's output resistance, R_O .

With R_L connected across the output terminals, the output voltage depends upon the values of v_{TH} , R_O , and R_L as shown in Figure E4-3B. The load voltage via voltage division is:

$$v_L = v_{TH} \left(\frac{R_L}{R_O + R_L} \right)$$

By solving this expression for R_O , you obtain the formula given in step 25.

The output resistance of a common-emitter amplifier is approximately equal to the value of the collector resistor, R_C . Thus, when you calculated R_O in step 25, you should have obtained a value for R_O of approximately $3.3k\Omega$.

Generally speaking, the methods used in this experiment to measure R_{IN} and R_O provide values that are within 20% of the actual values.

Procedure (Continued)

26. Adjust the $100k\Omega$ potentiometer shown in Figure E4-1 so that the output voltage is clipped on both the positive and negative peaks. This is exactly what you did previously in step 18.
27. Predict the clipping levels you would expect if $R_L = \infty$.

$$V^+ = \underline{\hspace{2cm}}$$

$$V^- = \underline{\hspace{2cm}}$$

28. Remove the $2.2k\Omega$ load resistor from the circuit and record the actual clipping levels.

$$V^+ = \underline{\hspace{2cm}}$$

$$V^- = \underline{\hspace{2cm}}$$

Discussion

As discussed previously, the clipping levels observed in step 26 should be approximately equal to $\pm 4.42\text{V}$. When we designed the original circuit, in steps 1 through 12, we used the following values:

$$I_{CQ} = 3\text{mA.}$$

$$V_{CEQ} = 4.42\text{V.}$$

$$R_C = 3.49\text{k}\Omega.$$

$$R_{E1} = 123\Omega.$$

$$R_L = 2.2\text{k}\Omega.$$

$$r_L = 1.35\text{k}\Omega.$$

Using these numbers, let's predict the clipping levels, assuming $R_L = \infty$, which is equivalent to "removing R_L from the circuit."

Since $r_L = R_C \parallel R_L$, when $R_L = \infty$, you have:

$$r_L = R_C \parallel \infty = R_C \text{ or } 3.49\text{k}\Omega.$$

Ideally, the value of r_L should not affect the DC currents and voltages. Consequently, I_{CQ} and V_{CEQ} are assumed to be 3mA and 4.42V respectively. Thus:

$$V^- = V_{CEQ} = 4.42\text{V, as before.}$$

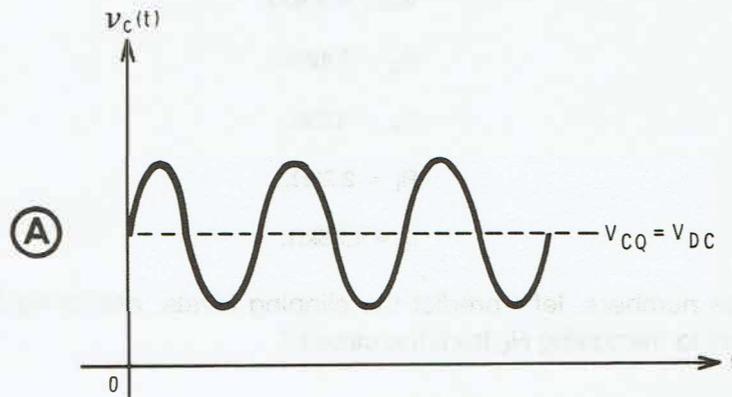
The positive clipping level is determined by:

$$V^+ = I_{CQ}(R_{E1} + r_L).$$

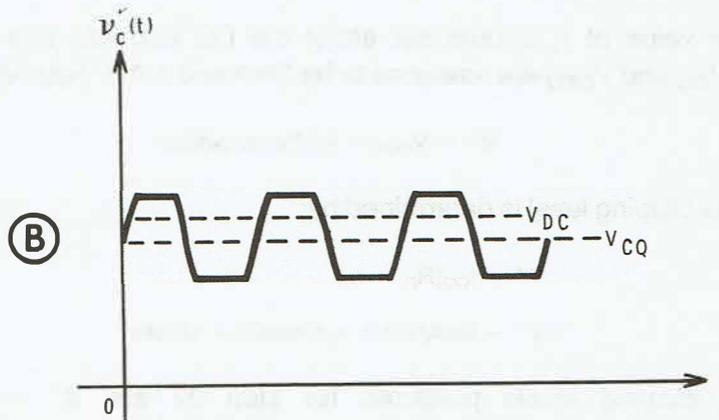
$$V^+ = 3\text{mA}(123\Omega + 3.49\text{k}\Omega) = 10.84\text{V.}$$

Thus, the clipping levels predicted for step 27 are $V^+ = 10.84\text{V}$, and $V^- = 4.42\text{V}$. The values you observed in step 28 should be reasonably close to the calculated values.

When R_L was removed from the circuit in step 28, you probably noticed a small change in the negative clipping level. This change occurred because the AC collector voltage is no longer symmetrical above and below the DC collector voltage level. Specifically, the area above V_{CQ} is larger than the area below V_{CQ} as shown in Figure E4-4B. This changes the average, DC, value of the collector voltage, which in turn changes the DC collector-to-emitter voltage. Since V_{CE} changes, the value of the negative clipping level must also change.



SYMMETRICAL AC COLLECTOR
VOLTAGE $V_{DC} = V_{CQ}$



NON SYMMETRICAL AC COLLECTOR
VOLTAGE $V_{DC} \neq V_{CQ}$

Figure E4-4

When the AC collector voltage is symmetrical, the average, DC, collector voltage equals V_{CQ} . However, if the AC collector voltage is non-symmetrical, the average, DC, collector voltage no longer equals V_{CQ} .

- A. Symmetrical AC collector voltage $V_{DC} = V_{CQ}$.
- B. Non-symmetrical AC collector voltage $V_{DC} \neq V_{CQ}$.

To accurately predict this change in the clipping level, a rather complex analysis is required. This effect is much more pronounced in high gain amplifiers since a small change in the input voltage produces a relatively large change in the collector voltage.

Naturally, this "problem" can be avoided by restricting the input signal to values that do not result in a clipped output signal.

EXPERIMENT 5

× 100 COMMON-EMITTER VOLTAGE AMPLIFIER

Objective:

To design and experimentally verify the operation of a high gain common-emitter voltage amplifier.

Introduction

In this experiment, you are to design a common-emitter voltage amplifier according to the following specifications.

Typical voltage gain = 100. Large unit-to-unit variations are permissible. A given unit however, should have a minimum gain of 50.

Load resistance = 10k Ω .

Lowest signal frequency = 100Hz.

Supply voltage = 12V.

Quiescent collector current = 2mA.

Considering the gain and stability requirements, select a collector and emitter feedback circuit for the design. Naturally, the emitter resistor will be fully bypassed due to the high gain requirements.

Material Required

Heathkit Engineering Design Trainer ET-1000

Oscilloscope

1 — NPN type 2N3904 transistor (417-875)

1 — 1.8k Ω , 1/4-watt, 5% resistor

1 — 2.2k Ω , 1/4-watt, 5% resistor

1 — 10k Ω , 1/4-watt, 5% resistor

1 — 270k Ω , 1/4-watt, 5% resistor

3 — 47 μ F, 50V, electrolytic capacitors

1 — 100k Ω potentiometer located on Trainer

Procedure

Refer to the collector and emitter feedback circuit in the Design Guide provided in Unit 3. Following the steps in the Design Guide, proceed as follows:

1. $I_{CQ} = 2\text{mA}$.
2. $r_{e'} = \frac{37\text{mV}}{I_{CQ}} = \frac{37\text{mV}}{2\text{mA}} = 18.5\Omega$.
3. $R_{E_1} = 0$ since the emitter resistor is fully bypassed.
4. $r_L = A_V(R_{E_1} + r_{e'}) = \text{_____} \text{k}\Omega$.
5. $R_C = \frac{R_L r_L}{R_L - r_L} = \text{_____} \text{k}\Omega$.
6. $V_{CEQ} = I_{CQ}(R_{E_1} + r_L) = \text{_____} \text{V}$.
7. $V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CEQ}] = \text{_____} \text{V}$.
8. $R_E = V_{EQ}/I_{CQ} = \text{_____} \text{k}\Omega$.
9. $R_{E_2} = R_E$ since $R_{E_1} = 0$.
10. Assume $h_{fe} = 200$ to calculate I_{BQ} .
11. $R_{IN(BASE)} = h_{fe}(R_{E_1} + r_{e'}) = \text{_____} \text{k}\Omega$.

$$R_B = R_{B'} = \frac{R_B}{A_V + 1} = \text{_____} \text{k}\Omega$$

$$R_{IN} = R_B || R_{IN(BASE)} = \text{_____} \text{k}\Omega$$

$$C_1 = \frac{3.18}{F_1 R_{IN}} = \text{_____} \mu\text{F}$$

$$C_2 = \frac{3.18}{F_1 R_L} = \text{_____} \mu\text{F}$$

$$C_3 = \frac{3.18}{F_1 R_E} = \text{_____} \mu\text{F}$$

Discussion

Steps 1 through 11 outline the design process. Your calculations should be similar to the following:

$$1. \quad I_{CQ} = 2\text{mA}.$$

$$2. \quad r_{e'} = \frac{37\text{mV}}{I_{CQ}} = \frac{37\text{mV}}{2\text{mA}} = 18.5\Omega.$$

$$3. \quad R_{E_1} = 0.$$

$$4. \quad r_L = A_V(R_{E_1} + r_{e'}) = 100(0 + 18.5\Omega) = 1.85\text{k}\Omega.$$

$$5. \quad R_C = \frac{R_L r_L}{R_L - r_L} = \frac{10\text{k}\Omega(1.85\text{k}\Omega)}{10\text{k}\Omega - 1.85\text{k}\Omega} = 2.27\text{k}\Omega.$$

$$6. \quad V_{CEQ} = I_{CQ}(R_{E_1} + r_L) = 2\text{mA}(0 + 1.85\text{k}\Omega) = 3.7\text{V}.$$

$$\begin{aligned} 7. \quad V_{EQ} &= V_{CC} - [I_{CQ}R_C + V_{CEQ}]. \\ &= 12\text{V} - [2\text{mA}(2.27\text{k}\Omega) + 3.7\text{V}]. \\ &= 12\text{V} - 8.24\text{V}. \\ &= 3.76\text{V}. \end{aligned}$$

$$8. \quad R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{3.76\text{V}}{2\text{mA}} = 1.88\text{k}\Omega.$$

$$9. \quad R_{E_2} = R_E = 1.88\text{k}\Omega.$$

$$10. \quad I_{BQ} = \frac{I_{CQ}}{h_{fe}} = \frac{2\text{mA}}{200} = 10\mu\text{A}.$$

$$R_B = \frac{V_{CEQ} - V_{BE}}{I_{BQ}} = \frac{3.7\text{V} - 0.7\text{V}}{10\mu\text{A}} = 300\text{k}\Omega.$$

$$11. R_{IN(BASE)} = h_{fe}(R_{E_1} + r_{e'}) = 200(0 + 18.5\Omega) = 3.7k\Omega.$$

$$R_B = R_{B'} = \frac{R_B}{A_V + 1} = \frac{300k\Omega}{101} = 2.97k\Omega.$$

$$R_{IN} = R_B || R_{IN(BASE)} = 2.97k\Omega || 3.7k\Omega = 1.65k\Omega.$$

$$C_1 = \frac{3.18}{F_1 R_{IN}} = \frac{3.18}{100(1.65k\Omega)} = 19.3\mu F.$$

$$C_2 = \frac{3.18}{F_1 R_L} = \frac{3.18}{100(10k\Omega)} = 3.18\mu F.$$

$$C_3 = \frac{3.18}{F_1 R_E} = \frac{3.18}{100(1.88k\Omega)} = 16.9\mu F.$$

The calculated capacitor values are minimum values. The capacitor voltage ratings should exceed:

$$V_{C_1} > V_{BQ} \text{ Thus, } V_{C_1} > (V_{EQ} + V_{BE}) \text{ or } 4.46V.$$

$$V_{C_2} > V_{CQ} \text{ Thus, } V_{C_2} > [12V - 2mA(2.27k\Omega)] \text{ or } 7.46V.$$

$$V_{C_3} > V_{EQ} \text{ Thus, } V_{C_3} > 3.76V.$$

As in Experiment 4, we select three 47 μ F, 50V, electrolytic capacitors for the design.

The following table summarizes the calculated resistor values, and the standard value resistors selected for the actual circuit.

RESISTOR	CALCULATED VALUE	STANDARD VALUE
R_C	2.27k Ω	2.2k Ω
R_E	1.88k Ω	1.8k Ω
R_B	300k Ω	270k Ω

Table E5-1

Calculated and standard resistor values.

The data sheet for a 2N3904 lists the minimum and maximum values of h_{fe} as 100 and 400 respectively, for $I_C = 1\text{mA}$, $V_{CE} = 10\text{V}$, and $F = 1\text{kHz}$. Similarly, $h_{fe(\text{MIN})}$ is given as 70, for $I_C = 1\text{mA}$ and $V_{CE} = 1\text{V}$. No maximum value of h_{fe} is listed for these conditions. Since both h_{FE} and h_{fe} vary widely from unit to unit, we assumed both h_{FE} and h_{fe} were approximately 200 in steps 10 and 11.

Procedure (Continued)

- With the power off, construct the circuit shown in Figure E5-1. Make sure the electrolytic capacitors are inserted with the correct polarity.

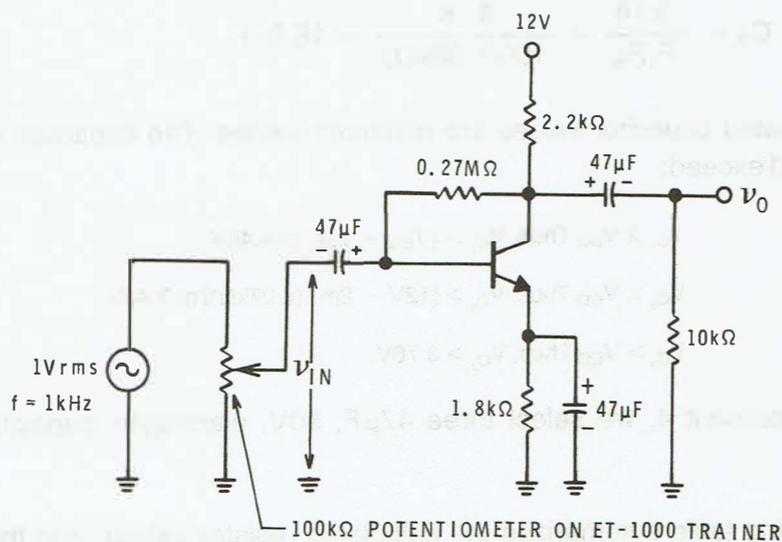


Figure E5-1

× 100 common-emitter voltage amplifier.

- Turn the power on and adjust the 100kΩ potentiometer so that v_{IN} equals 10mV peak-to-peak. The frequency of the input signal should be 1kHz.
- Use the oscilloscope to measure the peak-to-peak output voltage.

$$v_O = \text{_____ V peak-to-peak.}$$

- Calculate the measured value of the voltage gain.

$$A_V = \frac{v_O(\text{step 14})}{10\text{mV}} = \text{_____}$$

16. Assuming $100 \leq h_{FE} \leq 400$, calculate the minimum and maximum values you would expect for R_{IN} . Use the component values in Figure E5-1 for your calculations.

$$R_{IN(MIN)} = \text{_____} \text{ k}\Omega, \quad R_{IN(MAX)} = \text{_____} \text{ k}\Omega.$$

17. As you did in Experiment 4, insert a $1\text{k}\Omega$ resistor in series with the amplifier input lead. If necessary, refer to Figure E4-2.
18. Adjust the $100\text{k}\Omega$ potentiometer so that $v_1 = 400\text{mV}$ peak-to-peak. Measure v_2 .

$$v_2 = \text{_____} \text{ V peak-to-peak.}$$

19. Calculate the amplifier's input resistance.

$$R_{IN} = \frac{v_2(1\text{k}\Omega)}{v_1 - v_2} = \text{_____} \text{ k}\Omega.$$

20. Remove the $1\text{k}\Omega$ resistor used in steps 17 through 20. Replace the $2.2\text{k}\Omega$ load resistor with this $1\text{k}\Omega$ resistor.
21. Adjust the $100\text{k}\Omega$ potentiometer so that v_O is 0.4V peak-to-peak. We will call this value of v_O , v_L .
22. Remove the $1\text{k}\Omega$ resistor, and note the peak-to-peak value of the output voltage. We will call this value of v_O , v_{TH} .

$$v_{TH} = \text{_____} \text{ V peak-to-peak.}$$

23. Calculate the amplifier's output resistance.

$$R_O = \frac{(v_{TH} - v_L)1\text{k}\Omega}{v_L} = \text{_____} \text{ k}\Omega.$$

Discussion

In Experiment 4, it was relatively easy to estimate values for $R_{IN(MIN)}$ and $R_{IN(MAX)}$. In this case however, the process is more complex due to the following reasons:

- Since the circuit uses collector feedback, the value of R_B' depends upon the actual value of a particular unit's voltage gain. Recall that:

$$R_B' = \frac{R_B}{A_V + 1}$$

- In this case, $A_V = r_L/r_e'$. Since r_e' varies widely from unit to unit, you can expect large unit-to-unit variations in A_V .
- It is assumed that $100 \leq h_{FE} \leq 400$. Since $R_{IN(BASE)} = h_{FE}r_e'$ you will find large unit-to-unit variations in $R_{IN(BASE)}$.

Therefore, to accurately predict the range of the unit-to-unit values of R_{IN} , you must take all of the previous factors into account. To begin, let's consider the expected variations in gain due to variations in r_e' .

Recall that r_e' typically is such that:

$$\frac{26\text{mV}}{I_{CQ}} \leq r_e' \leq \frac{52\text{mV}}{I_{CQ}}$$

$$\text{If } r_e' = \frac{26\text{mV}}{I_{CQ}} = \frac{26\text{mV}}{2\text{mA}} = 13\Omega$$

$$\text{Then } A_V = \frac{r_L}{r_e'} = \frac{2.2\text{k}\Omega \parallel 10\text{k}\Omega}{13\Omega} = 138.7$$

$$\text{Similarly, if } r_e' = \frac{52\text{mV}}{I_{CQ}} = \frac{52\text{mV}}{2\text{mA}} = 26\Omega$$

$$\text{Then } A_V = \frac{r_L}{r_e'} = \frac{2.2\text{k}\Omega \parallel 10\text{k}\Omega}{26\Omega} = 69.4$$

The expected range in the unit-to-unit voltage gains is 69.4 to 138.7. Recall that the specifications stated that a particular unit should have a minimum gain of 50.

Since $R_B' = \frac{R_B}{A_V + 1}$, the expected range in values of R_B' is:

$$R_B' = \frac{270\text{k}\Omega}{139.7} = 1.93\text{k}\Omega, \text{ to } \frac{270\text{k}\Omega}{70.4} = 3.84\text{k}\Omega.$$

Since $100 \leq h_{fe} \leq 400$, you can expect unit-to-unit variations in $R_{IN(BASE)}$ to be between:

$$R_{IN(BASE)} = 100(r_e'_{(MIN)}), \text{ to } 400(r_e'_{(MAX)}). \\ = 100(13\Omega) = 1.3\text{k}\Omega, \text{ to } 400(26\Omega) = 10.4\text{k}\Omega.$$

A summary of the calculations to date is provided in Figure E5-2. Here, the arrow means "produce."

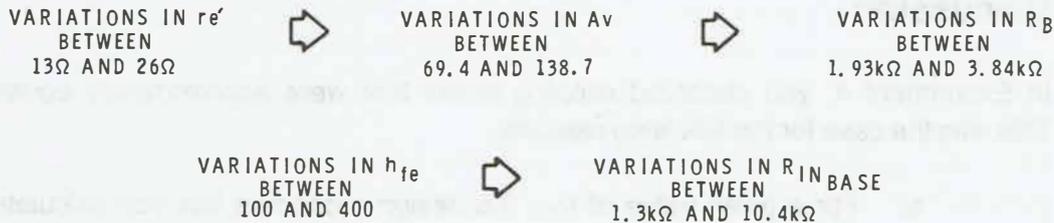


Figure E5-2

Summary of partial calculations for step 16.

Since $R_{IN} = R_B || R_{IN(BASE)}$ the expected range of variations in R_{IN} are:

$$R_{IN} = 1.93\text{k}\Omega || 1.3\text{k}\Omega = 780\Omega, \text{ to } 3.84\text{k}\Omega || 10.4\text{k}\Omega = 2.72\text{k}\Omega.$$

Based upon this rather lengthy analysis, the value of R_{IN} obtained in step 19 probably was between 780Ω and $2.72\text{k}\Omega$. The resistor tolerance and measurement accuracy could account for up to an additional 15 percent variation from the calculated values.

The procedure for measuring the amplifier's output resistance in steps 20 through 23 was similar to the technique employed in Experiment 4. The $1\text{k}\Omega$ resistor was used so that the difference between v_L and v_{TH} would be large enough to obtain accurate data. Since $R_O \approx R_C$, the value obtained in step 23 should be approximately equal to $2.2\text{k}\Omega$.

Procedure (Continued)

24. Reinstall the $2.2\text{k}\Omega$ load resistor. Adjust the $100\text{k}\Omega$ potentiometer so that the AC output voltage is minimum.
25. *Slowly* turn the $100\text{k}\Omega$ potentiometer until clipping just occurs on one peak of the output voltage. Record the value of this clipping level.

$$V_{\text{CLIP}} = \text{_____} \text{V.}$$

26. Continue to turn the $100\text{k}\Omega$ potentiometer until both peaks of the AC output voltage are clearly clipped. Does the clipping level observed in step 25 change?

Discussion

In Experiment 4, you observed clipping levels that were approximately equal. This was the case for the following reasons:

- a. For a given value of I_{CQ} , the design procedure lets you calculate the component values that result in an operating point near the middle of the AC load line.
- b. If the operating point is near the middle of the AC load line.

$$V^+ = V^- = V_{\text{CEQ}}$$

- c. The voltage divider circuit, used in Experiment 4, provides a value of I_{CQ} that is essentially independent of B . For this reason, the actual value of I_{CQ} was very close to the design value. This ensured that the circuit's actual operating point was near the center of the AC load line.

This experiment used a collector and emitter feedback biasing circuit. The operating point in this circuit isn't nearly as independent of B , as a voltage divider biasing circuit. For this reason, the actual operating point probably differed slightly from the design value. The actual operating point probably was not exactly in the middle of the AC load line.

Given the large gain of the amplifier, a slight increase in v_{IN} quickly produces saturation or cutoff on **one half cycle or the other**. When this occurs, the average, DC, collector voltage changes, which in turn shifts the Q point.

Since a shift in the Q point occurs, the values corresponding to $i_{C(SAT)}$ and $v_{CE(CUT)}$ change. For this reason, a *noticeable shift* in the clipping levels in step 26 depended upon the amplitude of v_{IN} .

Comparing the results of Experiment 5 with those obtained in Experiment 4 illustrates the fact that the shift in actual clipping levels is considerably more pronounced in large gain amplifiers.

EXPERIMENT 6

× 10 COMMON-BASE VOLTAGE AMPLIFIER

Objective: *To design and experimentally verify the operation of a typical × 10 common-base voltage amplifier.*

Introduction

In this experiment, you will design a common-base amplifier comparable to the common-emitter amplifier designed in Experiment 4. In addition, you will experimentally determine the output resistance, R_s , of the Heathkit ET-1000 Design Trainer.

The specifications for the amplifier you are to design are as follows:

- Voltage gain** = 10.
- Load resistance** = $2.2\text{k}\Omega$
- Lowest signal frequency** = 500Hz.
- Supply voltage** = 20V.
- Quiescent collector current** = 3mA.
- Biasing scheme** — voltage divider.

Material Required

- Heathkit Engineering Design Trainer ET-1000
- Oscilloscope
- 1 — NPN type 2N3904 transistor (417-875)
- 1 — 100Ω , 1/4-watt, 5% resistor
- 1 — 120Ω , 1/4-watt, 5% resistor
- 1 — 680Ω , 1/4-watt, 5% resistor
- 1 — $2.2\text{k}\Omega$, 1/4-watt, 5% resistor
- 1 — $3.3\text{k}\Omega$, 1/4-watt, 5% resistor
- 1 — $3.9\text{k}\Omega$, 1/4-watt, 5% resistor
- 2 — $1.5\text{k}\Omega$, 1/4-watt, 5% resistor
- 2 — $10\mu\text{F}$, 50V, electrolytic capacitors
- 1 — $100\mu\text{F}$, 50V, electrolytic capacitor
- 1 — $100\text{k}\Omega$ potentiometer located on Trainer

Procedure

Refer to the voltage divider circuit in the common-base design guide provided in unit 4. Refer to the steps in the Design Guide, and proceed as follows:

1. $I_{CQ} = 3\text{mA}$.

2. $r_{e'} = \frac{37\text{mV}}{I_{CQ}} = \frac{37\text{mV}}{3\text{mA}} = \underline{\hspace{2cm}} \Omega$.

3. $R_{E_1} = 10r_{e'} = \underline{\hspace{2cm}} \Omega$.

4. $r_L = A_V(R_{E_1} + r_{e'}) = \underline{\hspace{2cm}} \text{k}\Omega$.

5. $R_C = \frac{R_L r_L}{R_L - r_L} = \underline{\hspace{2cm}} \text{k}\Omega$.

6. $V_{CBQ} = I_{CQ} R_C = \underline{\hspace{2cm}} \text{V}$.

7. $V_{EQ} = V_{CC} - [I_{CQ} R_C + V_{CBQ} + V_{BE}] = \underline{\hspace{2cm}} \text{V}$.

8. $R_E = \frac{V_{EQ}}{I_{CQ}} = \underline{\hspace{2cm}} \text{k}\Omega$.

9. $R_{E_2} = R_E - R_{E_1} = \underline{\hspace{2cm}} \text{k}\Omega$.

10. Select $R_2 = 1.5\text{k}\Omega$.

11. $R_1 = \frac{R_2(V_{CC} - V_{BQ})}{V_{BQ}} = \underline{\hspace{2cm}} \text{k}\Omega$.

12. Assume $h_{FE} = 100$.

$$R_1 \parallel R_2 = \underline{\hspace{2cm}} \text{k}\Omega$$

$$h_{FE}(R_{E_1} + r_{e'}) = \underline{\hspace{2cm}} \text{k}\Omega$$

$$R_{IN'} = R_1 \parallel R_2 \parallel h_{FE}(R_{E_1} + r_{e'}) = \underline{\hspace{2cm}} \text{k}\Omega$$

$$R_{IN} = R_{E_2} \parallel (R_{E_1} + r_{e'}) = \underline{\hspace{2cm}} \Omega$$

Calculate the minimum capacitor values:

$$C_1 = \frac{3.18}{F_1 R_{IN}} = \text{_____} \mu\text{F.}$$

$$C_2 = \frac{3.18}{F_1 R_L} = \text{_____} \mu\text{F.}$$

$$C_3 = \frac{3.18}{F_1 R_{IN}} = \text{_____} \mu\text{F.}$$

Discussion

Steps 1 through 12 outline the design process. Your calculations should be similar to the following:

$$1. \quad I_{CQ} = 3\text{mA.}$$

$$2. \quad r_{e'} = \frac{37\text{mV}}{I_{CQ}} = \frac{37\text{mV}}{3\text{mA}} = 12.3\Omega.$$

$$3. \quad R_{E_1} = 10r_{e'} = 10(12.3\Omega) = 123\Omega.$$

$$4. \quad r_L = A_V(R_{E_1} + r_{e'}) = 10(123\Omega + 12.3\Omega) = 1.35\text{k}\Omega.$$

$$5. \quad R_C = \frac{R_L r_L}{R_L - r_L} = \frac{2.2\text{k}\Omega(1.35\text{k}\Omega)}{2.2\text{k}\Omega - 1.35\text{k}\Omega} = 3.49\text{k}\Omega.$$

$$6. \quad V_{CBQ} = I_{CQ} r_L = 3\text{mA}(1.35\text{k}\Omega) = 4.05\text{V.}$$

$$7. \quad V_{EQ} = V_{CC} - [I_{CQ} R_C + V_{CBQ} + V_{BE}].$$

$$V_{EQ} = 20\text{V} - [3\text{mA}(3.49\text{k}\Omega) + 4.05\text{V} + 0.7\text{V}].$$

$$V_{EQ} = 20\text{V} - 15.22\text{V.}$$

$$V_{EQ} = 4.78\text{V.}$$

$$8. \quad R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{4.78\text{V}}{3\text{mA}} = 1.59\text{k}\Omega.$$

$$9. \quad R_{E_2} = R_E - R_{E_1} = 1.59\text{k}\Omega - 123\Omega = 1.47\text{k}\Omega.$$

10. $R_2 = 1.5k\Omega$.

11. With $V_{EQ} = 4.78V$, $V_{BQ} = 4.78V + 0.7V = 5.48V$. Thus:

$$R_1 = R_2 \frac{[V_{CC} - V_{BQ}]}{V_{BQ}} = \frac{1.5k\Omega[20V - 5.48V]}{5.48V} = 3.97k\Omega.$$

12. $R_1 \parallel R_2 = 3.97k\Omega \parallel 1.5k\Omega = 1.09k\Omega$.

13. $h_{fe}(R_{E_1} + r_e') = 100(123\Omega + 12.3\Omega) = 13.53k\Omega$.

14. $R_{IN}' = R_1 \parallel R_2 \parallel h_{FE}(R_{E_1} + r_e') = 1.09k\Omega \parallel 13.53k\Omega = 1.01k\Omega$.

15. $R_{IN} = R_{E_2} \parallel (R_{E_1} + r_e') = 1.47k\Omega \parallel (123\Omega + 12.3\Omega) = 123.9\Omega$.

Finally:

$$C_1 = \frac{3.18}{F_1 R_{IN}} = \frac{3.18}{500(123.9\Omega)} = 51.3\mu F.$$

$$C_2 = \frac{3.18}{F_1 R_L} = \frac{3.18}{500(2.2k\Omega)} = 2.9\mu F.$$

$$C_3 = \frac{3.18}{F_1 R_{IN}'} = \frac{3.18}{500(1.01k\Omega)} = 6.3\mu F.$$

Figure E6-1 illustrates the circuit with standard value components.

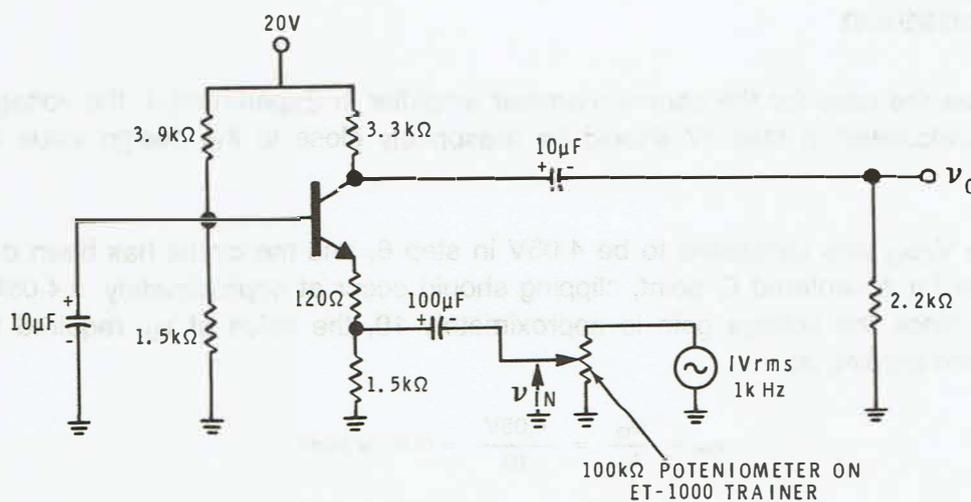


Figure E6-1

× 10 common-base voltage amplifier.

Procedure (Continued)

13. With the power off, construct the circuit shown in Figure E6-1. Make sure you observe the proper polarity when you place the capacitors in the circuit.
14. Turn the power on, and adjust the supply voltage to +20V.
15. Adjust the 100k Ω potentiometer to obtain an input voltage, v_{IN} of 0.1V peak. The frequency of the input signal should be 1kHz.
16. Measure the peak output voltage with the oscilloscope. If you have a dual-trace oscilloscope measure the input and output voltages simultaneously. You should observe input and output voltages that are in phase with each other.

$$v_O = \text{_____} \text{ V peak.}$$

17. Calculate the measured value of the voltage gain:

$$A_V = \frac{v_O(\text{step 16})}{0.1V} = \text{_____}.$$

18. Adjust the 100k Ω potentiometer for maximum input voltage. With v_{IN} maximum, examine the output voltage. Is either peak of the output voltage clipped?

Discussion

As was the case for the common-emitter amplifier in Experiment 4, the voltage gain calculated in step 17 should be reasonably close to the design value of 10.

Since V_{CBQ} was calculated to be 4.05V in step 6, and the circuit has been designed for a centered Q point, clipping should occur at approximately $\pm 4.05V$. Also, since the voltage gain is approximately 10, the value of v_{IN} required to produce clipping is:

$$v_{IN} = \frac{v_O}{A_V} = \frac{4.05V}{10} = 0.405V \text{ peak.}$$

When v_{IN} was adjusted to its maximum value in step 18, no clipping occurred because $v_{IN} < 0.405V$ peak. This was the case because **the small input resistance of the common-base amplifier loaded the signal source.**

This concept is illustrated in Figure E6-2. Note that the unloaded, open-circuit voltage from the ET-1000 Trainer is approximately 1.41V peak. When the common-base amplifier is connected to the signal source, the voltage supplied to the amplifier input terminals, v_{IN} , is:

$$v_{IN} = \frac{1.41V(R_{IN})}{R_S + R_{IN}}$$

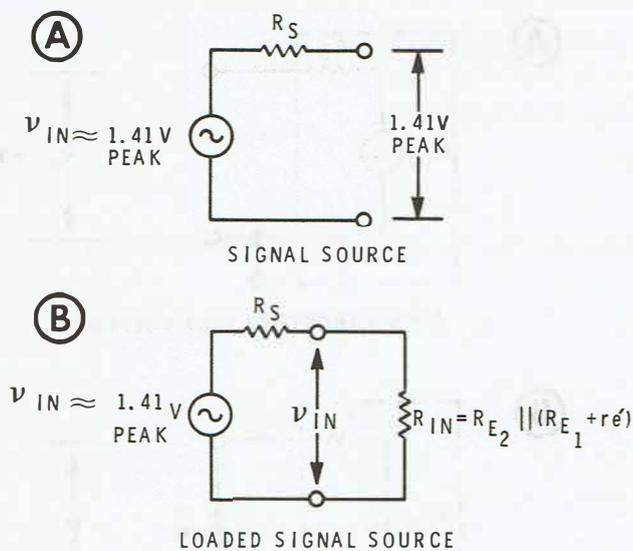


Figure E6-2

Loading effects.

If v_{IN} and R_S are known, R_{IN} can be determined experimentally.

Clearly, if R_{IN} is not large compared to R_S , a significant portion of the 1.41V peak signal will be dropped across R_S . This is precisely what happened in step 18.

Procedure (Continued)

- Disconnect the 100kΩ potentiometer. Measure the open-circuit AC output voltage from the ET-1000 Trainer as shown in Figure E6-3A.

$$v_{OC} = \text{_____ V peak} = v_s.$$

- Connect a 680Ω resistor across the ET-1000 Trainer signal source as shown in Figure E6-3B. Measure the voltage across the 680Ω resistor.

$$v_L = \text{_____ V peak.}$$

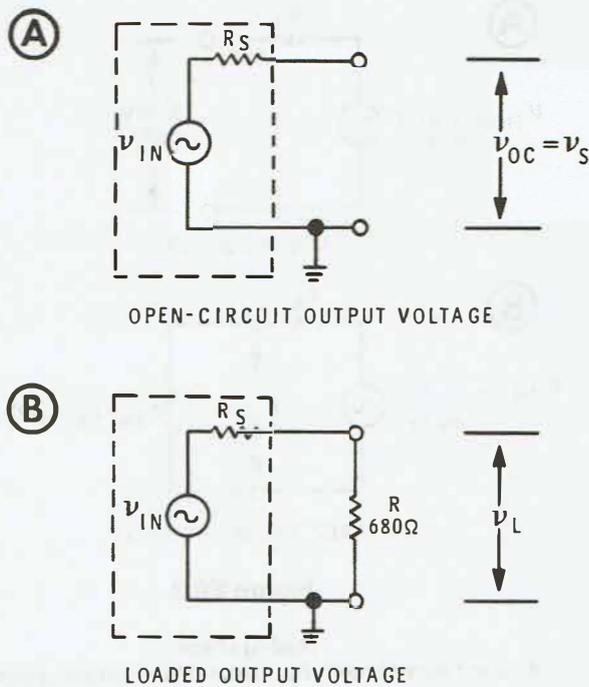


Figure E6-3

Circuits for experimentally determining the value of R_s .

- Calculate the output resistance of the ET-1000 Trainer using the following formula:

$$R_s = \frac{680\Omega(v_s - v_L)}{v_L} = \text{_____ } \Omega.$$

Discussion

Since the ET-1000 Trainer is designed to provide an AC output voltage of approximately 1V rms, the open-circuit voltage measured in step 19 should have been approximately 1.4V peak.

In Figure E6-3 the voltage across the load resistor, R_L is:

$$v_L = \frac{v_S R}{R_S + R}$$

Solving for R_S yields:

$$R_S = \frac{R(v_S - v_L)}{v_L}$$

which is the formula given in step 21.

The value of R calculated in step 21 should equal approximately 600Ω . Most signal sources are designed to provide an output resistance of either 50Ω or 600Ω . The output resistance of the ET-1000 Trainer, therefore, represents a typical value.

Procedure (Continued)

22. Connect the AC output voltage from the ET-1000 Trainer directly to the amplifier input terminals. Record the peak value of v_{IN} .

$$v_{IN} = \text{_____ V peak.}$$

23. Calculate the amplifier's input resistance from the following formula:

$$R_{IN} = \frac{v_{IN}(R_S)}{v_S - v_{IN}} = \text{_____ } \Omega$$

Recall that:

v_{IN} was measured in step 22.

v_S was measured in step 19.

R_S was calculated in step 21.

Discussion

The input resistance of a common-base amplifier equals $R_{E2} \parallel (R_{E1} + r_o')$. In step 12, R_{IN} was calculated to be approximately 123.9Ω . The value of R_{IN} obtained in step 23 should be close to this value.

The equation provided in step 23 to calculate R_{IN} is obtained by applying the voltage division principle to the circuit shown in Figure E6-2B. The input voltage, v_{IN} is:

$$v_{IN} = \frac{v_S(R_{IN})}{R_S + R_{IN}}$$

Solving this equation for R_{IN} yields:

$$R_{IN} = \frac{v_{IN}(R_S)}{v_S - v_{IN}}$$

which is the formula given in step 23.

Procedure (Continued)

24. Reconnect the $100\text{k}\Omega$ potentiometer, and adjust it to obtain an input voltage of 0.2V peak-to-peak. Remove the $2.2\text{k}\Omega$ load resistor, R_L and measure the peak-to-peak output voltage.

$$v_O = \text{_____ V peak-to-peak} = v_{TH}$$

25. Reconnect the $2.2\text{k}\Omega$ load resistor, and measure the peak-to-peak output voltage, v_O .

$$v_O = \text{_____ V peak-to-peak} = v_L$$

26. As you did in Experiment 4, calculate the amplifier's output resistance from:

$$R_O = \frac{(v_{TH} - v_L)}{v_L} \quad R_L = \text{_____ k}\Omega.$$

Discussion

The output resistance of a common-base amplifier approximately equals R_C . The value of R_O obtained in step 26 should be approximately equal to $3.3k\Omega$.

The significant differences, between the common-base amplifier in this experiment, and the common-emitter amplifier of Experiment 4 are:

- a. The input resistance of the common-base amplifier is much smaller than the common-emitter amplifier.
- b. The common-base amplifier does not introduce a 180° phase shift in the signal voltage.

EXPERIMENT 7

THE EMITTER FOLLOWER

Objective: *To design and experimentally verify the operation of an emitter-follower amplifier.*

Introduction

Emitter followers typically have a large input resistance, a small output resistance, and a voltage gain slightly less than 1. These characteristics make the emitter follower especially useful for impedance matching applications.

In this experiment, we wish to drive a 470Ω load from the AC signal source on the ET-1000 Trainer. Since the output resistance, R_S of the ET-1000 Trainer is approximately 600Ω a 470Ω load connected directly to the Trainer would load the signal source.

You are to design an emitter follower so that the 470Ω load **does not** significantly load the signal source.

The specifications for the proposed circuit are as follows:

Supply voltage = 12V.

Voltage gain = 1.

Lowest signal frequency = 100Hz.

Biasing scheme = voltage divider.

Load resistance = 470Ω .

Material Required

Heathkit Engineering Design Trainer ET-1000

Oscilloscope

1 — NPN type 2N3904 transistor (417-875)

1 — 470Ω , 1/4-watt, 5% resistor

1 — $22k\Omega$, 1/4-watt, 5% resistor

1 — $220k\Omega$, 1/4-watt, 5% resistor

1 — $2.2M\Omega$, 1/4-watt, 5% resistor

2 — $2.2k\Omega$, 1/4-watt, 5% resistor

1 — $47\mu\text{F}$, 50V electrolytic capacitor

1 — $100\mu\text{F}$, 50V electrolytic capacitor

Procedure

Refer to the voltage divider circuit in the emitter-follower Design Guide provided in Unit 4. Refer to the steps in the Design Guide, and proceed as follows.

$$1. R_E = 5R_L = \text{_____} \text{ k}\Omega.$$

$$2. r_L = \frac{R_E R_L}{R_E + R_L} = \text{_____} \Omega.$$

$$3. I_{CQ} = \frac{V_{CC}}{R_E + r_L} = \text{_____} \text{ mA}.$$

$$4. V_{EQ} = I_{CQ} R_E = \text{_____} \text{ V}.$$

$$5. V_{CEQ} = V_{CC} - V_{EQ} = \text{_____} \text{ V}.$$

$$6. R_2 = 10R_E = \text{_____} \text{ k}\Omega.$$

$$7. R_1 = \frac{R_2(V_{CC} - V_{BQ})}{V_{BQ}} = \text{_____} \text{ k}\Omega.$$

$$8. R_1 \parallel R_2 = \text{_____} \text{ k}\Omega.$$

$$h_{fe}(r_L + r_e') = \text{_____} \text{ k}\Omega. \text{ Assume } h_{fe} = 100$$

$$R_{IN} = R_1 \parallel R_2 \parallel h_{fe}(r_L + r_e') = \text{_____} \text{ k}\Omega.$$

Calculate the minimum capacitor values:

$$C_1 = \frac{3.18}{F_1 R_{IN}} = \text{_____} \mu\text{F}.$$

$$C_2 = \frac{3.18}{F_1 R_L} = \text{_____} \mu\text{F}.$$

Discussion

Your calculations for steps 1 through 8 should be similar to:

1. $R_E = 5R_L = 5(470\Omega) = 2.35k\Omega.$
2. $r_L = \frac{R_E R_L}{R_E + R_L} = \frac{2.35k\Omega(470\Omega)}{2.35k\Omega + 470\Omega} = 392\Omega.$
3. $I_{CQ} = \frac{V_{CC}}{R_E + r_L} = \frac{12V}{2.35k\Omega + 392\Omega} = 4.38mA.$
4. $V_{EQ} = I_{CQ}R_E = 4.38mA(2.35k\Omega) = 10.3V.$
5. $V_{CEQ} = V_{CC} - V_{EQ} = 12V - 10.3V = 1.7V.$
6. $R_2 = 10R_E = 10(2.35k\Omega) = 23.5k\Omega.$
7. $R_1 = R_2 \frac{(V_{CC} - V_{BQ})}{V_{BQ}}.$

Since $V_{EQ} = 10.3V$, $V_{BQ} = 10.3V + 0.7V$ or $11V$. Thus:

$$R_1 = \frac{23.5k\Omega(12V - 11V)}{11V} = 2.14k\Omega.$$

$$8. \quad R_1 \parallel R_2 = 2.14k\Omega \parallel 23.5k\Omega = 1.96k\Omega.$$

$$r_e' = \frac{37mV}{I_E} = \frac{37mV}{4.38mA} = 8.45\Omega.$$

$$h_{fe}(r_L + r_e') = 100(392\Omega + 8.45\Omega) \approx 40k\Omega.$$

$$R_{IN} = R_1 \parallel R_2 \parallel h_{fe}(r_L + r_e').$$

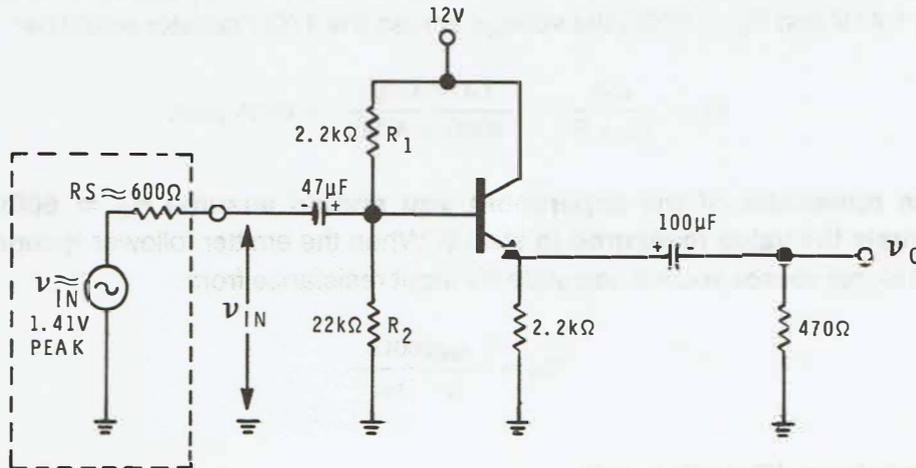
$$R_{IN} = 1.96k\Omega \parallel 40k\Omega = 1.87k\Omega.$$

Thus:

$$C_1 = \frac{3.18}{100(1.87k\Omega)} = 17\mu F.$$

$$C_2 = \frac{3.18}{100(470\Omega)} = 67.7\mu F.$$

Figure E7-1 illustrates the circuit with standard value components.



Procedure (Continued)

9. Turn on the Trainer, and measure the peak output voltage from the signal source, $v_S = \underline{\hspace{2cm}}$ V peak. The frequency of the signal source should be set to 1kHz.
10. Connect a 470Ω resistor across the signal source, and measure the peak output voltage.

$v_O = \underline{\hspace{2cm}}$ V peak.

Discussion

The voltage measured in step 10 was less than the voltage measured in step 9 since the 470Ω resistor loaded the signal source. For example, assuming $v_S = 1.41\text{V}$ and $R_S = 600\Omega$ the voltage across the 470Ω resistor would be:

$$v_R = \frac{v_S R}{R_S + R} = \frac{1.41\text{V}(470\Omega)}{600\Omega + 470\Omega} = 0.62\text{V peak.}$$

In the remainder of the experiment you should assume $R_S = 600\Omega$ and v_S equals the value measured in step 9. When the emitter follower is connected to the signal source you will calculate its input resistance from:

$$R_{IN} = \frac{v_{IN}(600\Omega)}{v_S - v_{IN}}$$

Procedure (Continued)

- Remove the 470Ω resistor. With the power off, construct the circuit shown in Figure E7-1. Make sure the capacitors are placed in the circuit with the proper polarity.
- Turn the power on. Measure the peak input, v_{IN} , and output, v_O , voltages.

$$v_{IN} = \text{_____ V peak.} \quad v_O = \text{_____ V peak.}$$

- Calculate the measured voltage gain, A_V , and input resistance, R_{IN} , as follows:

$$A_V = \frac{v_O}{v_{IN}} = \text{_____}$$

$$R_{IN} = \frac{v_{IN}(600\Omega)}{v_S - v_{IN}} = \text{_____ k}\Omega.$$

- Estimate the output resistance of the emitter follower from:

$$R_O = [r_e' + \frac{R_B \parallel R_S}{h_{fe}}] \parallel R_E = \text{_____ } \Omega.$$

Discussion

In step 8, the input resistance of the emitter follower was calculated to be approximately $1.87\text{k}\Omega$. The emitter follower increases the effective resistance seen by the signal source from 470Ω to $1.87\text{k}\Omega$. The measured value of R_{IN} obtained in step 13 should be approximately $1.87\text{k}\Omega$.

Assuming $v_S = 1.41\text{V}$, $R_S = 600\Omega$, and $R_{IN} = 1.87\text{k}\Omega$. The value of v_{IN} measured in step 12 would be:

$$v_{IN} = \frac{v_S R_{IN}}{R_S + R_{IN}} = \frac{1.41\text{V}(1.87\text{k}\Omega)}{600\Omega + 1.87\text{k}\Omega} = 1.07\text{V}.$$

Naturally, the value of v_{IN} you measured in step 12 will depend upon the actual value of v_S measured in step 9. Also, R_{IN} depends upon the actual value of h_{fe} of your transistor.

The value of v_{IN} measured in step 12 is larger than it would be if the 470Ω load were connected directly across the signal source, as it was in step 10.

Using the values computed in steps 1 through 8, you can estimate the output resistance of the emitter follower as follows:

$$R_S = [r_e' + \frac{R_B \parallel R_S}{h_{fe}}] \parallel R_E.$$

$$R_S = [8.45\Omega + \frac{1.96\text{k}\Omega \parallel 600\Omega}{100}] \parallel 2.35\text{k}\Omega.$$

$$R_S = [8.45\Omega + 4.6\Omega] \parallel 2.35\text{k}\Omega \approx 13\Omega.$$

Compared to a common-emitter or common-base amplifier, this is a very small output resistance.

Since $R_L = 470\Omega$ and $R_O \approx 13\Omega$, the load resistor will not significantly load the amplifier. The voltage gain obtained in step 13 should be very close to 1.

Although the circuit increases the effective load resistance from 470Ω to approximately $1.87\text{k}\Omega$, the amplifier's input resistance was not large enough to prevent loading the signal source.

Since $R_{IN} = R_1 \parallel R_2 \parallel h_{fe}(r_L + r_e')$ the values chosen for R_1 and R_2 must be increased to obtain a larger value of R_{IN} .

Procedure (Continued)

15. Shut the power off. Change the values of R_1 and R_2 as follows:

$$R_1 = 22\text{k}\Omega \text{ and } R_2 = 220\text{k}\Omega.$$

16. Turn the power on. Wait approximately three minutes for the capacitor voltages to stabilize. Measure the peak input, v_{IN} , and output, v_O , voltages.

$$v_{IN} = \text{_____ V peak. } v_O = \text{_____ V peak.}$$

17. Calculate the input resistance from:

$$R_{IN} = \frac{v_{IN}(600\Omega)}{v_S - v_{IN}} = \text{_____ k}\Omega.$$

18. Measure the DC voltage across R_2 . If you have a $\times 10$ probe use it to make this measurement.

$$V_B = \text{_____ V.}$$

19. Turn the power off. Change R_1 to $220\text{k}\Omega$ and R_2 to $2.2\text{M}\Omega$. Turn the power on, and wait approximately three minutes for the capacitor voltages to stabilize.

20. Repeat steps 16 through 18.

$$v_{IN} = \text{_____ V peak.}$$

$$v_O = \text{_____ V peak.}$$

$$R_{IN} = \text{_____ k}\Omega.$$

$$V_B = \text{_____ V.}$$

Discussion

The emitter follower's input resistance is:

$$R_{IN} = R_1 \parallel R_2 \parallel h_{fe}(r_L + r_e')$$

In step 8, $h_{fe}(r_L + r_e')$ was found to be $40k\Omega$. Thus, when $R_1 = 22k\Omega$ and $R_2 = 0.22M\Omega$,

$$R_{IN} = 22k\Omega \parallel 0.22M\Omega \parallel 40k\Omega.$$

$$R_{IN} = 20k\Omega \parallel 40k\Omega \approx 13.3k\Omega.$$

This is a large enough value of R_1 to prevent excessive loading of a 600Ω source. The value of v_{IN} measured in step 16 should be close to the value of v_S measure in step 9. Naturally, the value of R_{IN} that you measured in step 17 will depend upon the actual value of h_{fe} for your transistor.

V_{BQ} was calculated to be 11V in step 7. The value of V_B measured in step 18 should be close to 11V. Also, the measured voltage gain should be approximately 1.

When $R_1 = 0.22M\Omega$ and $R_2 = 2.2M\Omega$:

$$R_{IN} = 0.22M\Omega \parallel 2.2M\Omega \parallel 40k\Omega.$$

$$R_{IN} = .2M\Omega \parallel 40k\Omega \approx 33.3k\Omega.$$

R_1 and R_2 are large enough that the value of R_{IN} is approaching the value of $h_{fe}(r_L + r_e')$. Obviously, we would not expect much loading of the 600Ω signal source.

The value of v_{IN} measured in step 20 should be very close to the value of v_S measured in step 9. For this reason, you may have found it difficult to accurately determine the difference between v_{IN} and v_S . Thus, the value of R_{IN} obtained in step 20 may differ significantly from the calculated value of $33.3k\Omega$.

When you measured V_B in step 20, you probably found V_B was significantly less than 11V. In this case, R_2 was so large that the effective DC resistance between the base of the transistor and ground loaded the voltage divider. This caused I_{CQ} to change, which shifted the Q point away from the center of the AC load line. The values selected for R_1 and R_2 represented a compromise between a large input resistance and a centered Q point.

In most cases, R_2 can be selected to be larger than $10R_E$. The choice of $R_2 = 10R_E$ minimizes potential loading of the voltage divider. In those cases where very large values of R_{IN} are required, a Darlington-pair emitter follower should be considered for the design.

EXPERIMENT 8

CLASS A POWER AMPLIFIERS

Objectives:

To design and experimentally verify the operation of an RC coupled class A power amplifier.

Introduction

In a class A power amplifier, P_{DQ} is equal to twice the maximum possible AC output power. Since only a portion of the AC output power is delivered to the actual load device, R_L , the conversion efficiency of a class A amplifier is quite low.

In this experiment, you will design a class A RC-coupled power amplifier according to the following specifications:

$$V_{CC} = 12V.$$

$$P_{RL} = 150mW.$$

$$F_1 = 2kHz.$$

The load device is a speaker, with an impedance of, approximately, 45Ω .

Material Required

Heathkit Engineering Design Trainer ET-1000

Oscilloscope

1 — NPN type MJE 181 power transistor (417-818)

1 — 741 Op-Amp (8 pin) (442-22)

1 — Speaker (401-163)

1 — 100Ω , 1/2-watt, 5% resistor

1 — 180Ω , 1/2-watt, 5% resistor

1 — 1Ω , 2-watt, 5% resistor

1 — 10Ω , 2-watt, 5% resistor

1 — 15Ω , 2-watt, 5% resistor (Parallel 5- 75Ω , 1/2-watt resistors)

2 — $100\mu F$, 50V, electrolytic capacitors

1 — $470\mu F$, 50V, electrolytic capacitor

1 — $100k\Omega$ potentiometer located on the Trainer.

Construct a 15Ω resistor by paralleling 5- 75Ω 1/2-watt resistors together.

Procedure

Refer to the RC-coupled class A power amplifier Design Guide provided in Unit 5. Referring to the steps in the Design Guide proceed as follows:

1. $V_{CEQ} = \sqrt{2P_{R_L}R_L} = \underline{\hspace{2cm}} \text{ V.}$
2. $P_{DQ} = 8.3P_{R_L} = \underline{\hspace{2cm}} \text{ W.}$
3. $I_{CQ} = \frac{P_{DQ}}{V_{CEQ}} = \underline{\hspace{2cm}} \text{ A.}$
4. $r_L = \frac{V_{CEQ}}{I_{CQ}} = \underline{\hspace{2cm}} \Omega.$
5. $R_C = \frac{R_L r_L}{R_L - r_L} = \underline{\hspace{2cm}} \Omega.$
6. $V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CEQ}] = \underline{\hspace{2cm}} \text{ V.}$
7. $R_E = \frac{V_{EQ}}{I_{CQ}} = \underline{\hspace{2cm}} \Omega.$
8. Select $R_2 = 100\Omega.$
9. $R_1 = R_2 \frac{[V_{CC} - V_{BQ}]}{V_{BQ}} = \underline{\hspace{2cm}} \Omega.$
10. Specify the minimum required BJT ratings:

$$P_{D(\text{MAX})} = \underline{\hspace{2cm}} \text{ W.}$$

$$V_{CE(\text{MAX})} = \underline{\hspace{2cm}} \text{ V.}$$

$$I_{C(\text{MAX})} = \underline{\hspace{2cm}} \text{ A.}$$

Calculate the average power dissipated by resistors:

$$P_{R_1} = \underline{\hspace{2cm}} \text{ W.}$$

$$P_{R_2} = \underline{\hspace{2cm}} \text{ W.}$$

$$P_{R_C} = \underline{\hspace{2cm}} \text{ W.}$$

$$P_{R_E} = \underline{\hspace{2cm}} \text{ W.}$$

Calculate the minimum capacitor values. Refer to the MJE181's data sheet in Appendix B to estimate h_{fe} and r_e' :

$$C_1 = \frac{3.18}{F_1 R_{IN}} = \text{_____} \mu\text{F.}$$

$$C_2 = \frac{3.18}{F_1 R_L} = \text{_____} \mu\text{F.}$$

$$C_3 = \frac{3.18}{F_1 R_E} = \text{_____} \mu\text{F.}$$

Discussion

The calculations for steps 1 through 11 should be similar to the following:

1. $V_{CEQ} = \sqrt{2P_{R_L} R_L} = \sqrt{2(0.15\text{W})(45\Omega)} = 3.67\text{V.}$
2. $P_{DQ} = 8.3P_{R_L} = 8.3(0.15\text{W}) = 1.25\text{W.}$

The choice of the multiplying factor, 8.3, is somewhat arbitrary. Generally a multiplying factor between 8 and 12 will produce satisfactory results.

$$3. \quad I_{CQ} = \frac{P_{DQ}}{V_{CEQ}} = \frac{1.25\text{W}}{3.67\text{V}} = 0.341\text{A.}$$

$$4. \quad r_L = \frac{V_{CEQ}}{I_{CQ}} = \frac{3.67\text{V}}{0.341\text{A}} = 10.76\Omega.$$

$$5. \quad R_C = \frac{R_L r_L}{R_L - r_L} = \frac{45\Omega(10.76\Omega)}{45\Omega - 10.76\Omega} = 14.14\Omega.$$

$$6. \quad V_{EQ} = V_{CC} - [I_{CQ}R_C + V_{CEQ}].$$

$$V_{EQ} = 12\text{V} - [0.341\text{A}(14.14\Omega) + 3.67\text{V}].$$

$$V_{EQ} = 12\text{V} - 8.49\text{V} = 3.51\text{V.}$$

$$7. \quad R_E = \frac{V_{EQ}}{I_{CQ}} = \frac{3.51\text{V}}{0.341\text{A}} = 10.3\Omega.$$

$$8. \quad R_2 = 100\Omega.$$

$$9. \quad R_1 = \frac{R_2[V_{CC} - V_{BQ}]}{V_{BQ}}.$$

Since $V_{EQ} = 3.51\text{V}$, $V_{BQ} = 3.51\text{V} + 0.7\text{V} = 4.21\text{V}$. Thus:

$$R_1 = 100\Omega \frac{[12\text{V} - 4.21\text{V}]}{4.21\text{V}} = 185\Omega.$$

10. $P_{D(\text{MAX})}$ should at least equal the value calculated in step 2:

$$P_{D(\text{MAX})} = 1.25\text{W}.$$

$V_{CE(\text{MAX})}$ should at least equal $2V_{CEQ}$:

$$V_{CE(\text{MAX})} = 2(3.67\text{V}) = 7.34\text{V}.$$

$I_{C(\text{MAX})}$ should at least equal $2I_{CQ}$:

$$I_{C(\text{MAX})} = 2(0.341\text{A}) = 0.682\text{A}.$$

$V_B = 4.21\text{V}$. Thus, the voltage across R_1 is $12\text{V} - 4.21\text{V}$ or 7.79V :

$$P_{R_1} = \frac{(7.79\text{V})^2}{185\Omega} = 0.328\text{W}.$$

Since $V_{R_2} = V_B$:

$$P_{R_2} = \frac{(4.21\text{V})^2}{100\Omega} = 0.177\text{W}.$$

Since $I_{CQ} = 0.341\text{A} \approx I_{EQ}$:

$$P_{R_C} = (0.341\text{A})^2(14.14\Omega) = 1.64\text{W}.$$

$$P_{R_E} = (0.341\text{A})^2(10.3\Omega) = 1.2\text{W}.$$

Consulting a manufacturer's catalog; we select an MJE181 transistor for the design. Appropriate specifications for this transistor are:

$$P_{D(\text{MAX})} = 1.5\text{W at } T_A = 25^\circ\text{C}.$$

$$V_{CE(\text{MAX})} = V_{CEO} = 60\text{V}.$$

$$I_{C(\text{MAX})} = 3\text{A Continuous}.$$

In addition, 1/2W resistors are specified for R_1 and R_2 . Similarly, 2W resistors are specified for R_C and R_E .

11. To calculate C_1 you need to first estimate R_{IN} . Recall that:

$$R_{IN} = R_1 \parallel R_2 \parallel (h_{fe} r_e')$$

$$R_1 \parallel R_2 = 185\Omega \parallel 100\Omega = 64.9\Omega.$$

Since $I_{CQ} = 0.341A$:

$$0.1I_{CQ} = 0.1(0.341A) = 0.0341A.$$

$$1.8I_{CQ} = 1.8(0.341A) = 0.6138A.$$

$$1.9I_{CQ} = 1.9(0.341A) = 0.6479A.$$

Referring to the MJE181's transconductance curve provided in Appendix B, we find:

$$V_{BE} \approx 0.88V \text{ at } I_C = 0.6479A.$$

$$V_{BE} \approx 0.7V \text{ at } I_C = 0.0341A.$$

Thus:

$$r_e' \approx \frac{0.88V - 0.7V}{0.6138A} = 0.293\Omega.$$

Note that the values of V_{BE} on the data sheet corresponds to $V_{CE} = 1V$. Even though V_{CE} is not 1V in this experiment, we will use the data sheet values as reasonable approximations for the actual V_{CE} values.

Referring to the MJE181's h_{fe} versus I_C curve, we estimate the value of h_{fe} at $I_C = 1.9I_{CQ} = 0.6479A$ to be approximately 75. Thus:

$$R_{IN} = 64.9\Omega \parallel 75(0.293\Omega) = 64.9\Omega \parallel 22\Omega = 16.4\Omega.$$

This is a small input resistance, and would therefore load most signal sources.

Finally the minimum capacitor values are:

$$C_1 = \frac{3.18}{F_1 R_{IN}} = \frac{3.18}{2\text{kHz}(16.4\Omega)} = 97\mu\text{F}.$$

$$C_2 = \frac{3.18}{F_1 R_L} = \frac{3.18}{2\text{kHz}(45\Omega)} = 35.3\mu\text{F}.$$

$$C_3 = \frac{3.18}{F_1 R_E} = \frac{3.18}{2\text{kHz}(10.3\Omega)} = 154.4\mu\text{F}.$$

Based on the calculated capacitor values, we select $C_1 = C_2 = 100\mu\text{F}$, and $C_3 = 470\mu\text{F}$.

If the BJT's transconductance curve and h_{fe} versus I_C curve are not available, you can obtain a rough estimate for R_{IN} by assuming that $h_{fe} = 25$, and $r_{e'} = 1\Omega$. For example:

$$R_1 \parallel R_2 = 64.9\Omega.$$

$$R_{IN} = 64.9\Omega \parallel 25\Omega = 18\Omega.$$

This is reasonably close to the 16.4Ω value calculated previously.

Procedure (Continued)

- Due to the low input resistance of the amplifier, excessive loading results if the signal source on the ET-1000 generator is connected directly to the amplifier input terminals. Consequently, a buffer is required between the signal source and amplifier. Specifically, a type 741 integrated circuit, IC, will be used for this purpose.

The pinouts for the IC and transistor that you will use in this experiment are provided in Figure E8-1A and Figure E8-1B respectively. Make sure you familiarize yourself with these figures before you build the experimental circuit.

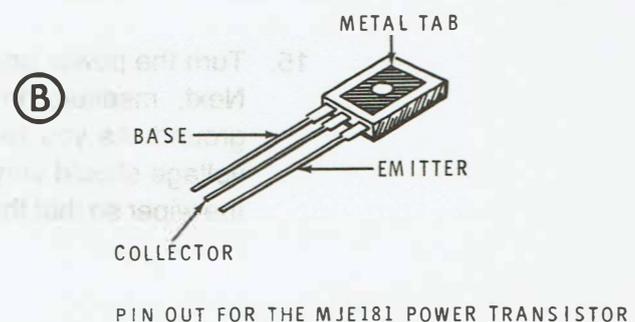
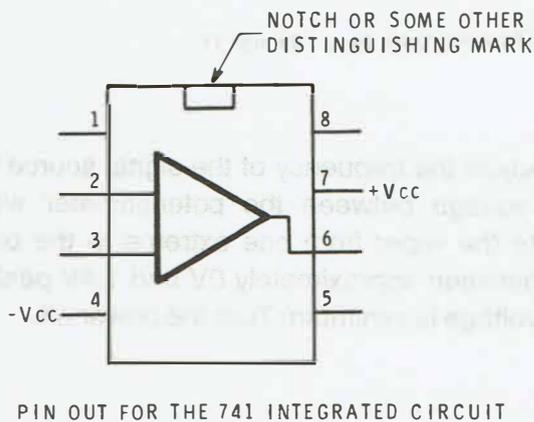


Figure E8-1

Pin connections for the 741 integrated circuit and MJE181 transistor.

- Pin out for the 741 integrated circuit.
- Pin out for the MJE181 power transistor.

13. With the power off, construct the portion of the circuit enclosed by dashed lines in Figure E8-2. Make sure pin 7 is connected to +12V and pin 4 to -12V. If these connections are reversed, the IC can be destroyed when power is applied.
14. Connect the 100kΩ potentiometer on the ET-1000 Trainer to the output of the buffered source, as shown in Figure E8-2.

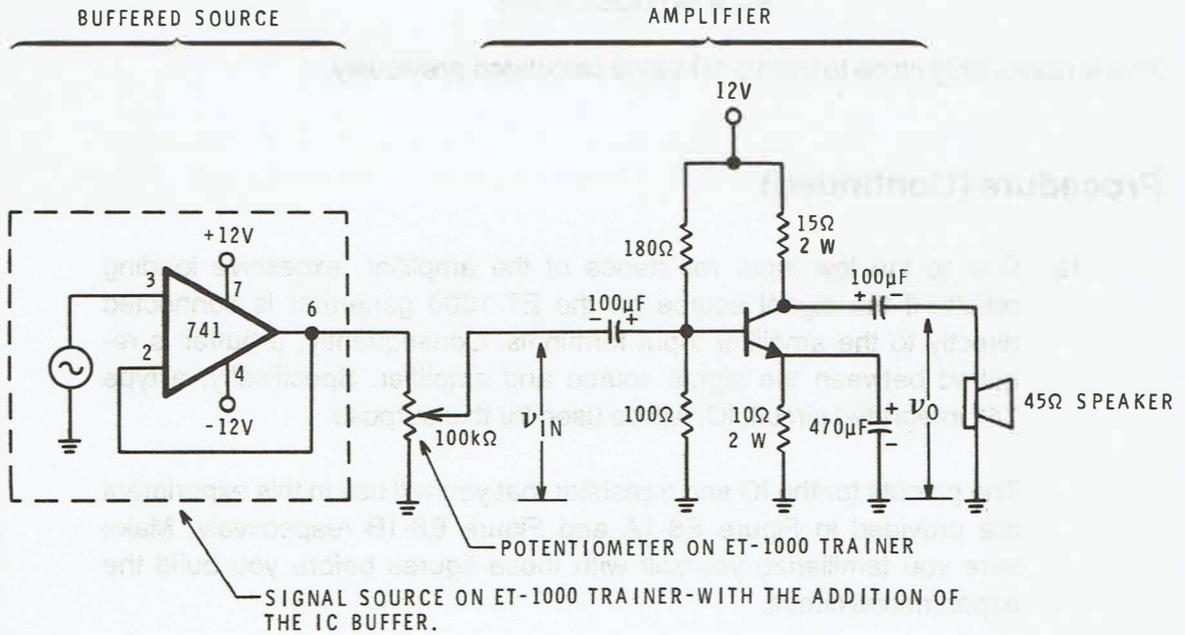


Figure E8-2

Class A power amplifier designed in steps 1 through 11.

15. Turn the power on. Adjust the frequency of the signal source to 2kHz. Next, measure the voltage between the potentiometer wiper and ground. As you rotate the wiper from one extreme to the other, this voltage should vary between approximately 0V and 1.4V peak. Adjust the wiper so that the voltage is minimum. Turn the power off.

16. With the power off, construct the amplifier portion of the circuit shown in Figure E8-2. Once the circuit is constructed, make the following checks:
 - a. The emitter, base, and collector connections should agree with the pinout provided in Figure E8-1B.
 - b. The polarity of the electrolytic capacitors should agree with the polarities shown in Figure E8-2.
 - c. The resistors used for R_C , 15Ω , and R_E , 10Ω , are 2W resistors.
17. Turn the power on. Adjust the potentiometer wiper until the output voltage, v_O , begins to clip. You should hear a very noticeable 2kHz tone from the speaker.
18. Change the frequency of the signal generator from 2kHz to 20kHz. Since 20kHz is at the upper end of the audio spectrum, you probably will not hear the sound from the speaker. Adjust the potentiometer wiper to obtain the maximum **unclipped** output voltage. Record the following values:

Positive peak = _____V.

Negative peak = _____V.

Peak-to-peak value = _____V.

Discussion

Ideally, the output voltage begins to clip at $\pm V_{CEQ}$ or $\pm 3.67V$. Due to the inherent nonlinear characteristics of the transistor, large signal swings produce a distorted output waveform. For this reason, the values of the positive and negative peaks measured in step 18 were probably **not** equal. The peak-to-peak value of the waveform measured in step 18 should have been reasonably close to 2 (3.67V) or 7.34V. Due to component and parameter tolerances, the measured peak-to-peak value may vary as much as 15 percent.

Procedure (Continued)

19. With $F = 20\text{kHz}$, and the potentiometer wiper adjusted to obtain the maximum unclipped output voltage, you will take the data necessary for a three-point analysis as follows:

- Set the volts/division and time/division on your oscilloscope to 2V/division , and $10\mu\text{s/division}$ respectively.
- Measure the voltage from the collector of the transistor to ground. You should obtain a waveform similar to the one illustrated in Figure E8-3.

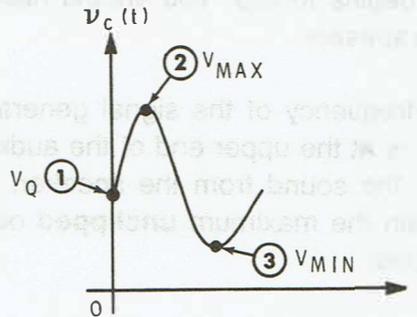


Figure E8-3

Collector voltage for step 19.

- Disconnect the lead going to the potentiometer wiper. The oscilloscope trace should now be a horizontal line that indicates the value of V_{CQ} . Record this value:

$$V_{CQ} = V_Q = \text{_____} \text{V.}$$

This measurement corresponds to point 1 in Figure E8-3.

- Reconnect the lead going to the potentiometer wiper. Record the values of $V_{(MAX)}$, point 2, and $V_{(MIN)}$, point 3.

$$V_{(MAX)} = \text{_____} \text{V.}$$

$$V_{(MIN)} = \text{_____} \text{V.}$$

20. Calculate the peak value of the fundamental and second harmonic components as follows:

$$V_1 = \frac{V_{(MAX)} - V_{(MIN)}}{2} = \text{_____} \text{ V.}$$

$$V_2 = \frac{V_{(MAX)} + V_{(MIN)} - 2V_Q}{4} = \text{_____} \text{ V.}$$

21. Estimate the amount of second harmonic distortion as follows:

$$D_2 = \left| \frac{V_2}{V_1} \right| \times 100 = \text{_____} \text{ \%}.$$

Discussion

The waveform measured in step 19 contains a significant amount of second harmonic distortion. Typically, the value calculated in step 21 is between 7% and 11%. Obviously, the experimental amplifier is not suited for high-fidelity applications.

To reduce the harmonic distortion in the output waveform, the signal swing could be limited to less than $\pm V_{CEQ}$. This approach significantly reduces the already low efficiency of the amplifier. A better approach is to **bypass only a portion of the emitter resistor**, as shown by the partial schematic in Figure E8-4. The addition of R_{E1} tends to mask out the nonlinear variations in r_e' for large-signal swings. Naturally, the addition of R_{E1} also reduces the voltage gain of the amplifier. However, since the amount of power delivered to R_L is our primary concern, this is not a significant disadvantage.

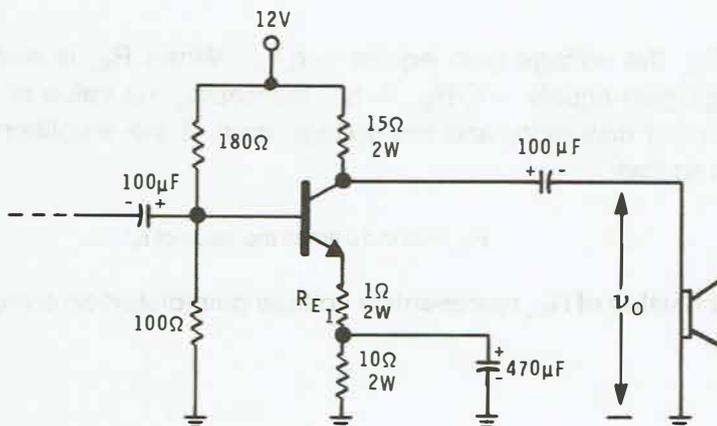


Figure E8-4

Adding R_{E1} reduces the harmonic distortion of the output voltage.

Procedure (Continued)

22. Turn the power off. Connect a 1Ω , 2W resistor in series with the emitter as shown in Figure E8-4.
23. Turn the power on. Adjust the potentiometer wiper to obtain the maximum unclipped output voltage. The output voltage should appear less distorted than before.
24. Measure the voltage from the collector of the transistor to ground. Take the data necessary for a three-point analysis. If necessary, refer to steps 19(a) through 19(d). Record your measured values:

$$V_Q = \text{_____} V.$$

$$V_{(MAX)} = \text{_____} V.$$

$$V_{(MIN)} = \text{_____} V.$$

25. Estimate the amount of second harmonic distortion as follows:

$$V_1 = V_{(MAX)} - V_{(MIN)} = \text{_____} V.$$

$$V_2 = V_{(MAX)} - V_{(MIN)} - 2V_Q = \text{_____} V.$$

$$D_2 = \left| \frac{V_2}{V_1} \right| \times 100 = \text{_____} \%.$$

Discussion

Since R_{E_1} was added to the circuit, the harmonic distortion calculated in step 25 should be less than the value calculated in step 21.

Without R_{E_1} , the voltage gain equals $-r_L/r_e'$. When R_{E_1} is added to the circuit, the voltage gain equals $-r_L/R_{E_1} + r_e'$. Increasing the value of R_{E_1} reduces both the amount of distortion, and the voltage gain of the amplifier. As a guide, R_{E_1} is chosen so that:

$$R_{E_1} = 3 \text{ to } 10 \text{ times the value of } r_e'.$$

Clearly, the value of R_{E_1} represents a voltage gain/distortion compromise.

The conversion efficiency of the amplifier constructed in this experiment is approximately:

$$\eta' = \frac{V_{CEQ}}{2V_{CC}} \times \frac{r_L}{R_L} \times 100.$$

$$\eta' = \frac{3.67V}{2(12V)} \times \frac{10.76\Omega}{45\Omega} \times 100 = 3.66\%.$$

As you can see, only a small portion of the DC input power is converted into useful AC output power. This is typical of a class A amplifier.

EXPERIMENT 9

CLASS AB POWER AMPLIFIERS

Objectives: *To design and experimentally verify the operation of a class AB power amplifier.*

Introduction

The transistors in a class AB push-pull circuit have a maximum collector dissipation of approximately one-fifth the maximum possible AB output power. For a given AC output power, less expensive transistors are required for a class AB design, than for a comparable class A design. In addition, the conversion efficiency of a class AB amplifier is considerably higher than the class A amplifier.

In this experiment, you will design a class AB push-pull, complementary - symmetry, amplifier to supply 0.15W to the speaker used in Experiment 8. Since the load device and AC load power are the same in each experiment, we can directly compare the results.

Material Required

Heathkit Engineering Design Trainer ET-1000
Multimeter
Oscilloscope
1 — NPN type 3904 transistor (471-875)
1 — PNP type 3906 transistor (417-874)
1 — 741 Op Amp (8 pin) (442-22)
2 — 1N4001 diodes (57-65)
1 — Speaker (401-163)
1 — 47Ω , 1/4-watt, 5% resistor
2 — 680Ω , 1/4-watt, 5% resistor
2 — $47\mu\text{F}$, 50V electrolytic capacitors
1 — $470\mu\text{F}$, 50V capacitor

Procedure

Refer to the single-supply, class AB, push-pull power amplifier Design Guide provided in Unit 5. Refer to the steps in the Design Guide, and proceed as follows:

1. $V_{CEQ} = \sqrt{2P_{AC}R_L} = \underline{\hspace{2cm}} \text{V.}$
2. $V_{CC} = 2V_{CEQ} = \underline{\hspace{2cm}} \text{V.}$
3. $i_{C(SAT)} = \frac{V_{CEQ}}{R_L} = \underline{\hspace{2cm}} \text{mA.}$
4. $I = 5\%i_{C(SAT)} = \underline{\hspace{2cm}} \text{mA.}$
5. $R = \frac{V_{CC} - 1.4\text{V}}{2I} = \underline{\hspace{2cm}} \Omega.$
6. Use 1N4001 diodes and a 2N3904/2N3906 complementary transistor pair.
7. Assume $F_1 = 300\text{Hz}$ and $h_{fe} = 50$. Calculate the minimum capacitor values:

$$R_{IN} = \frac{R}{2} \parallel h_{fe}R_L = \underline{\hspace{2cm}} \Omega.$$

$$C_1 = \frac{3.18}{F_1 R_{IN}} = \underline{\hspace{2cm}} \mu\text{F.}$$

$$C_2 = \frac{3.18}{F_1 R_L} = \underline{\hspace{2cm}} \mu\text{F.}$$

Discussion

Your calculations for steps 1 through 7 should be similar to the following:

1. $V_{CEQ} = \sqrt{2P_{AC}R_L} = \sqrt{2(0.15\text{W})(45\Omega)} = 3.67\text{V.}$
2. $V_{CC} = 2V_{CEQ} = 2(3.67\text{V}) = 7.34\text{V.}$
3. $i_{C(SAT)} = \frac{V_{CEQ}}{R_L} = \frac{3.67\text{V}}{45\Omega} = 81.5\text{mA.}$

$$4. \quad I = 5\% i_{C(SAT)} = 5\%(81.5\text{mA}) = 4.075\text{mA}.$$

$$5. \quad R = \frac{V_{CC} - 1.4\text{V}}{2I} = \frac{7.34\text{V} - 1.4\text{V}}{2(4.075\text{mA})} = 728.8\Omega.$$

6. The required transistor ratings are:

$$P_{D(MAX)} \geq \frac{P_{AC}}{5} \geq \frac{0.15\text{W}}{5} \geq 30\text{mW}.$$

$$V_{CE(MAX)} \geq V_{CEQ} \geq 3.67\text{V}.$$

$$I_{C(MAX)} \geq i_{C(SAT)} \geq 81.5\text{mA}.$$

Consulting a manufacturer's catalog, we select a 2N3904/2N3906 complementary transistor pair for the design. Appropriate specifications for these transistors follow:

$$P_{D(MAX)} = 350\text{mW at } T_A = 25^\circ\text{C}.$$

$$V_{CE(MAX)} = V_{CEO} = 40\text{V}.$$

$$I_{C(MAX)} = 200\text{mA}.$$

It is difficult to obtain a "good match" between diode IV curves and BJT transconductance curves, using discrete components. However, silicon type 1N4001 diodes are often adequate for this purpose. Therefore, two 1N4001 diodes were selected for this design.

7. Since $F_1 = 300\text{Hz}$ and h_{fe} is assumed to be 50, a reasonable estimate is:

$$R_{IN} = \frac{R}{2} \parallel h_{fe} R_L.$$

$$R_{IN} = \frac{728.8\Omega}{2} \parallel 50(45\Omega).$$

$$R_{IN} = 364.1\Omega \parallel 2250\Omega = 313.4\Omega.$$

$$C_1 = \frac{3.18}{F_1 R_{IN}} = \frac{3.18}{300\text{Hz}(313.4\Omega)} = 33.8\mu\text{F}.$$

$$C_2 = \frac{3.18}{F_1 R_L} = \frac{3.18}{300\text{Hz}(45\Omega)} = 235.6\mu\text{F}.$$

As discussed in Unit 5, it is sometimes desirable to drive the amplifier with two input coupling capacitors. Consequently, this design will use three capacitors, two for input coupling and one for output coupling. Figure E9-1 illustrates the design using standard value components.

In Figure E9-1, note that an IC buffer is used between the signal source on the ET-1000 Trainer and the power amplifier.

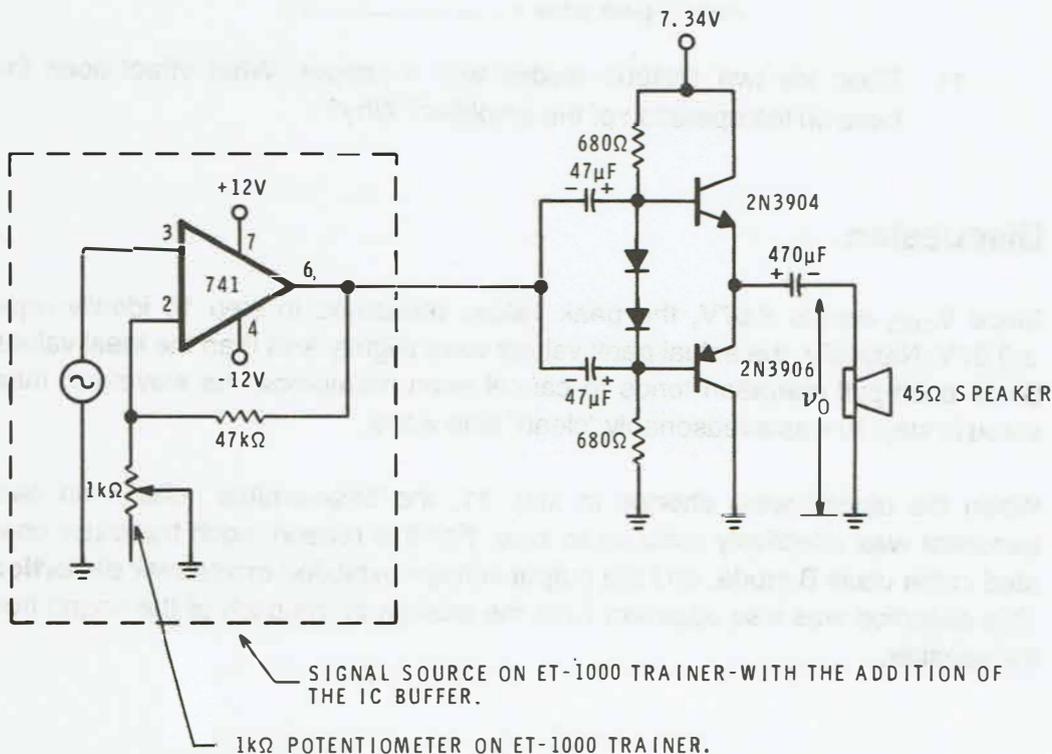


Figure E9-1

Class AB power amplifier designed in steps 1 through 7.

Procedure (Continued)

8. Adjust the 0-20V voltage on the ET-1000 Trainer to 7.34V. Once this voltage is set, turn the Trainer off.
9. With the power off, construct the circuit shown in Figure E9-1. Pay particular attention to the IC power supply connections and the capacitor polarities. Also, make sure each transistor is properly placed in the circuit.

10. Turn the power on. Adjust the frequency of the signal source to 1kHz. Next, adjust the potentiometer wiper to obtain the maximum possible **unclipped** output voltage. You should hear a 1kHz tone from the speaker. Record the following values:

Positive peak = _____ V.

Negative peak = _____ V.

Peak-to-peak value = _____ V.

11. Short the two 1N4001 diodes with a jumper. What effect does this have on the operation of the amplifier? Why?

Discussion

Since V_{CEQ} equals 3.67V, the peak values measured in step 10 ideally equal $\pm 3.67V$. Naturally, the actual peak values were slightly less than the ideal values. Since push-pull operation tends to cancel even harmonics, the waveform measured in step 10 was a reasonably "clean" sine wave.

When the diodes were shorted in step 11, the base-emitter voltage on each transistor was effectively reduced to zero. For this reason, each transistor operated in the class B mode, and the output voltage exhibited **crossover distortion**. This distortion was also apparent from the change in the pitch of the sound from the speaker.

Procedure (Continued)

12. Remove the short across the diodes. Make sure that the output voltage is adjusted for the **maximum unclipped signal**. Record the peak load voltage.

$V_{O(MAX)} =$ _____ V.

13. Use the multimeter, connected as a **DC** ammeter on the 0 - 100mA range, to measure the average, DC, current supplied by V_{CC} . Connect the multimeter in series with V_{CC} for this measurement. Record the measured DC current drain from the power supply.

$I_{DC} =$ _____ mA.

14. Calculate the measured AC load power.

$$P_{AC} = \frac{(V_{O(MAX)} - \text{step 12})^2}{2R_L} = \underline{\hspace{2cm}} \text{ mW.}$$

15. Calculate the measured DC input power.

$$P_{DC} = V_{CC}(I_{DC} - \text{step 13}) = \underline{\hspace{2cm}} \text{ mW.}$$

16. Calculate the amplifier's conversion efficiency.

$$\eta' = \frac{P_{AC} - \text{step 14}}{P_{DC} - \text{step 15}} \times 100 = \underline{\hspace{2cm}} \%$$

Discussion

The maximum unclipped voltage measured in step 12 should be slightly less than 3.67V peak. Let's assume $V_{O(MAX)} = 3.3V$ peak.

The average DC current drawn from the power supply in a class AB amplifier increases when an AC signal is applied to the input of the amplifier. Let's assume the value measured in step 13 was approximately 27mA. Using $V_{O(MAX)} = 3.3V$ peak and $I_{DC} = 27\text{mA}$, we have:

$$P_{AC} = \frac{(3.3V)^2}{2R_L} = \frac{10.89V}{90\Omega} = 121\text{mW.}$$

$$P_{DC} = 7.34V(27\text{mA}) = 198.18\text{mW.}$$

Thus, the conversion efficiency is:

$$\eta' = \frac{121\text{mW}}{198.18\text{mW}} \times 100 = 61\%.$$

Depending upon your measured values, the conversion efficiency calculated in step 16 may be slightly higher or lower than 61%. In any event, the value you obtained should be considerably higher than the 3.66% approximate value calculated for the comparable class A amplifier in Experiment 8.

Procedure (Continued)

In this final portion of the experiment, you will modify the amplifier to illustrate dual-supply operation.

17. Reduce the output from the 0 to +20V power supply to +3.67V. Similarly, adjust the output voltage from the 0 to -20V supply to -3.67V. Once this is done, turn the power off.
18. Modify the circuit as shown in Figure E9-2. Since this is a dual-supply circuit, the 470 μ F output coupling capacitor is no longer required.

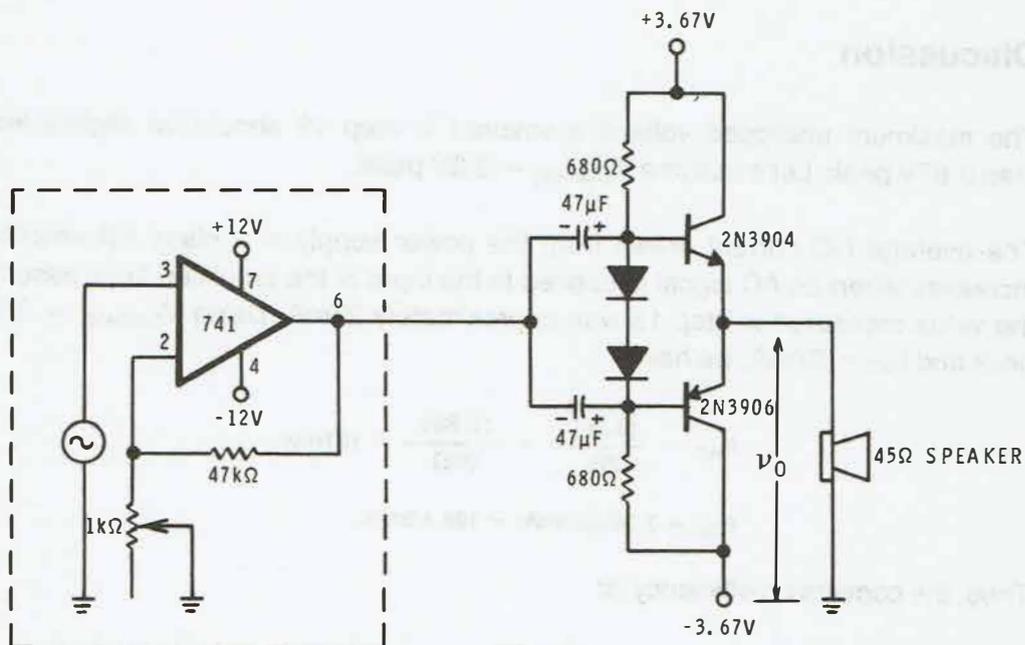


Figure E9-2

Modifying the amplifier for dual-supply operation.

19. Turn the power on. Adjust the potentiometer wiper to obtain the maximum unclipped output voltage. Record the following values:

Positive peak = _____ V.

Negative peak = _____ V.

Peak-to-peak values = _____ V.

Discussion

The values measured in step 19 should be similar to those obtained for the single-supply circuit in step 10. Since very small supply voltages are required for the dual-supply circuit, it is a popular choice for battery operated equipment.

EXPERIMENT 10

THE DIFFERENTIAL AMPLIFIER

Objectives:

To design a differential amplifier that uses a BJT constant-current source.

To modify the design by adding a DC balance control.

To investigate the characteristics of the modified circuit.

Introduction

In this experiment, you will design a differential amplifier according to the following specifications:

- a. $V_{CC} = +10V$, $V_{EE} = -10V$.
- b. $I_S = 2.3mA$.
- c. To obtain a large CMRR, the amplifier will use a BJT constant-current source similar to circuit number 1 in the constant-current source Design Guide.
- d. Three type MPS-A20 transistors will be used for the design. Once the circuit has been designed, we will discuss the concept of a balance control. You will then construct and experimentally verify the operation of the modified circuit.

Material Required

ET-1000 Electronic Design Trainer
Multimeter with leads
Oscilloscope with probe
Hookup wire
Soldering iron
3 — NPN transistors (417-801)
2 — $4.7\text{k}\Omega$, 1/4-watt resistors (yellow-violet-red)
2 — $10\text{k}\Omega$, 1/4-watt resistors (brown-black-orange)
1 — $2.2\text{k}\Omega$, 1/4-watt resistors (red-red-red)
2 — $33\text{k}\Omega$, 1/4-watt resistors (orange-orange-orange)
1 — $1\text{k}\Omega$, 1/4-watt resistors (brown-black-red)
1 — 100Ω , 1/4-watt resistors (brown-black-brown)
1 — 200Ω potentiometer (10-917)
1 — Audio transformer (51-97)
1 — $10\mu\text{F}$, 50V electrolytic capacitor

COMPONENT PREPARATION

- a. Cut eight 2" hookup wires. Remove 1/4" of insulation from each end.
- b. Solder a prepared hookup wire to each of the three terminals on the 200Ω potentiometer.
- c. Solder a prepared hookup wire to each of the five terminals on the audio transformer.

Procedure

Refer to the circuit shown in Figure E10-1, and the Design Guide in Unit 6.

1. I_S has been selected to be 2.3mA.
2. $R_C = \frac{V_{CC}}{I_S} = \underline{\hspace{2cm}} \text{ k}\Omega$.
3. Refer to steps 1-3 in the constant-current source Design Guide, circuit number 1.
 - a. $V_{R_2} = \frac{V_{EE}}{2} = \underline{\hspace{2cm}} \text{ V}$.
 - b. Select $R_1 = R_2 = 33\text{k}\Omega$.
 - c. $R_E = \frac{V_{R_2} - V_{BE}}{I_S} = \underline{\hspace{2cm}} \text{ k}\Omega$.
4. Select $R_B = 10\text{k}\Omega$.

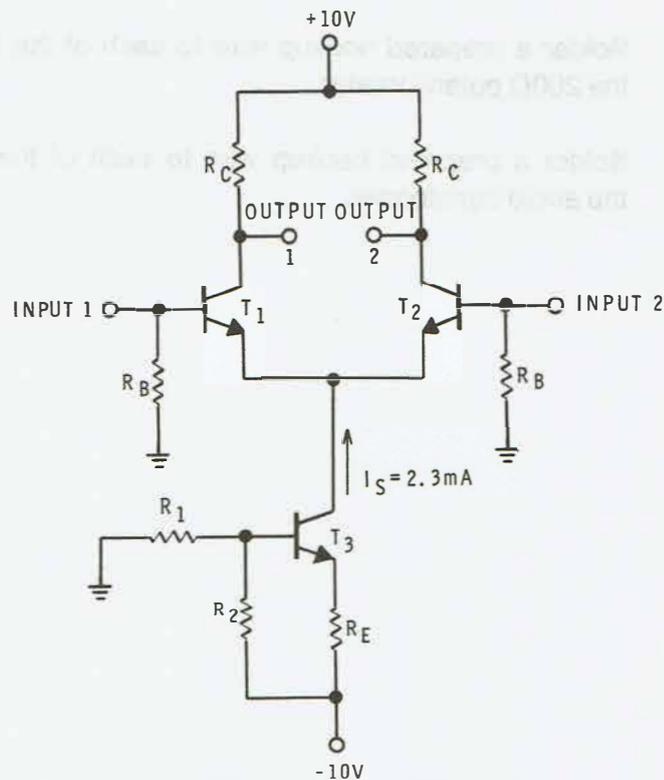


Figure E10-1

Circuit designed in steps 1-4.

Discussion

Your calculations for steps 1 through 4 should be similar to the following:

1. $I_S = 2.3\text{mA}$.

2. $R_C = \frac{V_{CC}}{I_S} = \frac{10\text{V}}{2.3\text{mA}} = 4.35\text{k}\Omega$.

3. $V_{R_2} = \frac{V_{EE}}{2} = \frac{10}{2} = 5\text{V}$.

a. $R_1 = R_2 = 33\text{k}\Omega$.

b. $R_E = \frac{V_{R_2} - V_{BE}}{I_S} = \frac{5\text{V} - 0.7\text{V}}{2.3\text{mA}} = 1.87\text{k}\Omega$.

4. $R_B = 10\text{k}\Omega$.

Using standard resistance values, we select $R_C = 4.7\text{k}\Omega$ and $R_E = 1.8\text{k}\Omega$ for the actual circuit.

As mentioned in the unit, it is very unlikely that the transistors in the differential pair, T_1 and T_2 , will have equal V_{BE} values. Recall, that any mismatch in V_{BE} is amplified as a differential voltage. The emitter currents and DC collector voltages in T_1 and T_2 will probably be unequal.

To compensate for this mismatch, a potentiometer can be added to the emitter circuit as shown in Figure E10-2. Here, the potentiometer is adjusted so that more resistance appears in the emitter circuit of the transistor with the lower value of V_{BE} . Thus, the extra V_{BE} drop in one transistor can be offset by the extra voltage drop across the emitter resistor, R_{E1} or R_{E2} of the other transistor. Without an AC input signal, the potentiometer is adjusted until the collector voltages are equal. This also helps to compensate for differences in collector resistance values caused by component tolerances.

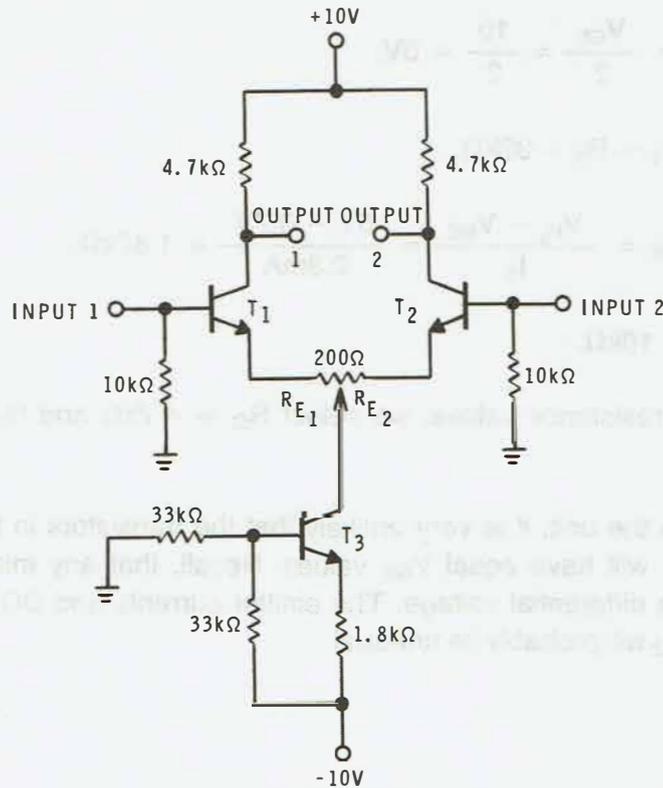


Figure E10-2

Modifying the circuit in Figure E10-1 to include a DC balance control.

The addition of a DC balance control significantly decreases the value of the differential voltage gain. Similarly, the input resistance looking into each input terminal is increased.

Assuming the original amplifier is only slightly unbalanced, $R_{E1} \approx R_{E2} \approx \frac{R_{POT}}{2}$.

In this case, the following approximate formulas are useful:

$$A_d = \frac{R_C}{2(R_{E'_2} + R'_E)}$$

$$R_{IN} = 2h_{ie}(R_{E'_2} + R'_E)$$

Where $R_E = \frac{R_{POT}}{2}$.

The value chosen for the potentiometer is usually not critical. Generally speaking, a 100Ω or 200Ω potentiometer proves satisfactory.

Procedure (Continued)

- Construct the circuit shown in Figure E10-3. Adjust the “+” voltage control for 10 volts between the POS and GND terminals. Adjust the “-” voltage control for 10 volts between the NEG and GND terminals.

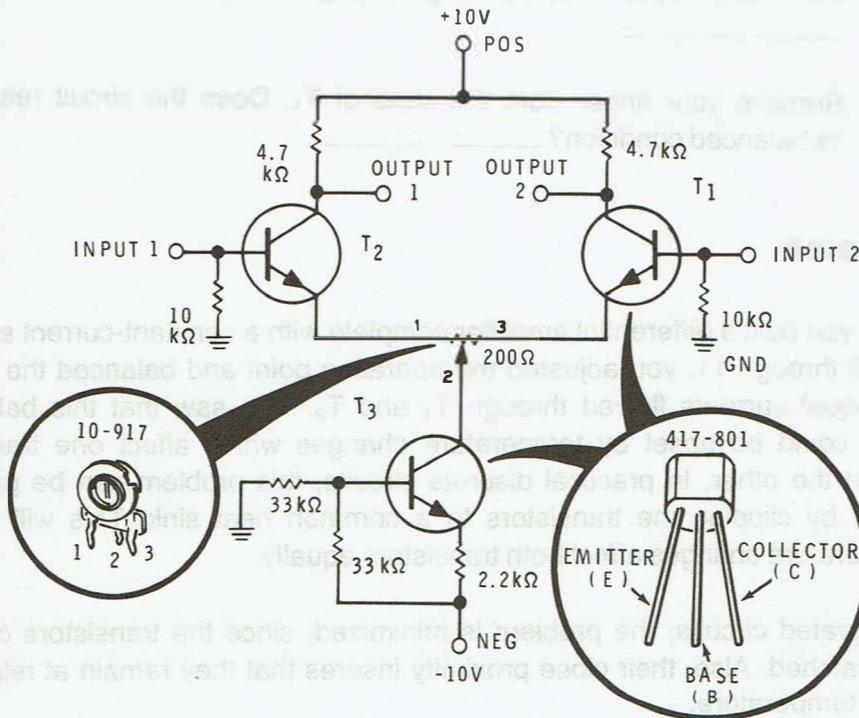


Figure E10-3
Circuit for steps 5 through 11.

6. Connect one lead of the voltmeter to the collector of T_1 (output 1). Connect the other lead to the collector of T_2 (output 2). Adjust the 200Ω potentiometer until the voltmeter reads 0 volts.
7. Set the voltmeter to its lowest DC voltage range. Readjust the potentiometer (if necessary) until the meter reads 0 volts.
8. Connect the voltmeter between the collector of T_1 and ground. Turn the negative voltage control until the voltmeter reads +5V.

READ THE CAUTION NOTE ATTACHED TO THE PARTS LIST BEFORE YOU CONTINUE THE EXPERIMENT.

9. Connect the voltmeter between output 1 and output 2. Readjust the potentiometer (if necessary) so that the voltmeter reads 0 volts. (see Caution note attached to parts list.)
10. With the voltmeter still connected, touch the plastic case of T_1 with your finger. Watch the voltmeter closely as your finger warms the transistor. Does the reading change? _____ Why?

11. Remove your finger from the case of T_1 . Does the circuit return to its balanced condition? _____.

Discussion

In step 5, you built a differential amplifier complete with a constant-current source. In steps 2 through 11, you adjusted the operating point and balanced the circuit so that equal currents flowed through T_1 and T_2 . You saw that this balanced condition could be upset by temperature changes which affect one transistor more than the other. In practical discrete circuits, this problem can be partially overcome by clipping the transistors to a common heat sink. This will insure that temperature changes affect both transistors equally.

With integrated circuits, the problem is minimized, since the transistors can be closely matched. Also, their close proximity insures that they remain at relatively the same temperature.

Procedure (Continued)

12. If necessary, rebalance the circuit as indicated in step 9; then remove your voltmeter from the circuit.
13. Connect the sine wave generator to the circuit via the potentiometer and $10\mu\text{F}$ capacitor as shown in Figure E10-4. Notice that an input signal is applied to the base of T_1 from the generator of the ET-1000. The $1\text{k}\Omega$ potentiometer is used as an amplitude adjust.

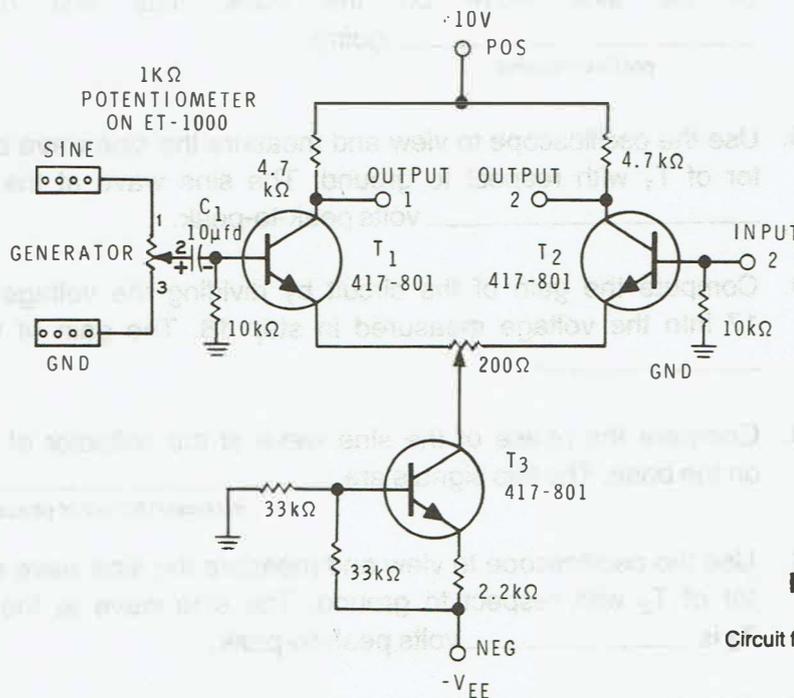


Figure E10-4

Circuit for steps 12 through 28.

14. Set the generator RANGE switch to LOW and the generator FREQUENCY to 1kHz .
15. Connect the external trigger input jack of your oscilloscope to the generator SQUARE terminal on the ET-1000. Place your oscilloscope in the external triggering mode. Set the triggering polarity or slope switch to the "+" position. Connect the lead from the vertical input of your oscilloscope to the SINE terminal of the generator. Connect the ground lead of the oscilloscope to the ground connection in the circuit. Adjust the TIME/CM or horizontal sweep rate on the oscilloscope until a few cycles of the sine wave are visible on the screen.

16. Adjust the horizontal position control on the oscilloscope so that the left side of the trace is visible on the screen. The first half-cycle of the waveform is _____ going. How does the phase of the sine wave produced by the generator compare with that of the square wave which you are using to trigger the oscilloscope?
_____ positive/negative
17. Connect the vertical input of the oscilloscope to the base of T_1 in the circuit. Adjust the $1k\Omega$ potentiometer until the sine wave on the base has a value of 0.2 volts peak to peak. Note the phase of the sine wave on the base. The first half-cycle is _____ going.
_____ positive/negative
18. Use the oscilloscope to view and measure the sine wave at the collector of T_1 with respect to ground. The sine wave at the collector is _____ volts peak-to-peak.
19. Compute the gain of the circuit by dividing the voltage set in step 17 into the voltage measured in step 18. The gain of the stage is _____
20. Compare the phase of the sine wave at the collector of T_1 with that on the base. The two signals are _____
_____ in phase/180° out of phase
21. Use the oscilloscope to view and measure the sine wave at the collector of T_2 with respect to ground. The sine wave at the collector of T_2 is _____ volts peak-to-peak.
22. Compute the gain of the circuit by dividing the voltage set in step 17 into the voltage measured in step 18. The gain of the circuit is _____. Is this approximately the same gain computed in step 19? _____
23. Compare the phase of the sine wave at the collector of T_2 with that on the base of T_1 . The two signals are _____
_____ in phase/180° out of phase
24. Compare the phase of the sine wave at the collector of T_2 with that at the collector of T_1 . These two signals are _____
_____ in phase/180° out of phase

25. Disconnect the external trigger input from the oscilloscope. Place the oscilloscope in the internal triggering mode. Stabilize the display using the triggering level control.
26. Remove any ground connection between the oscilloscope and the circuit under test.
27. Connect the ground lead of the oscilloscope to the collector of T_1 . Connect the vertical input of the oscilloscope to the collector of T_2 . Measure the amplitude of the sine wave between the two collectors. The signal is _____ volts peak-to-peak.
28. Compute the gain of the stage by dividing the input voltage set in step 17 into the output voltage measured in step 23. The gain of the stage is _____. How does this compare with that computed in steps 19 and 22? _____.

Discussion

In this part of the experiment, you examined the operation of the single-input differential amplifier. You applied a 1kHz signal from the generator to the base of T_1 and you triggered the oscilloscope with a square wave from the generator. Because the square wave has the same phase as the sine wave, you can easily monitor the phase of the signal at any point in the circuit. In steps 16 and 17, you saw that the first half-cycle of the waveform appeared to be positive going.

In step 17, you set the voltage on the base of T_1 to 0.2 volts peak-to-peak. Next, you measured the voltage at the collector of T_1 and found it to be about 2.2 volts peak-to-peak. (Your measurement may vary somewhat from this typical value). This corresponds to a circuit gain of:

$$\frac{2.2V}{0.2V} = 11.$$

You also found that the signal at the collector of T_1 is 180° out of phase with the base.

In step 21, you measured the voltage at the collector of T_2 . You should have found a signal about the same amplitude as that on the collector of T_1 . This signal is in phase with the input signal and 180° out of phase with the signal on the collector of T_1 .

Next, you connected the oscilloscope to monitor the output between the two collectors. The differential output appears about twice the amplitude as either of the outputs considered separately. Thus, the gain of the stage appears to double when the differential output is used.

Now let's examine the characteristics of an amplifier with complementary inputs. To operate in this mode, the amplifier requires two input signals which are 180° out of phase. An easy way to get two out-of-phase signals is to use a transformer with a center-tapped secondary.

Procedure (Continued)

- 29. Construct the circuit shown in Figure E10-5.

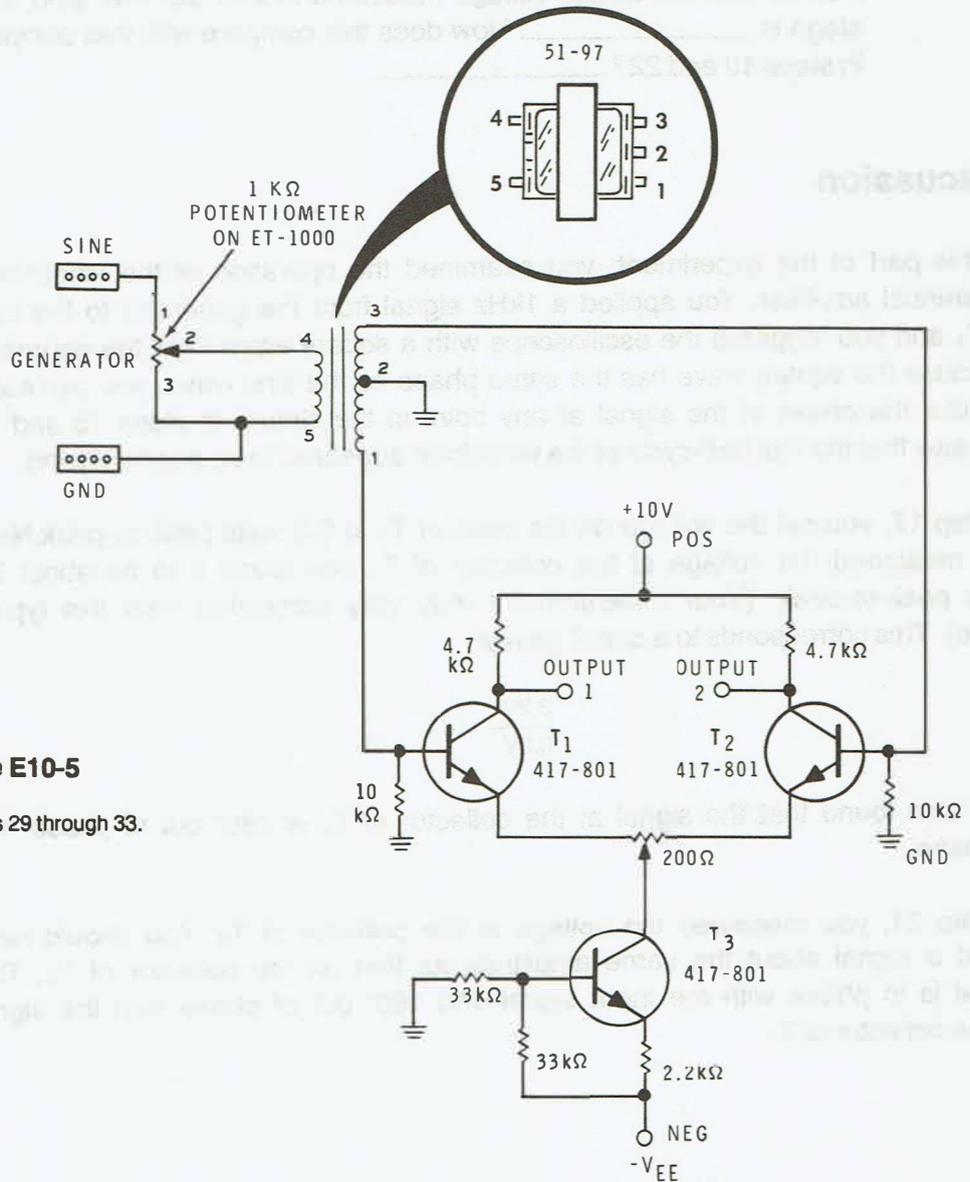


Figure E10-5

Circuit for steps 29 through 33.

(CAUTION THE ADAPTER PLUG ON THE TRAINER IS REQUIRED)

30. Remove any ground connection between the oscilloscope and the circuit. Connect the ground lead of the oscilloscope to the base of T_1 . Connect the vertical input lead to the base of T_2 .
31. Adjust the $1\text{k}\Omega$ potentiometer until the differential input between the bases is 0.2 volts peak-to-peak.
32. Connect the ground lead of the oscilloscope to the collector of T_1 . Connect the vertical input lead to the collector of T_2 . The differential output between the collectors has a value of _____ volts peak-to-peak.
33. Divide the input voltage set in step 31 into the output voltage measured in step 32. What is the gain of this stage? _____.

Discussion

Although the overall differential input voltage is 0.2 volts peak-to-peak, the voltage on each base with respect to ground is only 0.1 volts. The output voltage should be about 5.6 volts peak-to-peak. Thus, the gain of the stage is about 28.

The advantage of the differential input mode is not gain, but rather common-mode rejection. While the circuit will amplify differential inputs, it also rejects signals that are common to both inputs. We can verify this by intentionally introducing a common-mode signal.

Procedure (Continued)

34. Modify the circuit as shown in Figure E10-6. Notice that this introduces a relatively high 60Hz signal at the center of the transformer.

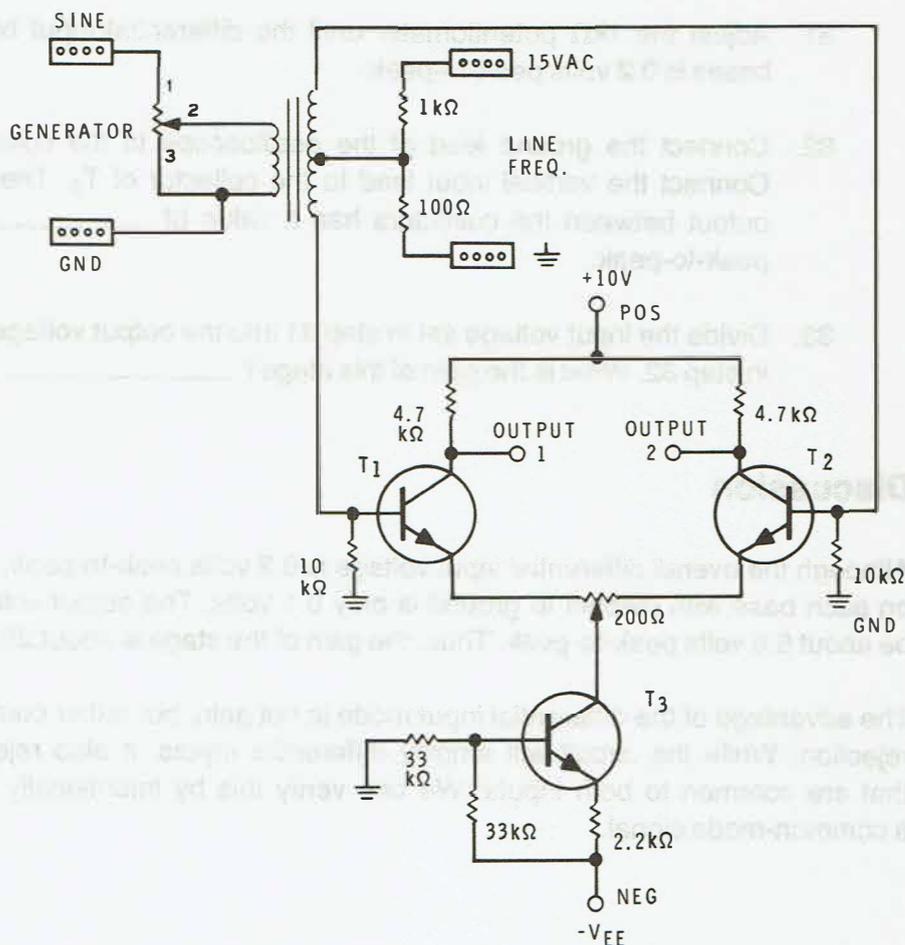


Figure E10-6

Circuit for steps 34 through 37.

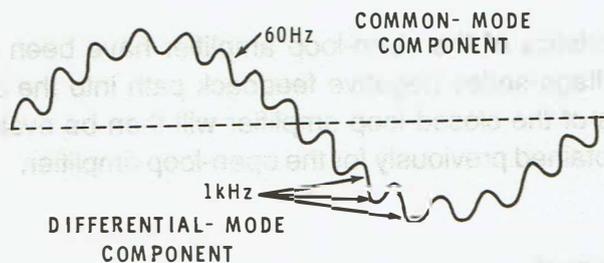
35. Connect the ground lead of the oscilloscope to the ground in the circuit. Connect the vertical input lead to the base of T_1 . On a separate sheet of paper, draw the waveform that you observe on the base. Label the 60Hz common-mode signal. Label the 1kHz differential signal. Which signal is higher in amplitude? _____.
36. View the signal on the base of T_2 . Does it appear the same as the signal on the base of T_1 ? _____.

(AGAIN, THE ADAPTER PLUG ON THE TRAINER IS REQUIRED.)

37. Remove any ground connection between the oscilloscope and the circuit. Connect the ground lead of the oscilloscope to the collector of T_1 . Connect the vertical input lead to the collector of T_2 . What is the amplitude of the 1kHz signal between the collectors? _____ volts peak-to-peak. Is the 60Hz common-mode signal present at the collector circuit? _____.

Discussion

In this part of the experiment, we deliberately applied a 4-volt peak-to-peak common-mode signal to the differential amplifier. Your sketch of the input signal should look somewhat like Figure E10-7. Notice that the signal we wish to amplify is barely visible. Nevertheless, the circuit responds to the tiny 1kHz signal and ignores the much larger common-mode signal. If the circuit is perfectly balanced, the 1kHz signal will be amplified normally. Only a slight trace of the 60Hz signal should be seen in the output circuit.

**Figure E10-7**

Signed at the base of T_1 .

EXPERIMENT 11

TWO STAGE AMPLIFIERS

Objectives:

To experimentally verify the operation of the two-stage amplifier designed in Unit 6.

To introduce a voltage-series, negative feedback path in the amplifier.

To investigate the characteristics of the feedback amplifier.

Introduction

Many applications require two or more stages of amplification in order to provide adequate voltage gain and/or resistance levels. In the first part of the experiment, you will construct a two-stage, RC-coupled voltage amplifier designed to provide a typical voltage gain of 500.

Once the characteristics of the open-loop amplifier have been determined, you will introduce a voltage-series negative feedback path into the amplifier system. The characteristics of the closed-loop amplifier will then be evaluated, and compared with those obtained previously for the open-loop amplifier.

Material Required

Heathkit Engineering Design Trainer ET-1000

Oscilloscope

2 — NPN type 2N3904 transistors (417-875)

1 — 100 Ω , 1/4-watt, 5% resistor

1 — 2.2k Ω , 1/4-watt, 5% resistor

3 — 8.2k Ω , 1/4-watt, 5% resistors

3 — 10k Ω , 1/4-watt, 5% resistors

2 — 27k Ω , 1/4-watt, 5% resistors

2 — 100k Ω , 1/4-watt, 5% resistors

3 — 10 μ F, 50V electrolytic capacitors

2 — 47 μ F, 50V electrolytic capacitors

Procedure

1. With the power off, construct the circuit shown in Figure E11-1. Make sure the electrolytic capacitors are placed in the circuit with the correct polarity.

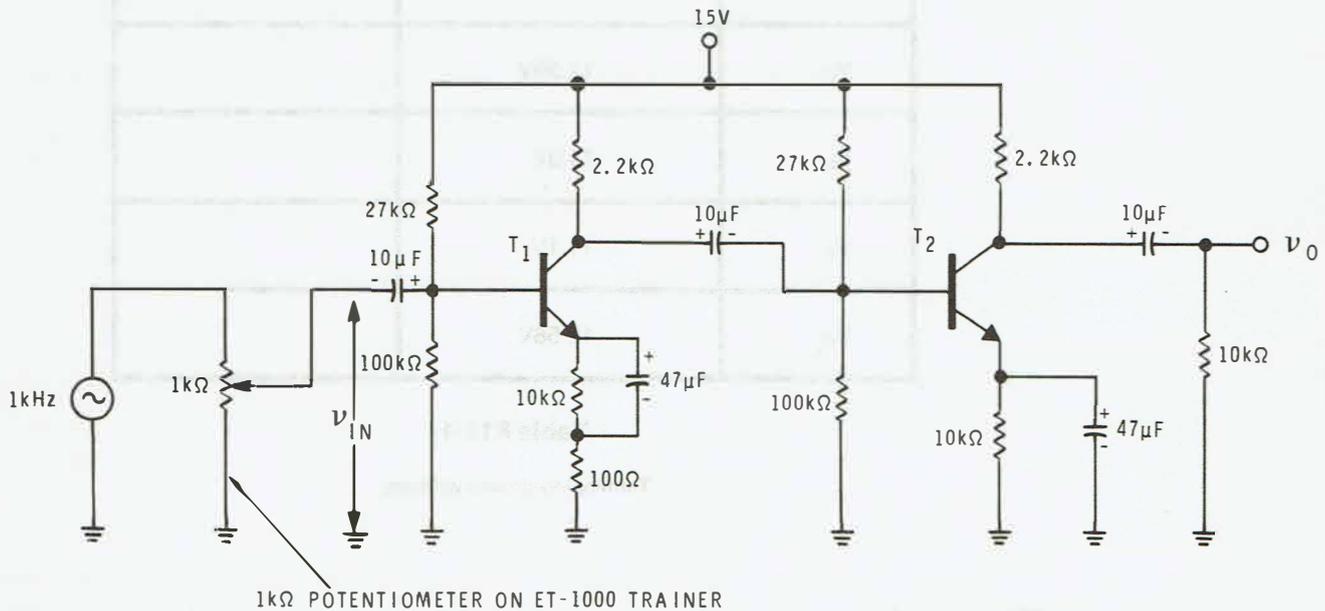


Figure E11-1

Two stage amplifier.

2. Disconnect the lead going to the middle of the potentiometer to ensure that $v_{IN} = 0$. Turn the power on, and adjust the variable positive power supply to obtain 15V.
3. The calculated values in Table E11-1 are based on those obtained in Example 6-15. Measure the actual terminal-to-ground voltages and record the measured values in the appropriate space provided in Table E11-1.

Voltage	Calculated Value	Measured Value
V_{B_1}	11.8V	
V_{E_1}	11.1V	
V_{C_1}	12.58V	
V_{B_2}	11.8V	
V_{E_2}	11.1V	
V_{C_2}	12.56V	

Table E11-1

Terminal-to-ground voltages.

Discussion

The values measured in step 3 should be close to the calculated values. If they are not, you probably have one or more wiring errors. If you note a significant difference between a calculated and measured value, carefully check the wiring to locate and correct the problem.

Procedure (Continued)

- Reconnect the lead going to the middle of the potentiometer. Adjust the potentiometer wiper to obtain a 0.5V peak, 1kHz output voltage.
- Remove the 10k Ω load resistor and note the peak output voltage.

$$v_o = \text{_____V peak.}$$

- Connect a 2.2k Ω resistor between the output of the amplifier and ground. Note the peak output voltage.

$$v_o = \text{_____V peak.}$$

Discussion

The output resistance of a common-emitter amplifier is approximately equal to R_C . The output resistance of the amplifier in Figure E11-1 should be approximately $2.2\text{k}\Omega$.

When $R_L = \infty$, the voltage drop across the output resistance of the amplifier is 0V . Similarly, when $R_L = R_O$ the voltage drop across the output and load resistors will be equal. The voltage measured in step 6, $R_L = 2.2\text{k}\Omega$, should be approximately one-half of the value measured in step 5 when R_L was ∞ .

Procedure (Continued)

7. Replace the $2.2\text{k}\Omega$ resistor with the $10\text{k}\Omega$ load resistor. If necessary, readjust the potentiometer wiper so that:

$$v_O = 0.5\text{V peak.}$$

8. Connect an $8.2\text{k}\Omega$ resistor in series with the potentiometer wiper. Note the peak value of the output voltage.

$$v_O = \text{_____ V peak.}$$

Discussion

In Example 6-15 the amplifier's input resistance was calculated to be $8.68\text{k}\Omega$. This analysis assumed both transistors had an h_{fe} of 100. The actual input resistance of your amplifier will depend upon the actual h_{fe} values of your transistors.

In step 8, part of the AC input voltage is dropped across the series $8.2\text{k}\Omega$ resistor. The remaining portion of the AC input voltage is dropped across the input resistance of the amplifier. For example, if $R_{IN} = 8.2\text{k}\Omega$, the AC input voltage would divide equally between the series resistor and R_{IN} :

$$v_O = 0.25\text{V peak.}$$

The value of v_O measured in step 8 depends upon the actual input resistance of your amplifier. In any event, you should have noted a significant decrease in v_O when the $8.2\text{k}\Omega$ resistor was connected in series with the potentiometer wiper. Typically, v_O will decrease by approximately 50% since R_{IN} is approximately $8.2\text{k}\Omega$.

Procedure (Continued)

- With $v_O = 0.5\text{V}$ peak, examine the AC voltage at the base of T_2 , and the AC input voltage v_{IN} . The series $8.2\text{k}\Omega$ resistor should be removed for these measurements.

Discussion

The amplifier in Figure E11-1 was designed to provide a “typical” second-stage gain of 50, and a first-stage gain of 10, with a total voltage gain of 10 (50) or 500. Assuming the actual stage gains are 10 and 50 respectively, the value of v_{B_2} and v_{IN} required for a 0.5V output voltage are:

$$v_{B_2} = \frac{0.5\text{V}}{50} = 10\text{mV peak.}$$

$$v_{IN} = \frac{10\text{mV}}{10} = 1\text{mV peak.}$$

To accurately measure these voltages, you need an oscilloscope with a vertical sensitivity **better than 10mV/division** . Even if you have such an oscilloscope, it is quite possible that you will have difficulty making accurate measurements due to the presence of noise voltage at the input of the amplifier.

Since the voltage gain of the second stage varies directly with r_{e_2}' , the total voltage gain of your amplifier will possibly differ significantly from 500. In any case, the actual total voltage gain should be greater than 200.

Procedure (Continued)

- Modify the circuit as shown in Figure E11-2. This modification introduces a negative voltage-series feedback path in the circuit.
- Adjust the potentiometer wiper so that $v_O = 0.5\text{V}$ peak.
- Connect a $2.2\text{k}\Omega$ resistor between the output of the amplifier and ground. Note the peak output voltage:

$$v_O = \text{_____ V peak.}$$

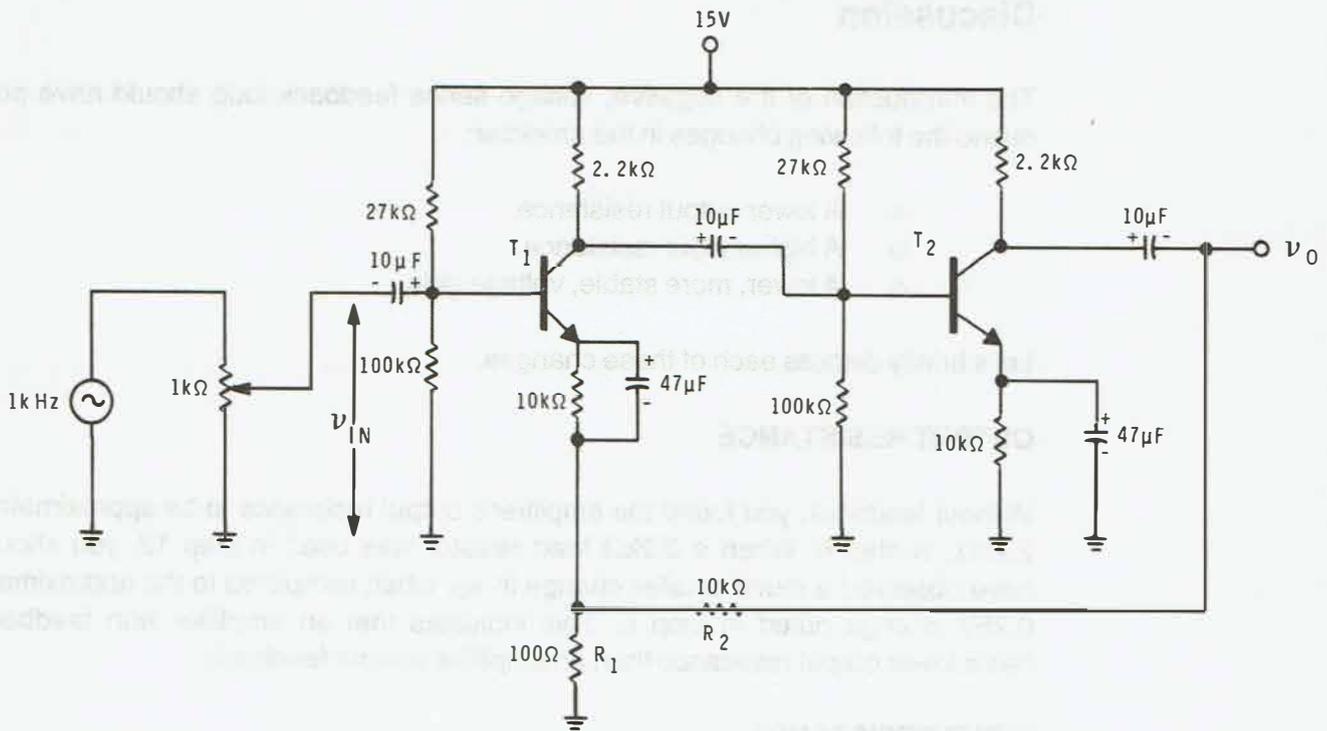


Figure E11-2

Feedback amplifier.

13. Remove the $2.2\text{k}\Omega$ load resistor. Next connect an $8.2\text{k}\Omega$ resistor in series with the potentiometer wiper. Note the peak output voltage:

$$v_O = \text{_____ V peak.}$$

14. Remove the series $8.2\text{k}\Omega$ resistor. With $v_O = 0.5\text{V}$ peak, measure the input voltage:

$$v_{IN} = \text{_____ V peak.}$$

15. Calculate the closed-loop gain of your amplifier:

$$A_{CL} = \frac{0.5\text{V}}{v_{IN(\text{step 14})}} \text{_____}$$

Discussion

The introduction of the negative, voltage-series feedback loop should have produced the following changes in the amplifier:

- A lower output resistance.
- A higher input resistance.
- A lower, more stable, voltage gain.

Let's briefly discuss each of these changes.

OUTPUT RESISTANCE

Without feedback, you found the amplifier's output resistance to be approximately $2.2\text{k}\Omega$, in step 6. When a $2.2\text{k}\Omega$ load resistor was used in step 12, you should have observed a much smaller change in v_O , when compared to the approximate 0.25V change noted in step 6. This indicates that an amplifier with feedback has a lower output resistance than an amplifier without feedback.

INPUT RESISTANCE

Without feedback, the output voltage decreased when an $8.2\text{k}\Omega$ resistor was connected in series with the signal source in step 8. The corresponding decrease in the output voltage of the feedback amplifier in step 13 should have been smaller than the change in step 8. This indicates that the feedback amplifier has a larger input resistance than the original amplifier.

VOLTAGE GAIN

In Figure E11-2, the voltage gain of the feedback network is:

$$B' = \frac{R_1}{R_1 + R_2} = \frac{100\Omega}{100\Omega + 10\text{k}\Omega} = 0.0099.$$

Thus, the closed loop voltage gain is:

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}B'} = \frac{A_{OL}}{1 + A_{OL}(0.0099)}.$$

The value of the closed-loop voltage gain obtained in step 15, depends upon the actual value of your amplifier's open-loop gain.

Table E11-2 summarizes the closed-loop voltage gains you can expect for open-loop voltage gains between 200 and 800.

A_{OL}	$A_{OL}B'$	$(1 + A_{OL}B')$	A_{CL}
200	1.98	2.98	67.1
300	2.97	3.97	75.6
400	3.96	4.96	80.6
500	4.95	5.95	84.0
600	5.94	6.94	86.45
700	6.92	7.92	88.27
800	7.92	8.92	89.7

Table E11-2

Open-loop and closed-loop gains for $B' = 0.0099$.

It is likely that the value of A_{CL} obtained in step 15 falls within the range provided in Table E11-2.

EXPERIMENT 12

JFET

Objectives:

To design and experimentally verify the operation of a self-bias, common-source voltage amplifier.

To construct and verify the operation of an analog multiplexer.

Introduction

In this experiment, you will examine a typical JFET data sheet to determine minimum and maximum parameter values. You will then design a self-bias, common-source amplifier based on average parameter values. You will then construct the amplifier and take appropriate data, so you can compare calculated and actual responses.

In the second portion of the experiment, the concept of an analog multiplexer will be introduced. As you will see, this versatile circuit is easily implemented with FETs.

Material Required

Heathkit Engineering Design Trainer ET-1000

Oscilloscope

2 — N-channel 2N5458 JFETs (417-291)

1 — 220 Ω , 1/4-watt, 5% resistor

1 — 2.2k Ω , 1/4-watt, 5% resistor

1 — 10k Ω , 1/4-watt, 5% resistor

2 — 1k Ω , 1/4-watt, 5% resistors

1 — 1M Ω , 1/4-watt, 5% resistors

2 — 1 μ F, 50V electrolytic capacitors

1 — 47 μ F, 50V electrolytic capacitor

Procedure

1. Refer to the 2N5458 data sheet in Appendix B, and record the following values:

$$I_{DSS(MIN)} = \text{_____ mA.}$$

$$I_{DSS(MAX)} = \text{_____ mA.}$$

$$V_{GS(OFF-MIN)} = \text{_____ V.}$$

$$V_{GS(OFF-MAX)} = \text{_____ V.}$$

$$g_{mo(MIN)} = \text{_____ mS.}$$

$$g_{mo(MAX)} = \text{_____ mS.}$$

$$g_{os(MIN)} = \text{_____ mS.}$$

$$g_{os(MAX)} = \text{_____ mS.}$$

2. Based on the data listed in step 1, calculate the average value of:

$$I_{DSS} = \text{_____ mA.}$$

$$V_{GS(OFF)} = \text{_____ V.}$$

$$g_{mo} = \text{_____ mS.}$$

Figure E12-1 shows a self-bias common-source amplifier. The specifications for this amplifier are as follows:

$$R_{IN} \geq 825 \text{ k}\Omega.$$

$$A_v = -5 \text{ (typical).}$$

$$F_1 = 500 \text{ Hz.}$$

$$V_{DD} = 15 \text{ V.}$$

$$I_{DQ} \approx 0.6 I_{DSS}.$$

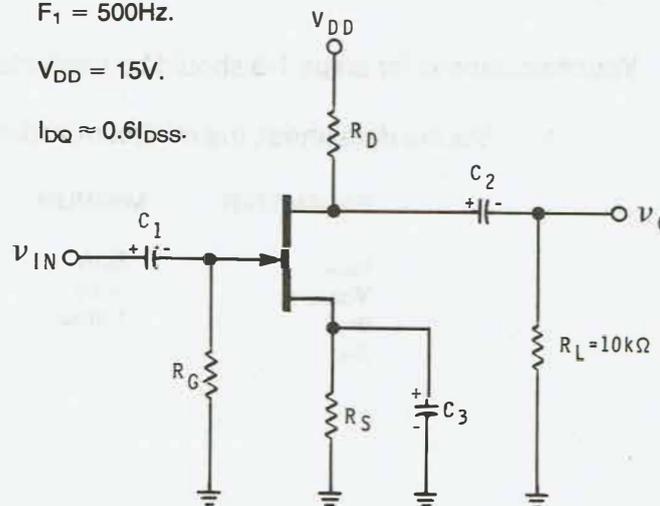


Figure E12-1

× 5 common-source amplifier.

3. Select a suitable value for R_G .

$$R_G = \underline{\hspace{2cm}}$$

4. Calculate the value of g_m for the given bias conditions.

$$g_m = \underline{\hspace{2cm}} \text{ mS.}$$

5. Calculate the value of R_S .

$$R_S = \underline{\hspace{2cm}}$$

6. Calculate the value of R_D .

$$R_D = \underline{\hspace{2cm}}$$

7. Calculate the minimum acceptable values for the coupling and bypass capacitors:

$$C_1 = \underline{\hspace{2cm}}$$

$$C_2 = \underline{\hspace{2cm}}$$

$$C_3 = \underline{\hspace{2cm}}$$

8. Based on the values calculated previously, estimate the V_{GSQ} and V_{DQ} .

$$V_{GSQ} = \underline{\hspace{2cm}} \text{ V.}$$

$$V_D = \underline{\hspace{2cm}} \text{ V.}$$

Discussion

Your calculations for steps 1-8 should be similar to the following:

1. Via the data sheet, the minimum and maximum parameter values are:

PARAMETER	MINIMUM	MAXIMUM
I_{DSS}	2mA	9mA
$V_{GS(OFF)}$	-1V	-7V
g_{m0}	1.5mS	5.5mS
g_{os}	$\underline{\hspace{1cm}}$	0.05mS

In the data sheet note:

- g_{m0} is listed as $|Y_{fs}|$.
- g_{os} is listed as $|Y_{os}|$.
- Both Y_{fs} and Y_{os} are given in units of μ mhos..
- The data sheet does not provide a minimum value for Y_{os} .

Since units of siemens, S, are preferred for conductance values, we elect to express g_{m0} and g_{os} in these units, rather than mhos.

The data sheet does not list a minimum value for Y_{os} since the maximum value is the worst case value. Recall that $r_d = 1/g_{os}$. Thus, the smallest value of r_d you would expect for a 2N5458 JFET is:

$$r_d = \frac{1}{g_{os}} = \frac{1}{Y_{os}} = \frac{1}{0.05\text{mS}} = 20\text{k}\Omega.$$

2. The average parameter values are:

$$I_{DSS} = \frac{2\text{mA} + 9\text{mA}}{2} = 5.5\text{mA}.$$

$$V_{GS(OFF)} = \frac{-1\text{V} + (-7\text{V})}{2} = -4\text{V}.$$

$$g_{m0} = \frac{1.5\text{mS} + 5.5\text{mS}}{2} = 3.5\text{mS}.$$

Note the "typical" data sheet values are approximately equal to the average values.

3. Since $R_{IN} = R_G$, a standard value $1\text{M}\Omega$ resistor satisfies the requirement:

$$R_{IN} \geq 825\text{k}\Omega.$$

4. When $I_D = 0.6I_{DSS}$ and $g_m \approx 0.774g_{m0}$:

$$g_m = 0.774(3.5\text{mS}) = 2.71\text{mS}.$$

5. In a self-bias circuit, the approximate value of R_S required to make $I_D \approx 0.6I_{DSS}$ is:

$$R_S \approx \frac{0.75}{g_{m0}} = \frac{0.75}{3.5\text{mS}} = 214.3\Omega.$$

6. First calculate the required value of r_L . Using the value of g_m calculated in step 4:

$$r_L = \frac{A_v}{g_m} = \frac{5}{2.71\text{mS}} = 1.84\text{k}\Omega.$$

Since the worst case value of r_d is $20\text{k}\Omega$, and $20\text{k}\Omega$ is large when compared to the calculated $1.84\text{k}\Omega$, you can neglect r_d . The required value of R_D is:

$$R_D = \frac{R_L r_L}{R_L - r_L} = \frac{10\text{k}\Omega(1.84\text{k}\Omega)}{10\text{k}\Omega - 1.84\text{k}\Omega} = 2.25\text{k}\Omega.$$

7. The minimum capacitor values are:

$$C_1 = \frac{3.18}{F_1 R_{IN}} = \frac{3.18}{500(1\text{M}\Omega)} = 0.0064\mu\text{F}.$$

$$C_2 = \frac{3.18}{F_1 R_L} = \frac{3.18}{500(10\text{k}\Omega)} = 0.636\mu\text{F}.$$

$$C_3 = \frac{3.18}{F_1 R_S} = \frac{3.18}{500(214.3\Omega)} = 29.7\mu\text{F}.$$

8. When $I_D = 0.6I_{DSS}$ and $V_{GSQ} \approx 0.225V_{GS(OFF)}$:

$$V_{GSQ} = 0.225(-4\text{V}) \approx -0.9\text{V}.$$

$$I_D = 0.6I_{DSS} = 0.6(5.5\text{mA}) = 3.3\text{mA}.$$

$$V_D = V_{DD} - I_D R_D = 15\text{V} - 3.3\text{mA}(2.25\text{k}\Omega) = 7.6\text{V}.$$

$$V_{DQ} = 7.6\text{V}.$$

Procedure (Continued)

- With the power off, construct the circuit shown in Figure E12-2. Be careful to observe the correct polarity for the electrolytic capacitors. Also, note the lead connections for the JFET.

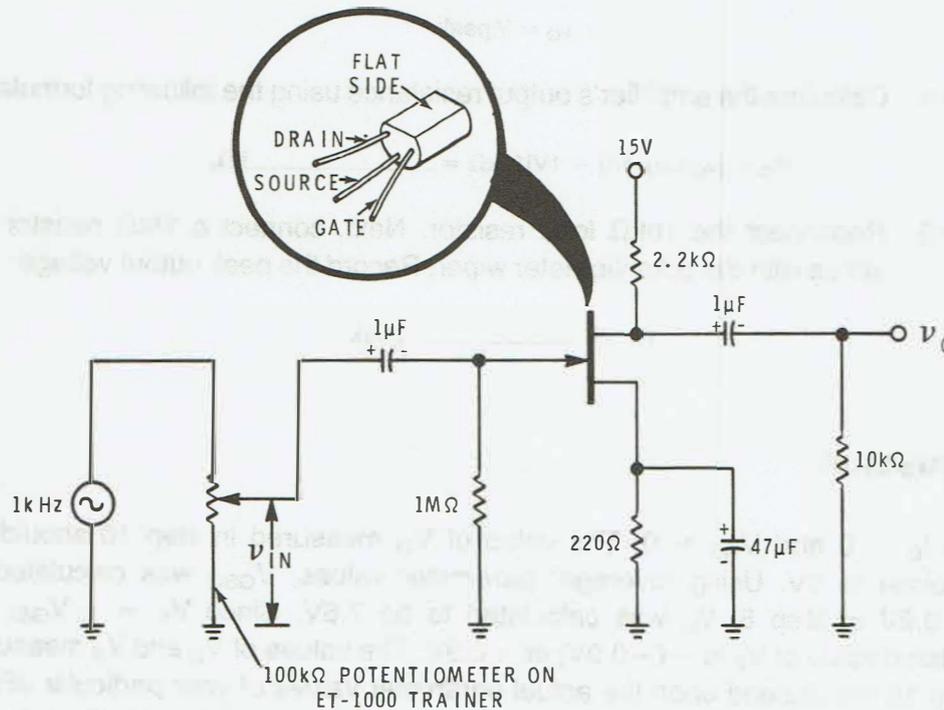


Figure E12-2

Circuit designed in steps 1 through 8.

- Turn the power on, and adjust the supply voltage to 15V. With $v_{IN} = 0V$, measure the terminal-to-ground voltages:

$$V_G = \text{_____} V.$$

$$V_D = \text{_____} V.$$

$$V_S = \text{_____} V.$$

- Adjust the 100kΩ potentiometer to obtain a 1V peak output. Record the value of v_{IN} that produces the 1V peak output.

$$v_{IN} = \text{_____} V \text{ peak.}$$

12. Calculate the measured voltage gain;

$$|A_V| = \frac{1V}{v_{IN}(\text{step 11})} = \underline{\hspace{2cm}}$$

13. Remove the $10k\Omega$ load resistor, and note the peak output voltage:

$$v_O = \underline{\hspace{2cm}} \text{ V peak.}$$

14. Calculate the amplifier's output resistance using the following formula:

$$R_O = [v_O(\text{step 13}) - 1V]10k\Omega = \underline{\hspace{2cm}} k\Omega.$$

15. Reconnect the $10k\Omega$ load resistor. Next, connect a $1M\Omega$ resistor in series with the potentiometer wiper. Record the peak output voltage:

$$v_O = \underline{\hspace{2cm}} \text{ peak.}$$

Discussion

Since $I_G \approx 0$ and $V_{RG} \approx 0$. The value of V_G measured in step 10 should be very close to $0V$. Using "average" parameter values, V_{GSQ} was calculated to be $-0.9V$ in step 8. V_D was calculated to be $7.6V$. Since $V_S = -V_{GS}$, the calculated value of V_S is $-(-0.9V)$ or $+0.9V$. The values of V_D and V_S measured in step 10 will depend upon the actual parameter values of your particular JFET. However, in most cases, the calculated and measured terminal-to-ground voltages will not differ by more than 25%.

The voltage gain measured in step 12 depends upon the actual value of g_m for your particular JFET. Assuming an "average" JFET, the voltage gain will be approximately 5.

The method used in step 14 to measure the amplifier's output resistance is similar to the method used for BJT circuits. Since $R_O \approx R_D$, the value of R_O calculated in step 14 should be approximately $2.2k\Omega$.

Since $R_{IN} = R_G$, the voltage gain is halved when a resistor equal to R_{IN} is connected in series with the amplifier. Consequently, the value of v_O measured in step 15 should be approximately $0.5V$ peak.

ANALOG MULTIPLEXER

In addition to serving as an amplifying device, a JFET can also function as an electronic switch. A block diagram of an **analog multiplexer** is provided in Figure E12-3. Note that:

- Numerous inputs are applied to the multiplexer - v_1, v_2, \dots, v_n .
- The multiplexer provides a single output, v_o .
- Numerous select lines, S_1, S_2, \dots, S_n are provided.

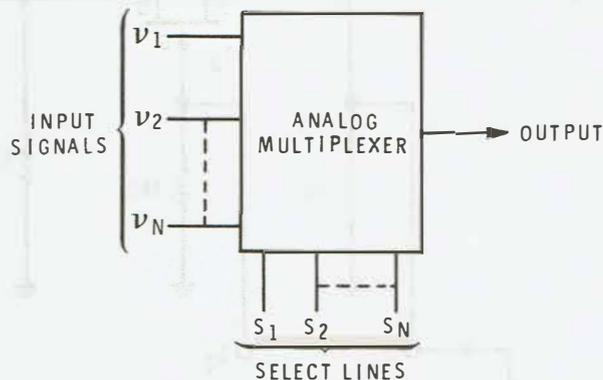


Figure E12-3

Block diagram of an n-channel analog multiplexer.

The function of the multiplexer is simply to connect one of the input lines to the output line.

By applying an appropriate signal to S_1 , the output line is connected to the first input line. In this case, $v_o = v_1$. Similarly, by applying the appropriate signal to S_2 , $v_o = v_2$, and so forth.

In this way, the user can select which input signal is transmitted through the multiplexer to the output line. The various input lines are normally referred to as channels.

A simplified version of a two-channel JFET analog multiplexer is shown in Figure E12-4. Note that the gate voltage, -8V , applied to T_1 , is more negative than $V_{GS(\text{OFF})}$. For this reason, T_1 is cutoff and therefore functions as an open switch. The signal applied to channel one is **not** transmitted to the output. The gate voltage applied to T_2 is essentially 0V , and since the gate is connected to ground via the $1\text{k}\Omega$ resistor, T_2 conducts - approximating a closed switch. In this case, the signal applied to channel 2 is transmitted to the output.

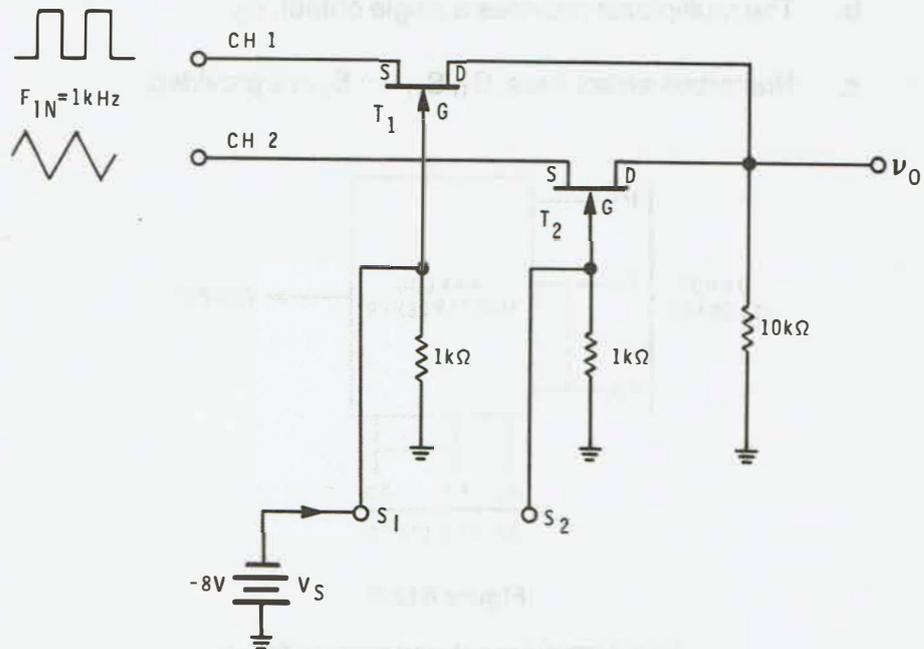


Figure E12-4

A two-channel analog multiplexer.

If -8V were applied to the gate of T_2 , rather than T_1 , T_2 would act like an open switch, and T_1 would act like a closed switch. In this case, the signal applied to channel 1 would be transmitted to the output.

Naturally, if -8V were applied to both gates, v_O would, ideally, equal 0V since both JFETs would act as open switches. Similarly, if each gate voltage was zero volts, both JFETs would conduct. In this case, v_O would be a complex wave that would represent the sum of the signals.

For proper circuit operation, the component values in Figure E12-4 are chosen so that:

- a. $|V_S| > |V_{GS(OFF)MAX}|$.
- b. $R_D \gg r_{d(ON)}$ (for this particular JFET).
- c. $R_G \leq 1k\Omega$.

Procedure (Continued)

16. Dismantle the circuit used in the first part of the experiment. Adjust the variable **negative** supply voltage to $-8V$. Then turn the power off.
17. Construct the circuit shown in Figure E12-4. The pulse and triangular input signals for channel 1 and channel 2 are available on the ET-1000 Trainer.
18. Turn the power on. Verify the operation of the multiplexer by noting the output voltage for the following conditions:

$$V_{G_1} = -8V, V_{G_2} = 0V.$$

$$V_{G_1} = V_{G_2} = 0V.$$

$$V_{G_1} = 0V, V_{G_2} = -8V.$$

$$V_{G_1} = V_{G_2} = -8V.$$

Discussion

The circuit should operate in the manner described earlier. Consequently, you should have noted the following:

V_{G_1}	V_{G_2}	v_o
$-8V$	$0V$	Triangular wave
$0V$	$-8V$	Pulse
$-8V$	$-8V$	$\approx 0V$
$0V$	$0V$	Complex wave

Analog multiplexers are used in data transmission systems, function generators, and many other applications. Numerous IC analog multiplexers are available that simplify system design.

EXPERIMENT 13

FREQUENCY EFFECTS

Objective:

To investigate the effect of frequency variations in a typical RC-coupled common-emitter amplifier.

Introduction

In an RC-coupled amplifier, coupling and bypass capacitors constitute high-pass filters which shape the low-frequency region of the overall frequency response curve. For this reason, the amplifier's lower cutoff frequency, F_1 , approximately equals F_{b_1} , F_{C_1} , or F_{e_1} , whichever is larger.

Similarly, the input and output capacitances function as low-pass filters which determine the high-frequency characteristics of the amplifier. The amplifier's upper cutoff frequency, F_2 approximately equals F_{b_2} or F_{C_2} , whichever is smaller.

In this experiment, you will measure the cutoff frequencies of the $\times 10$ common-emitter amplifier designed in Experiment 4.

You will use several different capacitor values so you can independently examine the effect of each internal filter.

Material Required

Heathkit Engineering Design Trainer ET-1000

Oscilloscope

1 — NPN type 2N3904 transistor (417-875)

1 — 2.2k Ω , 1/4-watt, 5% resistor

1 — 3.3k Ω , 1/4-watt, 5% resistor

1 — 3.9k Ω , 1/4-watt, 5% resistor

2 — 120 Ω , 1/4-watt, 5% resistors

2 — 560 Ω , 1/4-watt, 5% resistors

1 — 0.01 μ F, 25V ceramic capacitor

1 — 0.1 μ F, 25V ceramic capacitor

1 — 1 μ F, 50V electrolytic capacitor

1 — 0.1 μ F, Mylar* capacitor

3 — 47 μ F, 50V electrolytic capacitors

* Dupont registered trademark, Heath #A-8 27-77.

Test Circuit

The test circuit that you will construct in this experiment is illustrated in Figure E13-1. Note that a 600Ω , 20dB attenuator has been placed between the signal source and the amplifier. The purpose of the attenuator is twofold. First, the attenuator serves to reduce the amplitude of the signal source so that the amplifier is not overdriven. Second, the attenuator provides an effective Thevenin or source resistance, when viewed from the amplifier's input terminals, of approximately 600Ω . This is important, since the cutoff frequencies of the base and emitter filters depend upon the specific value of R_S .

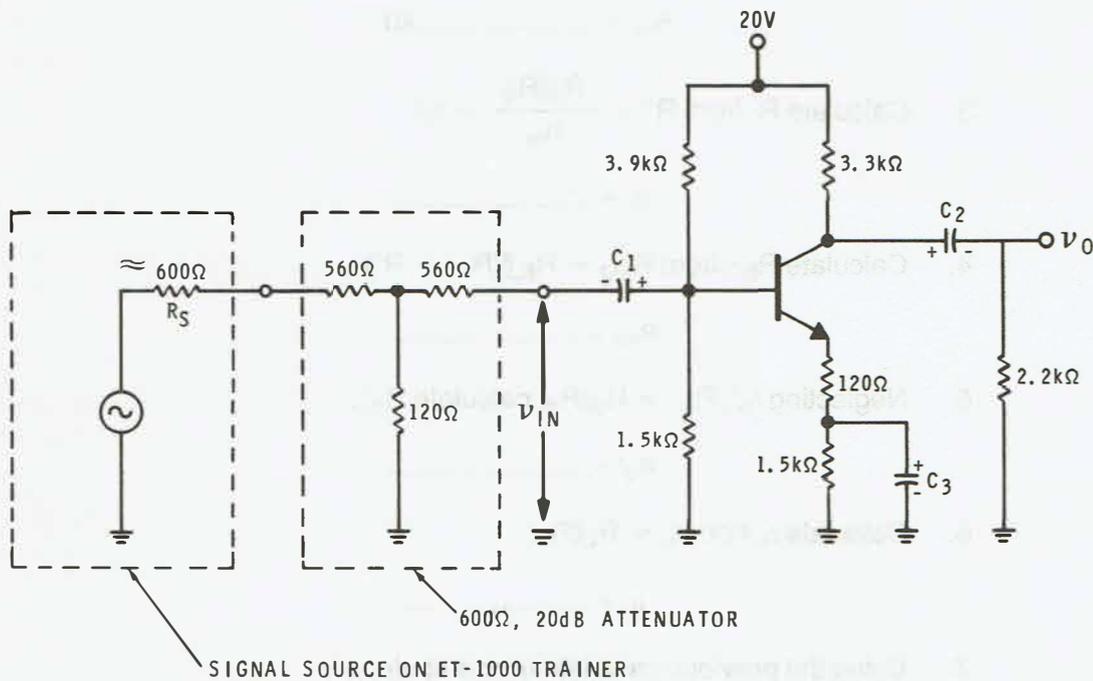


Figure E13-1

$\times 10$ common-emitter amplifier.

Procedure

The amplifier in Figure E13-1 was designed so that $I_{CQ} = 3\text{mA}$ and $A_V = -10$ in the mid-frequency region. For calculation purposes, we will assume $h_{fe} = 200$ and $r_{e'} = 12.3\Omega$.

1. Calculate $R_{IN(BASE)}$ from $R_{IN(BASE)} = h_{fe}(R_{E_1} + r_{e'})$:

$$R_{IN(BASE)} = \underline{\hspace{2cm}} \text{ k}\Omega.$$

2. Calculate R_{IN} from $R_{IN} = R_B || R_{IN(BASE)}$:

$$R_{IN} = \underline{\hspace{2cm}} \text{ k}\Omega.$$

3. Calculate R' from $R' = \frac{R_B || R_S}{h_{fe}} + r_{e'}$:

$$R' = \underline{\hspace{2cm}}.$$

4. Calculate R_{EQ} from $R_{EQ} = R_{E_2} || (R_{E_1} + R')$

$$R_{EQ} = \underline{\hspace{2cm}}.$$

5. Neglecting $r_{b'}$, $R_S' = R_S || R_B$, calculate R_S' :

$$R_S' = \underline{\hspace{2cm}}.$$

6. Calculate r_L from $r_L = R_C || R_L$:

$$r_L = \underline{\hspace{2cm}}.$$

7. Using the previous calculations, compute:

$$R_S + R_{IN} = \underline{\hspace{2cm}}.$$

$$R_C + R_L = \underline{\hspace{2cm}}.$$

$$R_{EQ} = \underline{\hspace{2cm}}.$$

$$R_S' || R_{IN(BASE)} = \underline{\hspace{2cm}}.$$

Discussion

The purpose of steps 1-7 is to get the preliminary calculations completed so that you can proceed with the experiment. Your calculations for step 1-7 should be similar to the following.

$$\begin{aligned} 1. \quad R_{IN(BASE)} &= h_{fe}(R_{E_1} + r_{e'}) \\ &= 200(120\Omega + 12.3\Omega) \\ &= 26.46k\Omega. \end{aligned}$$

$$\begin{aligned} 2. \quad R_{IN} &= R_B \parallel R_{IN(BASE)} \\ &= 3.9k\Omega \parallel 1.5k\Omega \parallel 26.46k\Omega \\ &= 1.08k\Omega \parallel 26.46k\Omega \\ &= 1.04k\Omega. \end{aligned}$$

$$\begin{aligned} 3. \quad R' &= \frac{R_B \parallel R_S}{h_{fe}} + r_{e'} \\ &= \frac{1.08k\Omega \parallel 600\Omega}{200} + 12.3\Omega \\ &= \frac{285.7\Omega}{200} + 12.3 = 14.23\Omega. \end{aligned}$$

$$\begin{aligned} 4. \quad R_{EQ} &= R_{E_2} \parallel (R_{E_1} + R') \\ &= 1.5k\Omega \parallel (120\Omega + 14.23\Omega) \\ &= 123.2\Omega. \end{aligned}$$

$$5. \quad R_{S'} = R_S \parallel R_B = 600\Omega \parallel 1.08k\Omega = 385.7\Omega.$$

$$6. \quad r_L = R_C \parallel R_L = 3.3k\Omega \parallel 2.2k\Omega = 1.32k\Omega.$$

$$7. \quad (R_S + R_{IN}) = 600\Omega + 1.04k\Omega = 1.64k\Omega.$$

$$(R_C + R_L) = 3.3k\Omega + 2.2k\Omega = 5.5k\Omega.$$

$$R_{EQ} = 123.2\Omega.$$

$$R_{S'} \parallel R_{IN(BASE)} = 385.7\Omega \parallel 26.46k\Omega = 380\Omega.$$

Procedure (Continued)

8. The cutoff frequency of the high-pass base filter is:

$$F_{b_1} = \frac{1}{2\pi(R_S + R_{IN})C_1}$$

Since $1/2\pi = 0.159$ and $(R_S + R_{IN}) = 1.64\text{k}\Omega$, we have:

$$F_{b_1} = \frac{0.159}{(1.64\text{k}\Omega)C_1}$$

Calculate the value of F_{b_1} for $C_1 = 0.01\mu\text{F}$, $0.1\mu\text{F}$, and $1\mu\text{F}$. Record your calculated values in the space provided in Table E13-1.

C_1	$F_{b_1}(\text{CAL})$	$F_{b_1}(\text{MEAS})$
$0.01\mu\text{F}$		
$0.1\mu\text{F}$		
$1\mu\text{F}$		

Table E13-1

High-pass base filter.

9. To ensure that the high-pass base filter has a cutoff frequency higher than F_{c_1} and F_{e_1} , we will make C_2 equal to C_3 and large compared to C_1 . Thus:

$$C_2 = C_3 = 47\mu\text{F}.$$

With $C_1 = 0.01\mu\text{F}$ construct the circuit shown in Figure E13-1. As usual, make sure the electrolytic capacitors are placed in the circuit with the correct polarity.

10. Turn the power on and set the frequency control to obtain a 100kHz output signal.

11. Measure the peak input, v_{IN} and output voltage, v_O

$$v_{IN} = \text{_____ V peak.}$$

$$v_O = \text{_____ V peak.}$$

Since the amplifier was designed to provide a mid-frequency voltage gain of 10, the ratio of v_O to v_{IN} should be close to 10.

12. Decrease the frequency of the input signal until $v_O = 0.707$ times the value measured in step 11. Record the measured frequency in Table E13-1.
13. Repeat step 12 for $C_1 = 0.1\mu\text{F}$ and $C_1 = 1\mu\text{F}$.

Discussion

The values calculated for F_{b_1} in step 8 are:

C_1	$F_{b_1}(\text{CAL})$
$0.01\mu\text{F}$	9.7kHz
$0.1\mu\text{F}$	940Hz
$1\mu\text{F}$	97Hz

Since component values were used to ensure $F_{b_1} > F_{c_1}$ and $F_{b_1} > F_{e_1}$, the value of F_{b_1} essentially establishes the amplifier's lower cutoff frequency, F_1 .

Due to parameter variations and component tolerances, the values of F_1 measured in steps 12 and 13 probably differ from the values calculated in step 8. Typically, your calculated and measured values in this portion of the experiment will be within 30% of each other.

Procedure (Continued)

14. The cutoff frequency of the high-pass collector filter is:

$$F_{c_1} = \frac{1}{2\pi(R_C + R_L)C_2}$$

Substituting 0.159 for $1/2\pi$, and $5.5k\Omega$ for $(R_C + R_L)$ yields:

$$F_{c_1} = \frac{0.159}{(5.5k\Omega)C_2}$$

Calculate the value of F_{c_1} for $C_1 = 0.01\mu F$, $0.1\mu F$, and $1\mu F$. Record your calculated values in Table E13-2.

C_2	$F_{c_1}(\text{CAL})$	$F_{c_1}(\text{MEAS})$
$0.01\mu F$		
$0.1\mu F$		
$1\mu F$		

Table E13-2

High-pass collector filter.

15. To ensure that the high-pass collector filter has a cutoff frequency higher than F_{b_1} and F_{e_1} , we will select:

$$C_1 = C_3 = 47\mu F.$$

With $C_2 = 0.01\mu F$, adjust the frequency of the input signal to 10kHz. Now decrease the frequency until $v_O = 0.707$ times the value measured in step 11. Record the measured frequency in Table E13-2.

16. Repeat step 15 for $C_2 = 0.1\mu F$ and $C_2 = 1\mu F$.

17. The cutoff frequency of the high-pass emitter filter is:

$$F_{e_1} = \frac{1}{2\pi R_{EQ} C_3}$$

Substituting 0.159 for $1/2\pi$ and 123.2Ω for R_{EQ} yields:

$$F_{e_1} = \frac{0.159}{(123.2\Omega)C_3}$$

Calculate the value of F_{e_1} for $C_3 = 0.01\mu\text{F}$, $0.1\mu\text{F}$, and $1\mu\text{F}$. Record your calculated values in Table E13-3.

C_3	$F_{e_1}(\text{CAL})$	$F_{e_1}(\text{MEAS})$
$0.01\mu\text{F}$		
$0.1\mu\text{F}$		
$1\mu\text{F}$		

Table E13-3

High-pass emitter filter.

18. By making $C_1 = C_2 = 47\mu\text{F}$, the cutoff frequency of the high-pass emitter filter will be higher than F_{b_1} and F_{c_1} .

Following a procedure similar to the one used for the base and collector filters, measure F_1 for $C_3 = 0.01\mu\text{F}$, $0.1\mu\text{F}$, and $1\mu\text{F}$. Record the measured values in Table E13-3.

Discussion

The calculated values for steps 14 and 17 are:

STEP 14

STEP 17

C_2	$F_{c_1}(\text{CAL})$	C_3	$F_{e_1}(\text{CAL})$
0.01 μF	2.89kHz	0.01 μF	129kHz
0.1 μF	289Hz	0.1 μF	12.9kHz
1 μF	28.9Hz	1 μF	1.29kHz

In steps 15 and 16, F_{c_1} dominates. Similarly, in step 18, F_{e_1} dominates. Consequently, the values of F_1 measured in steps 15 and 16 should approximately equal the values of F_{c_1} calculated in step 14. Similarly, the values of F_1 measured in step 18 should roughly agree with the calculated values of F_{e_1} in step 17.

Procedure (Continued)

In order to predict the cutoff frequencies of the low-pass base and collector filters, you need to know the values of C_{IN} and C_O . Typically, C_{IN} and C_O have values in the pF range.

To simplify the experimental procedure we will:

- Let $C_1 = C_2 = C_3 = 47\mu\text{F}$. This ensures that the lower cutoff frequency, F_1 , will be quite small.
- When examining the low-pass collector filter, we will shunt R_L with a 0.1 μF capacitor. This essentially makes $C_O = 0.1\mu\text{F}$, and ensures that $F_{c_2} < F_{b_2}$.
- When examining the low-pass base filter, we will connect a 0.1 μF capacitor between the transistor's base and ground.

This makes C_{IN} essentially equal to 0.1 μF and ensures that $F_{b_2} < F_{c_2}$.

By shunting the input or output with a large, 0.1 μF capacitor, the upper cutoff frequency, F_2 , will be low enough so that it is easy to measure.

19. The cutoff frequency of the low-pass collector filter is:

$$F_{c_2} = \frac{1}{2\pi r_L C_O}$$

Calculate F_{c_2} assuming $r_L = 1.32k\Omega$ and $C_O = 0.1\mu F$.

$$F_{c_2(CAL)} = \underline{\hspace{2cm}}$$

20. With $C_1 = C_2 = C_3 = 47\mu F$, adjust the frequency of the signal source to 10kHz. Connect a $0.1\mu F$ Mylar capacitor in parallel with the $2.2k\Omega$ load resistor.

21. Reduce the frequency of the signal source until $v_O = 0.707$ of the mid-frequency value. Record the measured value of F_2 .

$$F_2 = \underline{\hspace{2cm}}$$

22. The cutoff frequency of the low-pass base filter is:

$$F_{b_2} = \frac{1}{2\pi(R_S' \parallel R_{IN(BASE)})C_{IN}}$$

Calculate F_{b_2} assuming $(R_S' \parallel R_{IN(BASE)}) = 380\Omega$ and $C_{IN} = 0.1\mu F$.

$$F_{b_2(CAL)} = \underline{\hspace{2cm}}$$

23. Remove the $0.1\mu F$ Mylar capacitor from R_L . Connect the capacitor between the base of the transistor and ground. Adjust the frequency of the signal source to 10kHz.

24. Reduce the frequency of the signal source until $v_O = 0.707$ of the mid-frequency value. Record the measured value of F_2 .

$$F_2 = \underline{\hspace{2cm}}$$

Discussion

The values of F_{c_2} and F_{b_2} calculated in steps 19 and 22 respectively, are:

$$F_{c_2} = 4.18\text{kHz.}$$

$$F_{b_2} = 1.2\text{kHz.}$$

Consequently, the values of F_2 measured in steps 21 and 24 respectively, should be approximately equal to the calculated values.

APPENDIX A

RESISTOR COLOR CODE CHART

COLOR CODE CHART FIXED RESISTORS



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First Band	Second Band	Multiplier Band	Resistance Ω	First Band	Second Band	Multiplier Band	Resistance Ω	
Brown	Black	Black	10	Red	Black	Black	20	
		Brown	100			Brown	Brown	200
		Red	1000			Red	Red	2000
		Orange	10000			Orange	Orange	20000
		Yellow	0.1 Meg.			Yellow	Yellow	0.20 Meg.
		Green	1.0 Meg.			Green	Green	2.0 Meg.
		Blue	10.0 Meg.			Blue	Blue	20.0 Meg.
		Gray	10.0 Meg.					
	Brown	Black	11		Red	Black	22	
		Brown	110			Brown	220	
		Red	1100			Red	2200	
		Orange	11000			Orange	22000	
		Yellow	0.11 Meg.			Yellow	0.22 Meg.	
		Green	1.1 Meg.			Green	2.2 Meg.	
		Blue	11.0 Meg.			Blue	22.0 Meg.	
	Red	Black	12		Yellow	Black	24	
		Brown	120			Brown	240	
		Red	1200			Red	2400	
		Orange	12000			Orange	24000	
		Yellow	0.12 Meg.			Yellow	0.24 Meg.	
		Green	1.2 Meg.			Green	2.4 Meg.	
		Blue	12.0 Meg.					
	Orange	Black	13		Violet	Gold	2.7	
		Brown	130			Black	27	
		Red	1300			Brown	270	
		Orange	13000			Red	2700	
		Yellow	0.13 Meg.			Orange	27000	
		Green	1.3 Meg.			Yellow	0.27 Meg.	
		Blue	13.0 Meg.			Green	2.7 Meg.	
	Green	Black	15					
		Brown	150					
		Red	1500					
		Orange	15000					
		Yellow	0.15 Meg.					
		Green	1.5 Meg.					
		Blue	15.0 Meg.					
	Blue	Black	16					
		Brown	160					
		Red	1600					
		Orange	16000					
		Yellow	0.16 Meg.					
		Green	1.6 Meg.					
		Blue	16.0 Meg.					
	Gray	Black	18					
		Brown	180					
		Red	1800					
		Orange	18000					
		Yellow	0.18 Meg.					
		Green	1.8 Meg.					
		Blue	18.0 Meg.					

Standard C

BANDS: 1 2 3

5-BAND RESISTORS
($\pm 1\%$)



4-BAND RESISTORS
($\pm 10\%$)
($\pm 5\%$)



BANDS: 1 2 Mu



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MICHIGAN 49022

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597-1715

Band 1 1st Digit	
Color	Digit
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Gray	8
White	9

Band 2 2nd Digit	
Color	Digit
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Gray	8
White	9

Band 3 3rd Digit	
Color	Digit
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Gray	8
White	9

R RESISTORS

First Band	Second Band	Multiplier Band	Resistance Ω	First Band	Second Band	Multiplier Band	Resistance Ω	
Orange	Black	Gold	3.0	Yellow	Orange	Gold	4.3	
		Black	30			Black	43	
		Brown	300			Brown	430	
		Red	3000			Red	4300	
		Orange	30000			Orange	43000	
		Yellow	0.30 Meg.			Yellow	0.43 Meg.	
		Green	3.0 Meg.			Green	4.3 Meg.	
	Orange	Gold	3.3		Violet	Gold	4.7	
		Black	33	Black		47		
		Brown	330	Brown		470		
		Red	3300	Red		4700		
		Orange	33000	Orange		47000		
		Yellow	0.33 Meg.	Yellow		0.47 Meg.		
		Green	3.3 Meg.	Green	4.7 Meg.			
	Blue	Gold	3.6	Green	Brown	Gold	5.1	
			Black			36	Black	51
			Brown			360	Brown	510
			Red			3600	Red	5100
			Orange			36000	Orange	51000
			Yellow			0.36 Meg.	Yellow	0.51 Meg.
		Green	3.6 Meg.	Green	5.1 Meg.			
	White	Gold	3.9	Blue	Blue	Gold	5.6	
			Black			39	Black	56
			Brown			390	Brown	560
			Red			3900	Red	5600
			Orange			39000	Orange	56000
			Yellow			0.39 Meg.	Yellow	0.56 Meg.
		Green	3.9 Meg.	Green	5.6 Meg.			

Color Code

Multiplier Tolerance



* Note Wide Space



Multiplier Tolerance

Digit	Color	Multiplier	Color	Tolerance
0	Black	1	Silver	$\pm 10\%$
1	Brown	10	Gold	$\pm 5\%$
2	Red	100	Brown	$\pm 1\%$
3	Orange	1,000		
4	Yellow	10,000		
5	Green	100,000		
6	Blue	1,000,000		
7	Silver	0.01		
8	Gold	0.1		
9				

Blue	Red	Gold	6.2	Red	Gold	8.2	
		Black	62		Black	82	
		Brown	620		Brown	820	
		Red	6200		Red	8200	
		Orange	62000		Orange	82000	
		Yellow	0.62 Meg.		Yellow	0.82 Meg.	
		Green	6.2 Meg.			Green	8.2 Meg.
Violet	Gray	Gold	6.8	Green	Gold	7.5	
		Black	68		Black	75	
		Brown	680		Brown	750	
		Red	6800		Red	7500	
		Orange	68000		Orange	75000	
		Yellow	0.68 Meg.		Yellow	0.75 Meg.	
		Green	6.8 Meg.			Green	7.5 Meg.
White	Red	Gold	8.2	Brown	Gold	9.1	
		Black	82		Black	91	
		Brown	820		Brown	910	
		Red	8200		Red	9100	
		Orange	82000		Orange	91000	
		Yellow	0.82 Meg.		Yellow	0.91 Meg.	
		Green	8.2 Meg.			Green	9.1 Meg.

Brown	110
Red	1100
Orange	11000
Yellow	0.11 Meg.
Green	1.1 Meg.
Blue	11.0 Meg.

Black	12
Brown	120
Red	1200
Orange	12000
Yellow	0.12 Meg.
Green	1.2 Meg.
Blue	12.0 Meg.

Black	13
Brown	130
Red	1300
Orange	13000
Yellow	0.13 Meg.
Green	1.3 Meg.
Blue	13.0 Meg.

Black	15
Brown	150
Red	1500
Orange	15000
Yellow	0.15 Meg.
Green	1.5 Meg.
Blue	15.0 Meg.

Black	16
Brown	160
Red	1600
Orange	16000
Yellow	0.16 Meg.
Green	1.6 Meg.
Blue	16.0 Meg.

Black	18
Brown	180
Red	1800
Orange	18000
Yellow	0.18 Meg.
Green	1.8 Meg.
Blue	18.0 Meg.

Red	220
Orange	22000
Yellow	0.22 Meg.
Green	2.2 Meg.
Blue	22.0 Meg.

Red	24
Yellow	240
Black	2400
Orange	24000
Green	0.24 Meg.
Blue	2.4 Meg.

Gold	2.7
Black	27
Brown	270
Red	2700
Orange	27000
Yellow	0.27 Meg.
Green	2.7 Meg.

Gold	3.6
Black	36
Brown	360
Red	3600
Orange	36000
Yellow	0.36 Meg.
Green	3.6 Meg.

Gold	3.9
Black	39
Brown	390
Red	3900
Orange	39000
Yellow	0.39 Meg.
Green	3.9 Meg.

Gold	33
Black	330
Red	3300
Orange	33000
Yellow	0.33 Meg.
Green	3.3 Meg.

Gold	330
Black	3300
Brown	33000
Red	0.33 Meg.
Orange	3.3 Meg.
Yellow	3.6
Green	36
Blue	360
White	3600
White	36000
White	0.36 Meg.
White	3.6 Meg.

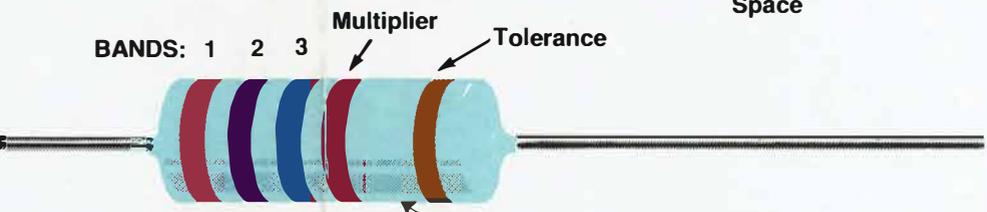
Gold	3.6
Black	36
Brown	360
Red	3600
Orange	36000
Yellow	0.36 Meg.
Green	3.6 Meg.

Gold	3.9
Black	39
Brown	390
Red	3900
Orange	39000
Yellow	0.39 Meg.
Green	3.9 Meg.

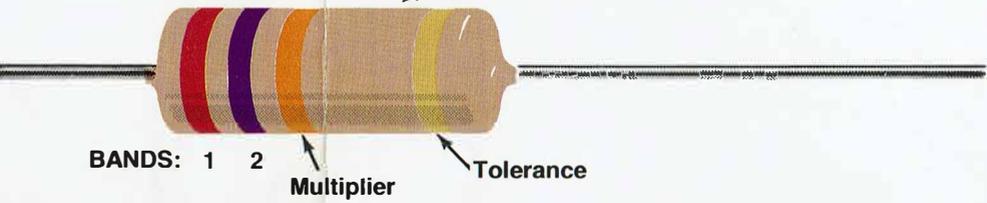
Standard Color Code

* Note Wide Space

5-BAND RESISTORS
(±1%)



4-BAND RESISTORS
(±10%)
(±5%)



Band 1 1st Digit	
Color	Digit
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Gray	8
White	9

Band 2 2nd Digit	
Color	Digit
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Gray	8
White	9

Band 3 (if used) 3rd Digit	
Color	Digit
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Gray	8
White	9

Multiplier	
Color	Multiplier
Black	1
Brown	10
Red	100
Orange	1,000
Yellow	10,000
Green	100,000
Blue	1,000,000
Silver	0.01
Gold	0.1

Resistance Tolerance	
Color	Tolerance
Silver	±10%
Gold	±5%
Brown	±1%

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BENTON HARBOR,
MICHIGAN 49022

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INTRODUCTION

The purpose of this introduction is to provide a brief overview of the contents of the manual. The manual is divided into several sections, each of which is described in detail in the following paragraphs.

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APPENDIX B

DATA SHEETS, CIRCUIT CONFIGURATIONS, PARAMETERS, AND DESIGN GUIDES

INTRODUCTION

This appendix is a compendium of the circuit configurations, parameters, and design guides found throughout this text. The caption indicates the unit from which the material was obtained. For instance:

TABLE 1-3

Approximate BJT Formulas (from Page 1-35)

Indicates that the discussion concerning this table can be found in Unit 1 near Page 35.

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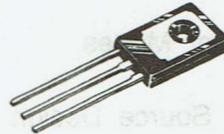
MJE170 thru MJE172 PNP (SILICON) MJE180 thru MJE182 NPN

COMPLEMENTARY PLASTIC SILICON POWER TRANSISTORS

... designed for low power audio amplifier and low current, high speed switching applications.

- Collector-Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 40 \text{ Vdc} - \text{MJE170, MJE180}$
 $= 60 \text{ Vdc} - \text{MJE171, MJE181}$
 $= 80 \text{ Vdc} - \text{MJE172, MJE182}$
- DC Current Gain –
 $h_{FE} = 30 \text{ (Min) @ } I_C = 0.5 \text{ Adc}$
 $= 12 \text{ (Min) @ } I_C = 1.5 \text{ Adc}$
- Current-Gain – Bandwidth Product –
 $f_T = 50 \text{ MHz (Min) @ } I_C = 100 \text{ mAdc}$
- Annular Construction for Low Leakages –
 $I_{CBO} = 100 \text{ nA (Max) @ Rated } V_{CB}$

**3 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
40-60-80 VOLTS
12.5 WATTS**



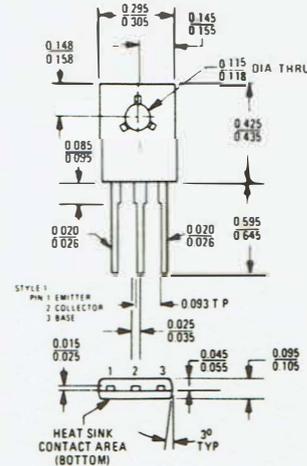
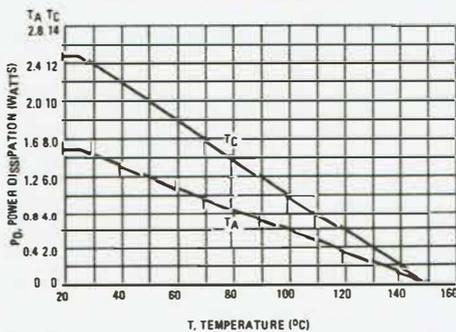
MAXIMUM RATINGS

Rating	Symbol	MJE170 MJE180	MJE171 MJE181	MJE172 MJE182	Unit
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	7.0			Vdc
Collector Current – Continuous Peak	I_C	3.0 6.0			Adc
Base Current	I_B	1.0			Adc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.5 0.012			Watts W/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	12.5 0.1			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	$^\circ\text{C/W}$

FIGURE 1 – POWER DERATING



CASE 77-03

MJE170, MJE171, MJE172, MJE180, MJE181, MJE182 (continued)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage ($I_C = 10 \text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	MJE 170, MJE 180 MJE 171, MJE 181 MJE 172, MJE 182	40 60 80	Vdc	
Collector Cutoff Current ($V_{CB} = 60 \text{ Vdc}$, $I_E = 0$)		I_{CBO}	MJE 170, MJE 180	—	μAdc
($V_{CB} = 80 \text{ Vdc}$, $I_E = 0$)			MJE 171, MJE 181	—	0.1
($V_{CB} = 100 \text{ Vdc}$, $I_E = 0$)	MJE 172, MJE 182		—	0.1	
($V_{CB} = 60 \text{ Vdc}$, $I_E = 0$, $T_C = 150^\circ\text{C}$)	MJE 170, MJE 180		—	0.1	
($V_{CB} = 80 \text{ Vdc}$, $I_E = 0$, $T_C = 150^\circ\text{C}$)	MJE 171, MJE 181		—	0.1	
($V_{CB} = 100 \text{ Vdc}$, $I_E = 0$, $T_C = 150^\circ\text{C}$)	MJE 172, MJE 182	—	0.1		
Emitter Cutoff Current ($V_{BE} = 7.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	0.1	μAdc	
ON CHARACTERISTICS					
DC Current Gain ($I_C = 100 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 500 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 1.5 \text{ Adc}$, $V_{CE} = 1.0 \text{ Vdc}$)	h_{FE}		50 30 12	—	
Collector-Emitter Saturation Voltage ($I_C = 500 \text{ mAdc}$, $I_B = 50 \text{ mAdc}$) ($I_C = 1.5 \text{ Adc}$, $I_B = 150 \text{ mAdc}$) ($I_C = 3.0 \text{ Adc}$, $I_B = 600 \text{ mAdc}$)		$V_{CE(sat)}$		— — —	0.3 0.9 1.7
Base-Emitter Saturation Voltage ($I_C = 1.5 \text{ Adc}$, $I_B = 150 \text{ mAdc}$) ($I_C = 3.0 \text{ Adc}$, $I_B = 600 \text{ mAdc}$)			$V_{BE(sat)}$		— —
Base-Emitter On Voltage ($I_C = 500 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$)	$V_{BE(on)}$			—	—
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (1) ($I_C = 100 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{test} = 10 \text{ MHz}$)	f_T	50	—	MHz	
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	MJE 170/MJE 172 MJE 180/MJE 182	— —	50 30	
					μF

(1) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

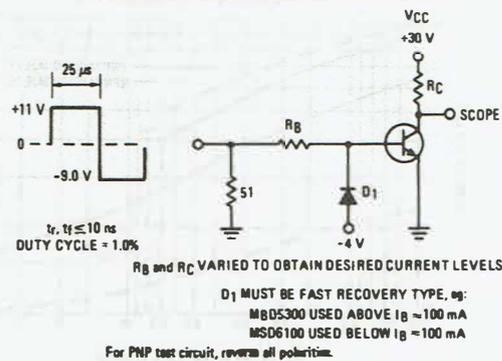
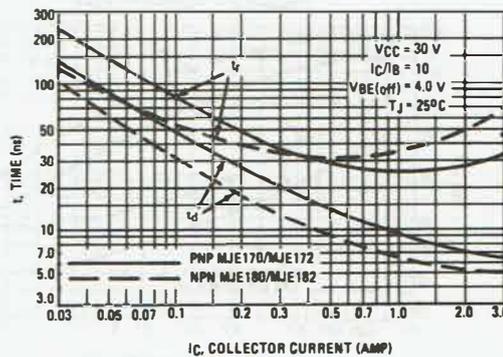
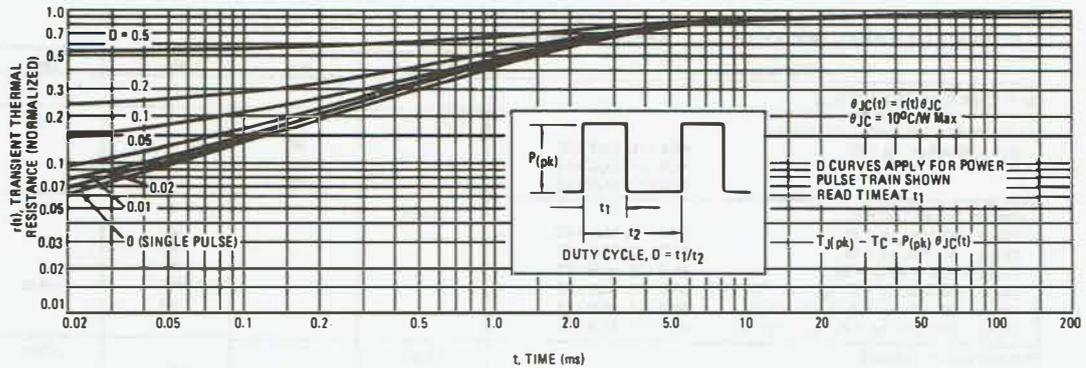


FIGURE 3 – TURN-ON TIME



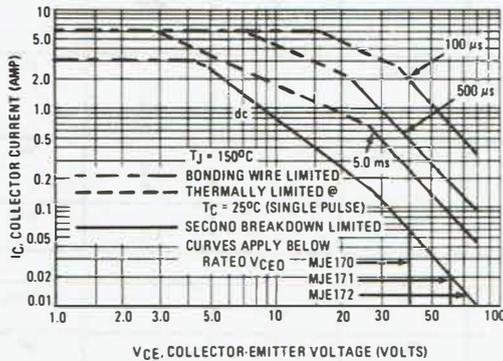
MJE170, MJE171, MJE172, MJE180, MJE181, MJE182 (continued)

FIGURE 4 - THERMAL RESPONSE



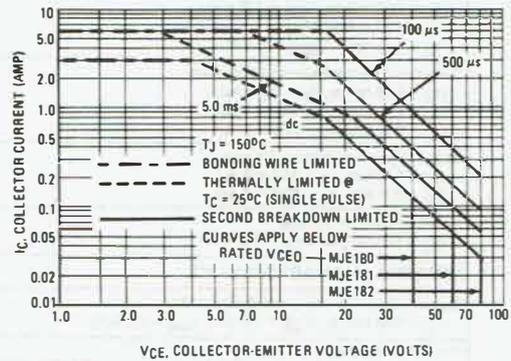
ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 - MJE170, MJE171, MJE172



There are two limitations on the power handling ability of a transistor - average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figures 5 and 6 is based on $T_J(pk) = 150^\circ\text{C}$; T_C is

FIGURE 6 - MJE180, MJE181, MJE182



variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_J(pk) < 150^\circ\text{C}$. $T_J(pk)$ may be calculated from the data in Figure 4. At high case temperature, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 7 - TURN-OFF TIME

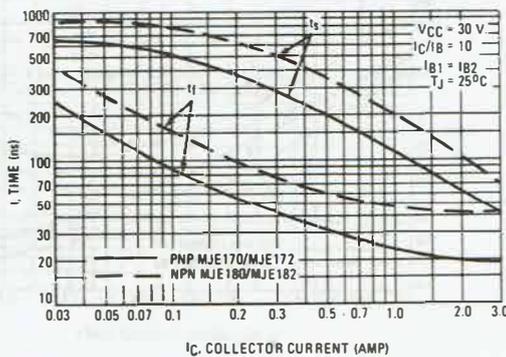
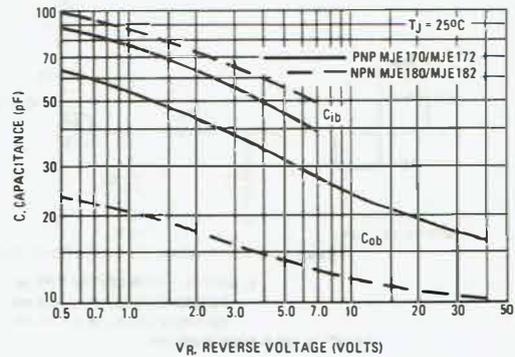
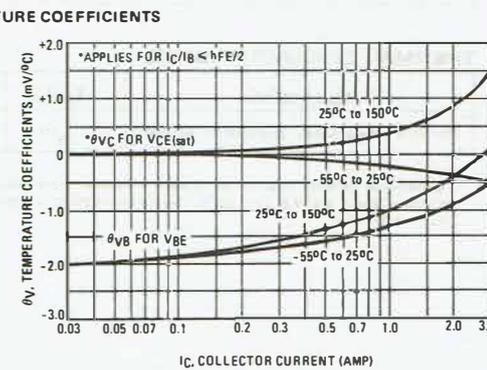
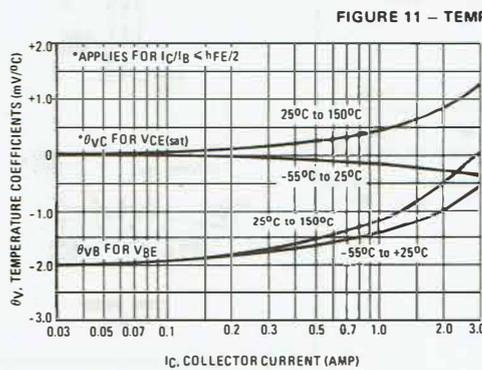
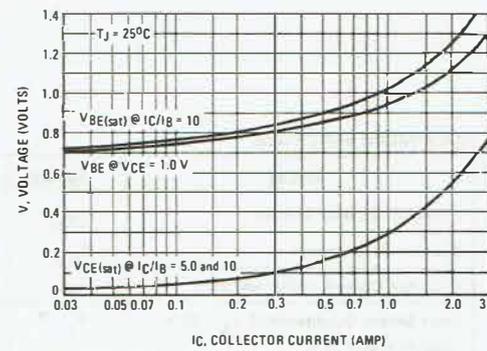
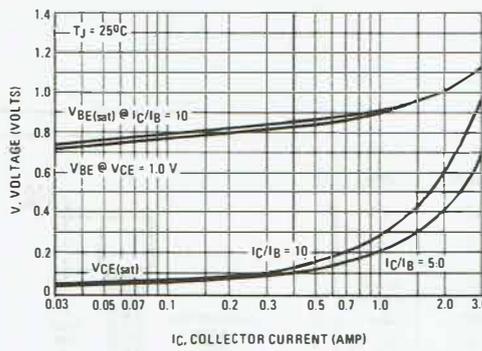
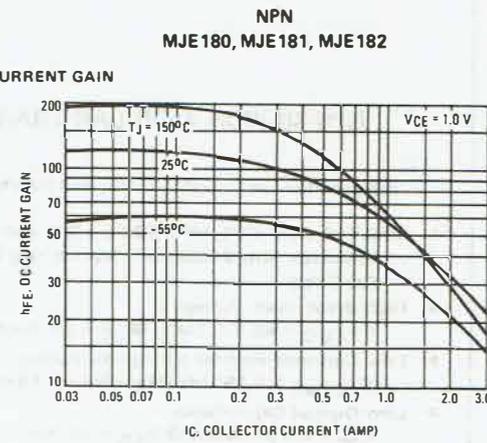
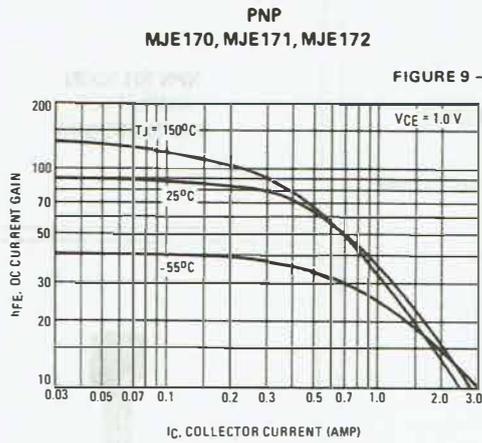


FIGURE 8 - CAPACITANCE



MJE170, MJE171, MJE172, MJE180, MJE181, MJE182 (continued)



MPS-A20 (SILICON) MPS-K20, MPS-K21, MPS-K22

NPN SILICON ANNULAR TRANSISTORS

... designed for use in audio, radio, and television applications.

- MPS-K20, MPS-K21, MPS-K22 are 3, 5 and 9 Transistor Kits Available in Varied h_{FE} Ranges - See Table 1
- High Breakdown Voltage - $V_{CEO} = 40$ Vdc (Min) @ $I_C = 1.0$ mAdc
- Low Collector-Emitter Saturation Voltage - $V_{CE(sat)} = 0.25$ Vdc (Max) @ $I_C = 10$ mAdc
- Low Output Capacitance - $C_{ob} = 4.0$ pF (Max) @ $V_{CB} = 10$ Vdc

NPN SILICON AMPLIFIER TRANSISTORS



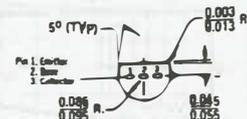
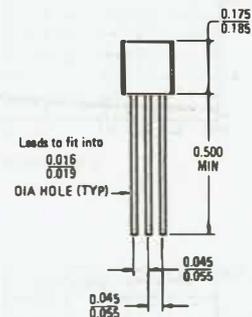
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current - Continuous	I_C	100	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	$P_D^{(1)}$	300 2.73	mW mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}^{(1)}$	-55 to +135	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$\theta_{JA}^{(1)}$	0.367	$^\circ\text{C}/\text{mW}$

(1) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows: $P_D = 1.0$ W @ $T_C = 25^\circ\text{C}$, Derate above $25^\circ\text{C} - 8.0$ mW/ $^\circ\text{C}$, $T_J = -65$ to $+150^\circ\text{C}$, $\theta_{JC} = 125^\circ\text{C}/\text{W}$.



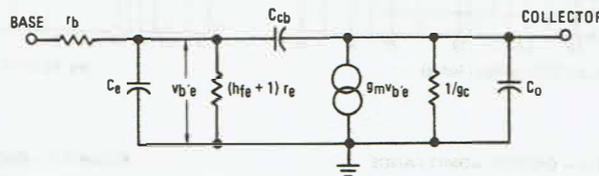
CASE 29-02
TO-92

MPS-A20, MPS-K20, MPS-K21, MPS-K22 (continued)

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ($I_C = 1.0 \text{ mAdc}$, $I_B = 0$)	BV_{CEO}	40	-	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100 \mu\text{Adc}$, $I_C = 0$)	BV_{EBO}	4.0	-	Vdc
Collector Cutoff Current ($V_{CB} = 30 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	-	100	nAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 5.0 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$)	h_{FE}	40	400	-
Collector-Emitter Saturation Voltage ($I_C = 10 \text{ mAdc}$, $I_B = 1.0 \text{ mAdc}$)	$V_{CE(sat)}$	-	0.25	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product ($I_C = 5.0 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 100 \text{ MHz}$)	f_T	125	-	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 100 \text{ kHz}$)	C_{ob}	-	4.0	pF

FIGURE 1 – SIMPLIFIED AC EQUIVALENT CIRCUIT (Common Emitter)



Notes:

Data for MPS-A20 is presented in terms of the equivalent circuit shown in Figure 1. Values for its components may be found or calculated as follows:

$$r_b' - \text{See Figure 8} \quad C_{cb} = C_{ob} - 0.2 \text{ pF (See Figure 6)}$$

$$r_e = 26 \text{ mV}/I_E \quad g_m = 1/r_e$$

$$C_e = \frac{1}{2\pi f_T r_e} \quad g_c = (h_{fe} + 1) h_{ob} \text{ (See Figures 2 \& 7)}$$

$$C_o = 0.2 \text{ pF}$$

Low frequency h parameters may be found from:

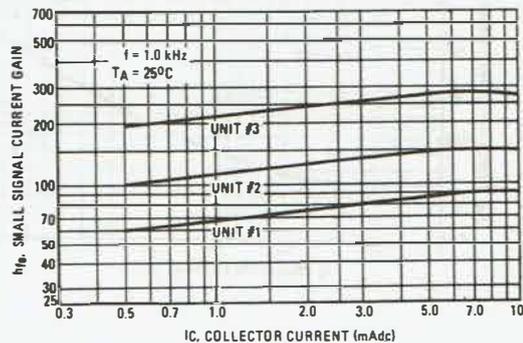
$$h_{ie} = r_b' + (h_{fe} + 1) r_e$$

$$h_{fe} = \text{See Figure 2}$$

$$h_{re} = \text{Negligible}$$

$$h_{oe} = (h_{fe} + 1) h_{ob}$$

FIGURE 2 – SMALL SIGNAL CURRENT GAIN



MPS-A20, MPS-K20, MPS-K21, MPS-K22 (continued)

FIGURE 3 - NORMALIZED DC CURRENT GAIN

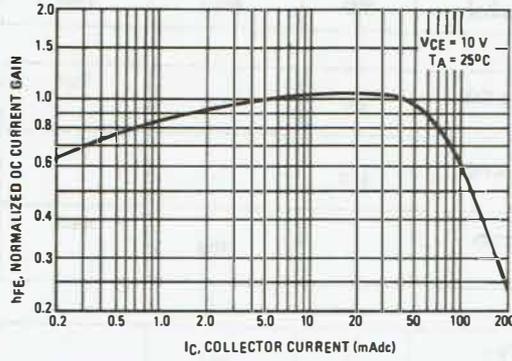


FIGURE 4 - "SATURATION" AND "ON" VOLTAGES

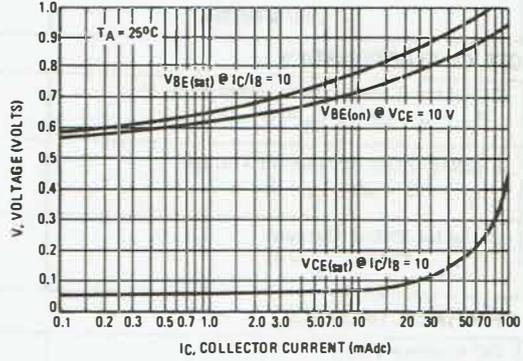


FIGURE 5 - CURRENT-GAIN-BANDWIDTH PRODUCT

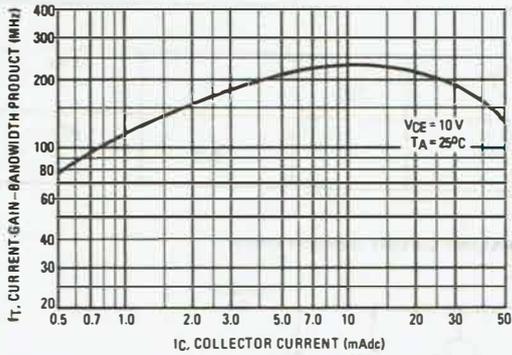


FIGURE 6 - CAPACITANCES

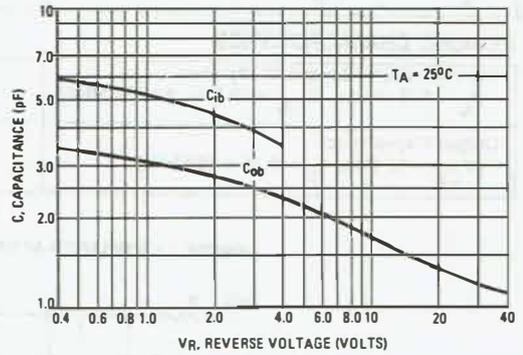


FIGURE 7 - OUTPUT ADMITTANCE

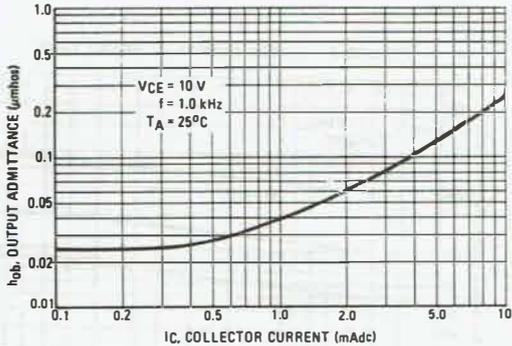
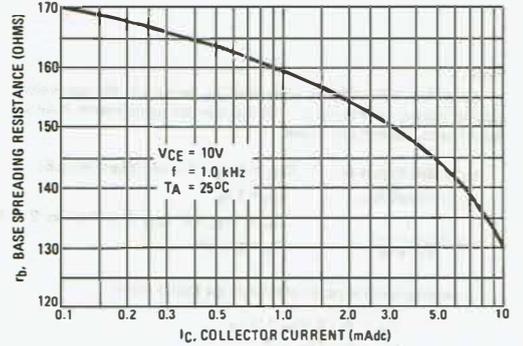
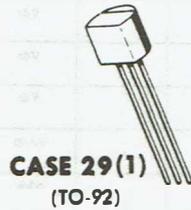


FIGURE 8 - BASE SPREADING RESISTANCE



2N3903 (SILICON)
2N3904



NPN silicon annular transistors, designed for general-purpose switching and amplifier applications, features one-piece, injection-molded plastic package for high reliability. The 2N3903 and 2N3904 are complementary with PNP types 2N3905 and 2N3906, respectively.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current	I_C	200	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$	P_D	350	mW
Derate above 25°C		2.73	mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	$^\circ\text{C}/\text{mW}$

2N3903, 2N3904 (continued)

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Breakdown Voltage ($I_C = 10 \mu\text{A dc}$, $I_E = 0$)		BV_{CBO}	60	-	Vdc
Collector-Emitter Breakdown Voltage* ($I_C = 1.0 \text{ mA dc}$, $I_B = 0$)		BV_{CEO}^*	40	-	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10 \mu\text{A dc}$, $I_C = 0$)		BV_{EBO}	6.0	-	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $V_{EB(\text{off})} = 3.0 \text{ Vdc}$)		I_{CEX}	-	50	nA dc
Base Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $V_{EB(\text{off})} = 3.0 \text{ Vdc}$)		I_{BL}	-	50	nA dc
ON CHARACTERISTICS					
DC Current Gain* ($I_C = 0.1 \text{ mA dc}$, $V_{CE} = 1.0 \text{ Vdc}$)	2N3903 2N3904	h_{FE}^*	20 40	-	-
($I_C = 1.0 \text{ mA dc}$, $V_{CE} = 1.0 \text{ Vdc}$)	2N3903 2N3904		35 70	-	-
($I_C = 10 \text{ mA dc}$, $V_{CE} = 1.0 \text{ Vdc}$)	2N3903 2N3904		50 100	150 300	-
($I_C = 50 \text{ mA dc}$, $V_{CE} = 1.0 \text{ Vdc}$)	2N3903 2N3904		30 60	-	-
($I_C = 100 \text{ mA dc}$, $V_{CE} = 1.0 \text{ Vdc}$)	2N3903 2N3904		15 30	-	-
Collector-Emitter Saturation Voltage* ($I_C = 10 \text{ mA dc}$, $I_B = 1.0 \text{ mA dc}$) ($I_C = 30 \text{ mA dc}$, $I_B = 5.0 \text{ mA dc}$)	16, 17	$V_{CE(\text{sat})}^*$	- -	0.2 0.3	Vdc
Base-Emitter Saturation Voltage* ($I_C = 10 \text{ mA dc}$, $I_B = 1.0 \text{ mA dc}$) ($I_C = 50 \text{ mA dc}$, $I_B = 5.0 \text{ mA dc}$)	17	$V_{BE(\text{sat})}^*$	0.65 -	0.65 0.95	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain-Bandwidth Product ($I_C = 10 \text{ mA dc}$, $V_{CE} = 20 \text{ Vdc}$, $f = 100 \text{ MHz}$)	2N3903 2N3904	f_T	250 300	-	MHz
Output Capacitance ($V_{CB} = 5.0 \text{ Vdc}$, $I_E = 0$, $f = 100 \text{ kHz}$)		C_{ob}	-	4.0	pF
Input Capacitance ($V_{BE} = 0.5 \text{ Vdc}$, $I_C = 0$, $f = 100 \text{ kHz}$)		C_{ib}	-	8.0	pF
Input Impedance ($I_C = 1.0 \text{ mA dc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	2N3903 2N3904	h_{ie}	0.5 1.0	8.0 10	k ohms
Voltage Feedback Ratio ($I_C = 1.0 \text{ mA dc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	2N3903 2N3904	h_{re}	0.1 0.5	5.0 8.0	$\times 10^{-4}$
Small-Signal Current Gain ($I_C = 1.0 \text{ mA dc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	2N3903 2N3904	h_{fe}	50 100	200 400	-
Output Admittance ($I_C = 1.0 \text{ mA dc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)		h_{oe}	1.0	40	μmhos
Noise Figure ($I_C = 100 \mu\text{A dc}$, $V_{CE} = 5.0 \text{ Vdc}$, $R_S = 1.0 \text{ k ohms}$, $f = 10 \text{ Hz}$ to 15.7 kHz)	2N3903 2N3904	NF	-	6.0 5.0	dB
SWITCHING CHARACTERISTICS					
Delay Time ($V_{CC} = 3.0 \text{ Vdc}$, $V_{BE(\text{off})} = 0.5 \text{ Vdc}$, $I_C = 10 \text{ mA dc}$, $I_{B1} = 1.0 \text{ mA dc}$)		1, 5	t_d	-	35 ns
Rise Time ($V_{CC} = 3.0 \text{ Vdc}$, $V_{BE(\text{off})} = 0.5 \text{ Vdc}$, $I_C = 10 \text{ mA dc}$, $I_{B1} = 1.0 \text{ mA dc}$)		1, 5, 6	t_r	-	35 ns
Storage Time ($V_{CC} = 3.0 \text{ Vdc}$, $I_C = 10 \text{ mA dc}$, $I_{B1} = I_{B2} = 1.0 \text{ mA dc}$)	2N3903 2N3904	2, 7	t_s	-	175 200 ns
Fall Time ($V_{CC} = 3.0 \text{ Vdc}$, $I_C = 10 \text{ mA dc}$, $I_{B1} = I_{B2} = 1.0 \text{ mA dc}$)		2, 8	t_f	-	50 ns

* Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2.0%.

FIGURE 1 — DELAY AND RISE TIME EQUIVALENT TEST CIRCUIT

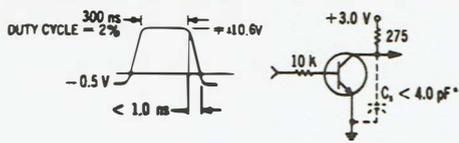
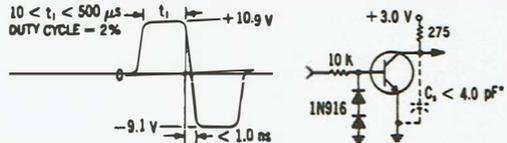


FIGURE 2 — STORAGE AND FALL TIME EQUIVALENT TEST CIRCUIT



*Total shunt capacitance of test jig and connectors

2N3903, 2N3904 (continued)

TRANSIENT CHARACTERISTICS

— $T_j = 25^\circ\text{C}$... $T_j = 125^\circ\text{C}$

FIGURE 3 — CAPACITANCE

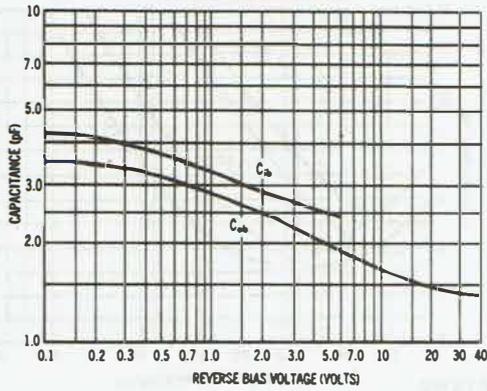


FIGURE 4 — CHARGE DATA

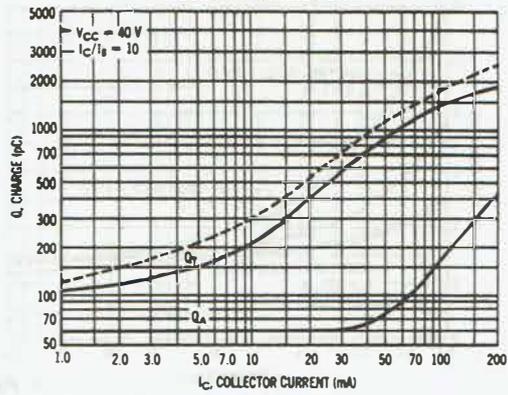


FIGURE 5 — TURN-ON TIME

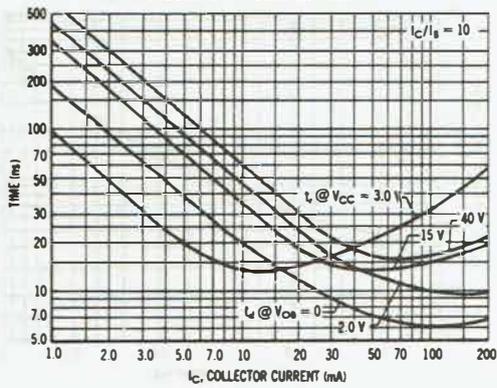


FIGURE 6 — RISE TIME

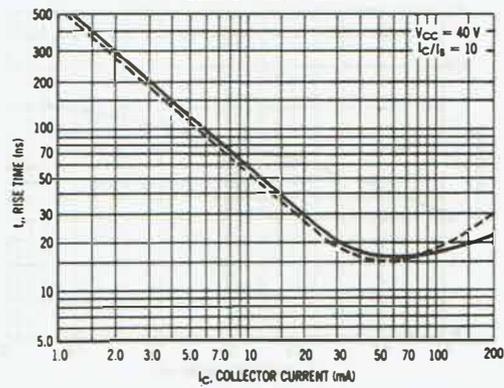


FIGURE 7 — STORAGE TIME

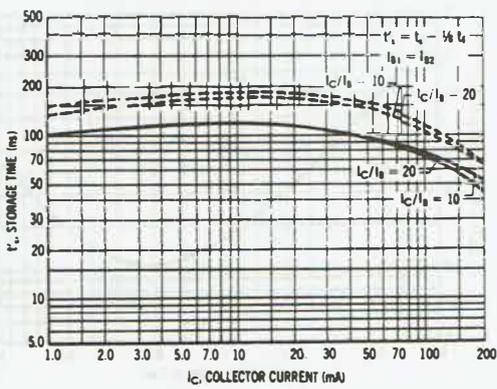
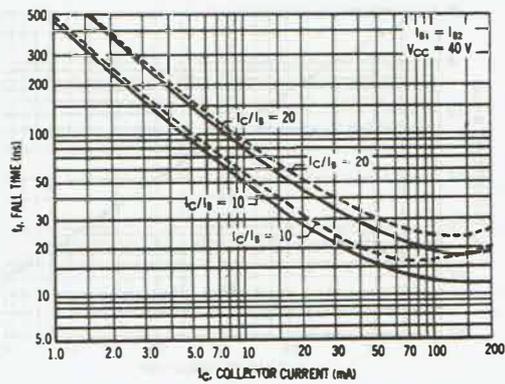


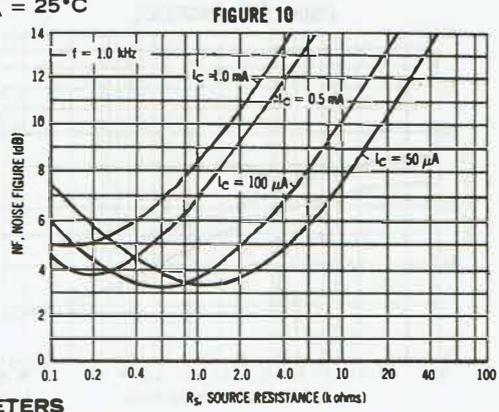
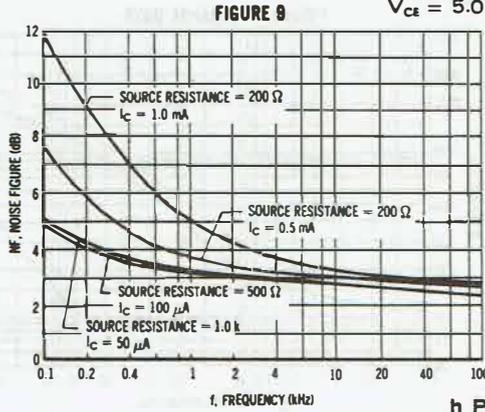
FIGURE 8 — FALL TIME



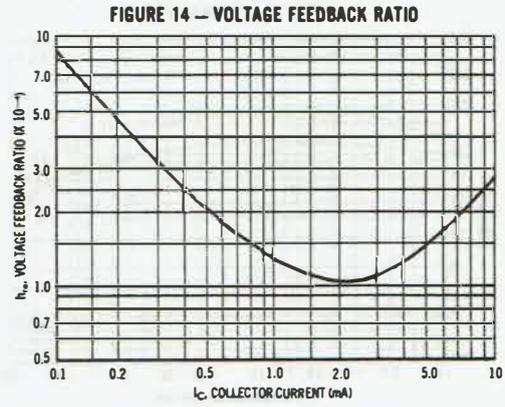
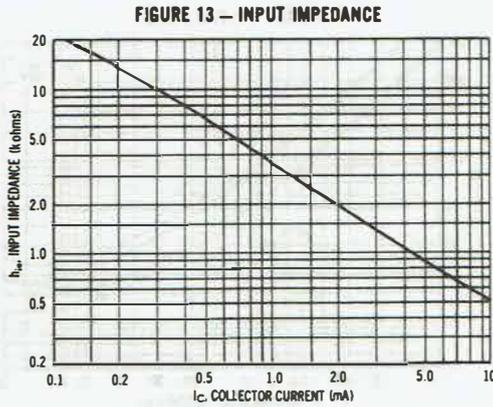
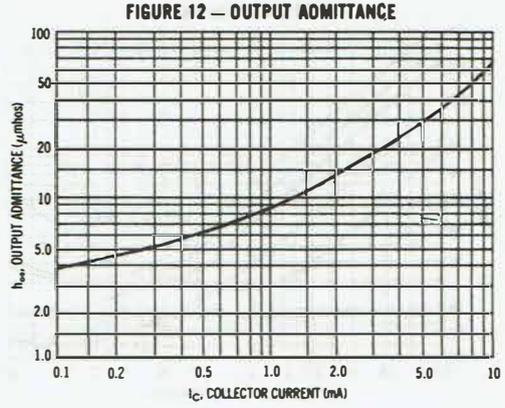
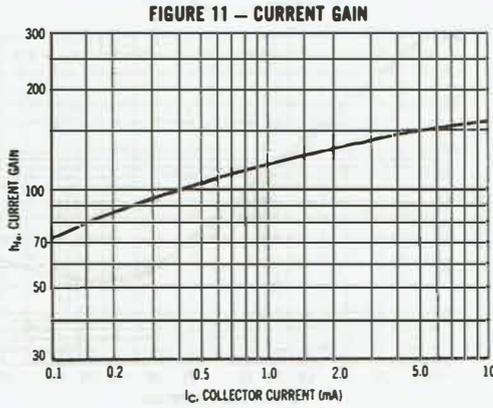
2N3903, 2N3904 (continued)

AUDIO SMALL SIGNAL CHARACTERISTICS

NOISE FIGURE VARIATIONS
 $V_{CE} = 5.0 \text{ Vdc}$, $T_A = 25^\circ\text{C}$



h PARAMETERS
 $(V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ kHz}, T_A = 25^\circ\text{C})$



2N3903, 2N3904 (continued)

STATIC CHARACTERISTICS

FIGURE 15 – NORMALIZED CURRENT GAIN

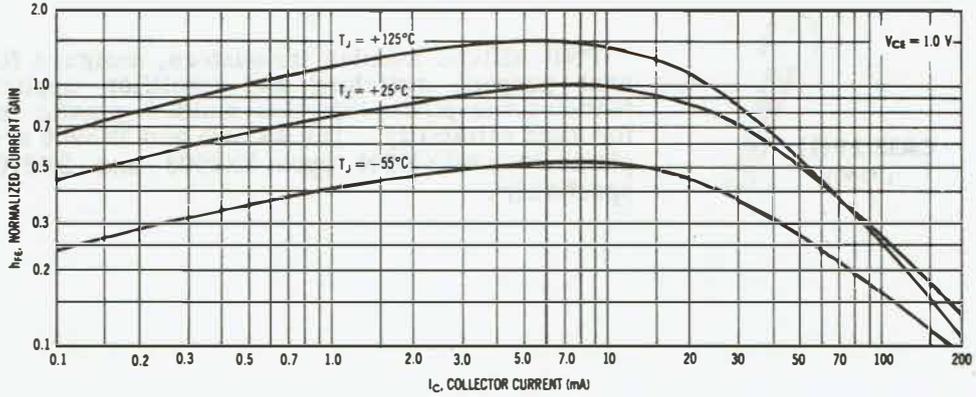


FIGURE 16 – COLLECTOR SATURATION REGION

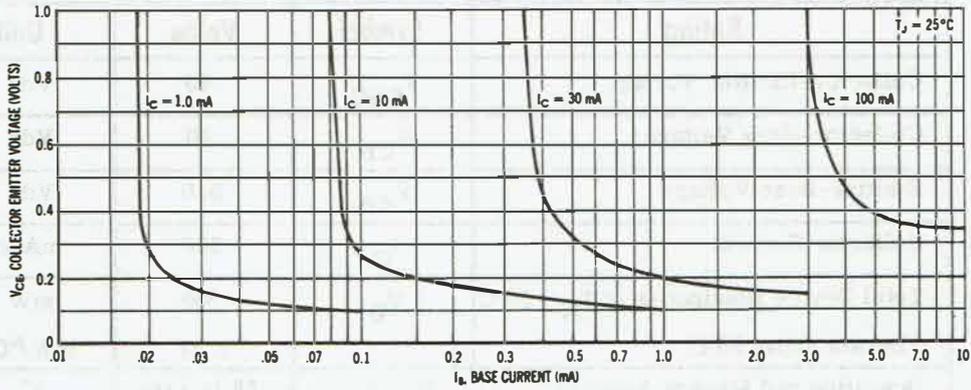


FIGURE 17 – "ON" VOLTAGES

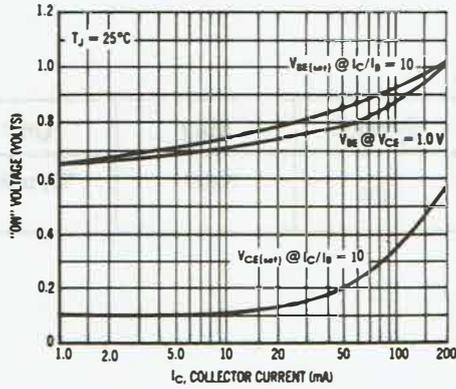
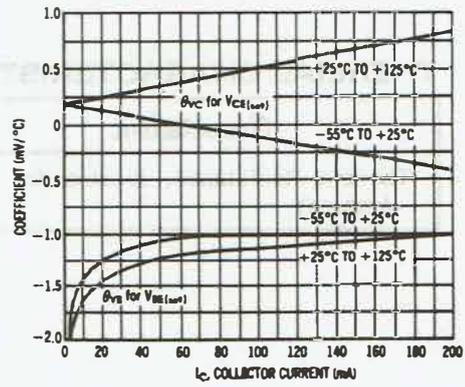
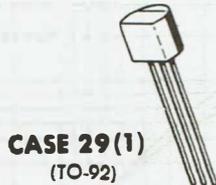


FIGURE 18 – TEMPERATURE COEFFICIENTS



2N3905 (SILICON)**2N3906**

PNP silicon annular transistors, designed for general purpose switching and amplifier applications, features one-piece, injection-molded plastic package for high reliability. The 2N3905 and 2N3906 are complementary with NPN types 2N3903 and 2N3904, respectively.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	200	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$	P_D	350	mW
Derate above 25°C		2.73	mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	$^\circ\text{C}/\text{mW}$

2N3905, 2N3906 (continued)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Breakdown Voltage (I _C = 10 μA, I _E = 0)		BV _{CBO}	40	-	Vdc
Collector-Emitter Breakdown Voltage (1) (I _C = 1.0 mA, I _B = 0)		BV _{CEO}	40	-	Vdc
Emitter-Base Breakdown Voltage (I _E = 10 μA, I _C = 0)		BV _{EBO}	5.0	-	Vdc
Collector Cutoff Current (V _{CE} = 30 Vdc, V _{BE(off)} = 3.0 Vdc)		I _{CEX}	-	50	nA
Base Cutoff Current (V _{CE} = 30 Vdc, V _{BE(off)} = 3.0 Vdc)		I _{BL}	-	50	nA

ON CHARACTERISTICS						
DC Current Gain (1) (I _C = 0.1 mA, V _{CE} = 1.0 Vdc)	2N3905 2N3906	15	h _{FE}	30	-	-
(I _C = 1.0 mA, V _{CE} = 1.0 Vdc)	2N3905 2N3906			40	-	-
(I _C = 10 mA, V _{CE} = 1.0 Vdc)	2N3905 2N3906			50	150	300
(I _C = 50 mA, V _{CE} = 1.0 Vdc)	2N3905 2N3906			30	-	-
(I _C = 100 mA, V _{CE} = 1.0 Vdc)	2N3905 2N3906			15	-	-
(I _C = 100 mA, V _{CE} = 1.0 Vdc)	2N3905 2N3906			30	-	-
Collector-Emitter Saturation Voltage (1) (I _C = 10 mA, I _B = 1.0 mA) (I _C = 50 mA, I _B = 5.0 mA)		16, 17	V _{CE(sat)}	-	0.25 0.4	Vdc
Base-Emitter Saturation Voltage (1) (I _C = 10 mA, I _B = 1.0 mA) (I _C = 50 mA, I _B = 5.0 mA)		17	V _{BE(sat)}	0.65	0.85 0.86	Vdc

SMALL-SIGNAL CHARACTERISTICS						
Current-Gain-Bandwidth Product (I _C = 10 mA, V _{CE} = 20 Vdc, f = 100 MHz)	2N3905 2N3906		f _T	200 250	-	MHz
Output Capacitance (V _{CB} = 5.0 Vdc, I _E = 0, f = 100 kHz)		3	C _{ob}	-	4.5	pF
Input Capacitance (V _{BE} = 0.5 Vdc, I _C = 0, f = 100 kHz)		3	C _{ib}	-	10	pF
Input Impedance (I _C = 1.0 mA, V _{CE} = 10 Vdc, f = 1.0 kHz)	2N3905 2N3906	13	h _{ie}	0.5 2.0	8.0 12	k ohms
Voltage Feedback Ratio (I _C = 1.0 mA, V _{CE} = 10 Vdc, f = 1.0 kHz)	2N3905 2N3906	14	h _{re}	0.1 1.0	5.0 10	X 10 ⁻⁴
Small-Signal Current Gain (I _C = 1.0 mA, V _{CE} = 10 Vdc, f = 1.0 kHz)	2N3905 2N3906	11	h _{fe}	50 100	200 400	-
Output Admittance (I _C = 1.0 mA, V _{CE} = 10 Vdc, f = 1.0 kHz)	2N3905 2N3906	12	h _{oe}	1.0 5.0	40 60	μmhos
Noise Figure (I _C = 100 μA, V _{CE} = 5.0 Vdc, R _B = 1.0 k ohm, f = 10 Hz to 15.7 kHz)	2N3905 2N3906	9, 10	NF	-	5.0 4.0	dB

SWITCHING CHARACTERISTICS						
Delay Time	(V _{CC} = 3.0 Vdc, V _{BE(off)} = 0.5 Vdc, I _C = 10 mA, I _{B1} = 1.0 mA)	1, 5	t _d	-	35	ns
Rise Time		1, 5, 6	t _r	-	35	ns
Storage Time	(V _{CC} = 3.0 Vdc, I _C = 10 mA, I _{B1} = I _{B2} = 1.0 mA)	2, 7	t _s	-	200 235	ns
Fall Time		3, 8	t _f	-	60 75	ns

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

FIGURE 1 — DELAY AND RISE TIME EQUIVALENT TEST CIRCUIT

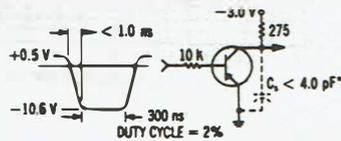
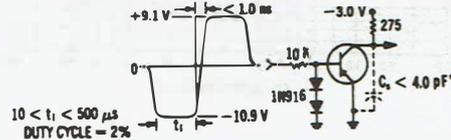


FIGURE 2 — STORAGE AND FALL TIME EQUIVALENT TEST CIRCUIT



*Total shunt capacitance of test jig and connectors

2N3905, 2N3906 (continued)

TRANSIENT CHARACTERISTICS
 — $T_j = 25^\circ\text{C}$ --- $T_j = 125^\circ\text{C}$

FIGURE 3 — CAPACITANCE

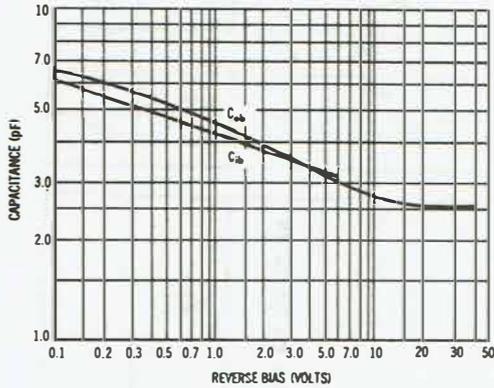


FIGURE 4 — CHARGE DATA

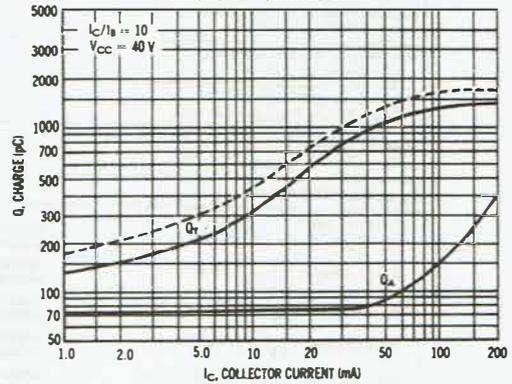


FIGURE 5 — TURN-ON TIME

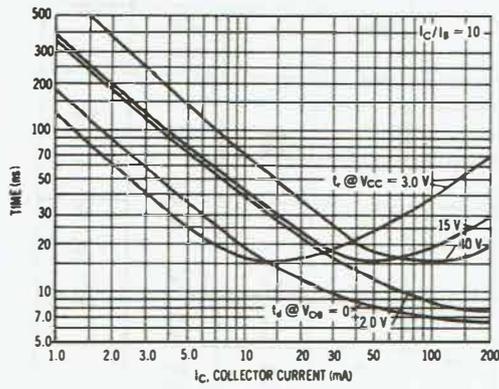


FIGURE 6 — RISE TIME

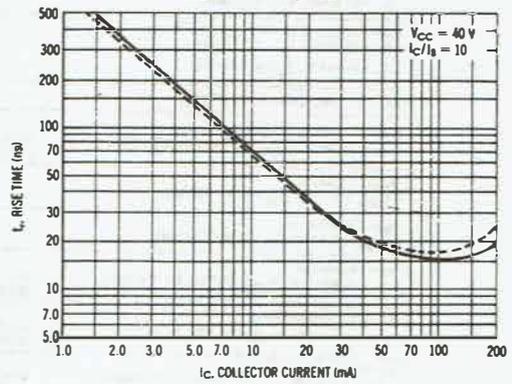


FIGURE 7 — STORAGE TIME

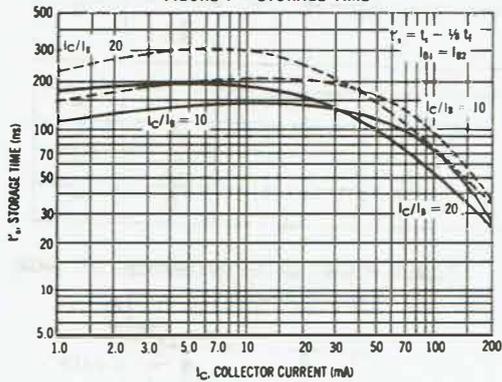
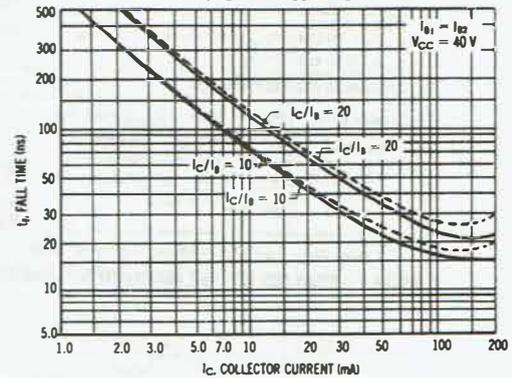


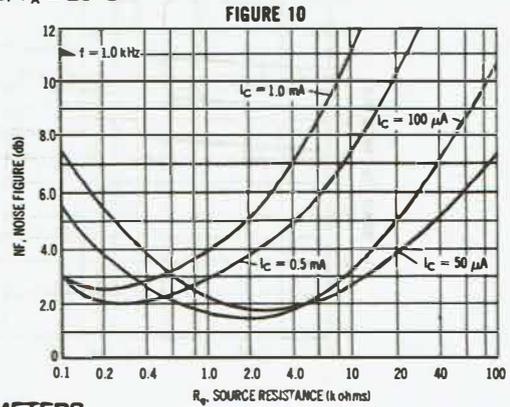
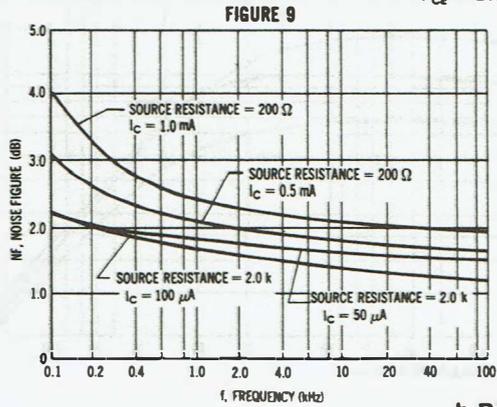
FIGURE 8 — FALL TIME



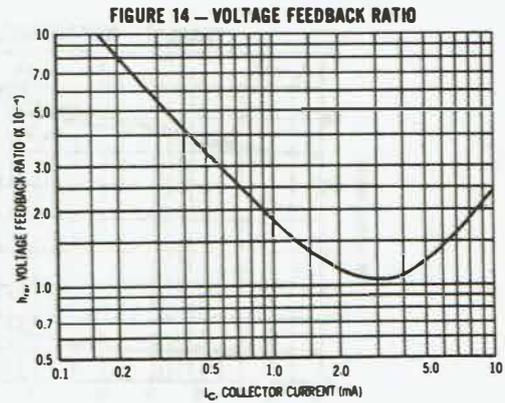
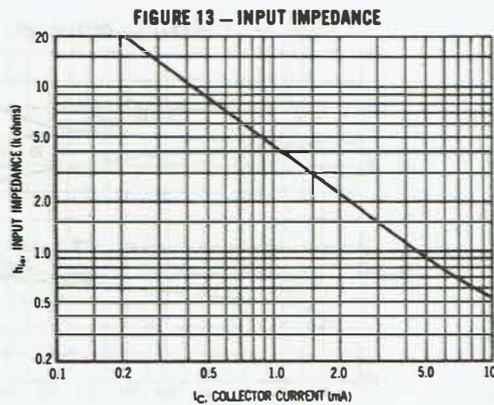
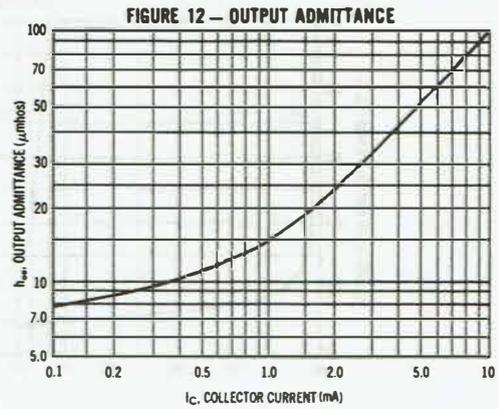
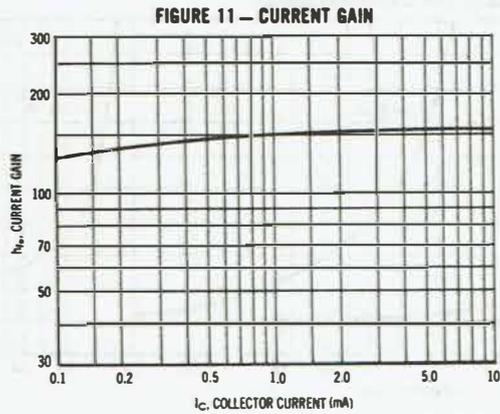
2N3905, 2N3906 (continued)

AUDIO SMALL SIGNAL CHARACTERISTICS

NOISE FIGURE VARIATIONS
 $V_{CE} = 5.0 \text{ Vdc}$, $T_A = 25^\circ\text{C}$



h PARAMETERS
 $(V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$, $T_A = 25^\circ\text{C})$



2N3905, 2N3906 (continued)

STATIC CHARACTERISTICS

FIGURE 15 — NORMALIZED CURRENT GAIN

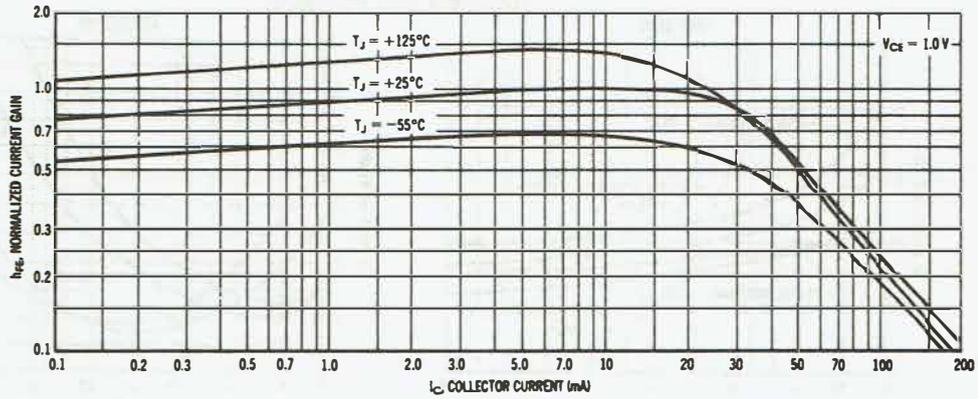


FIGURE 16 — COLLECTOR SATURATION REGION

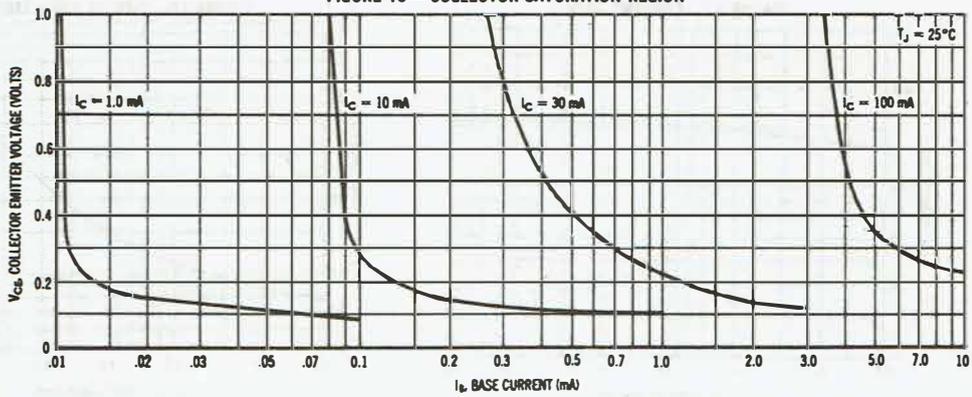


FIGURE 17 — "ON" VOLTAGES

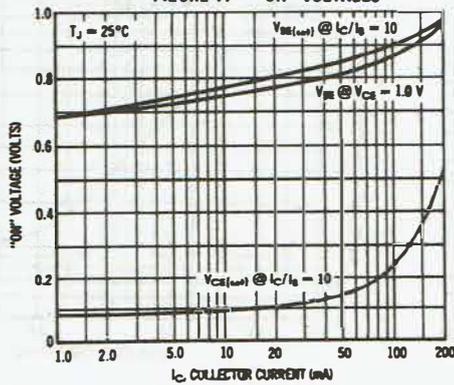
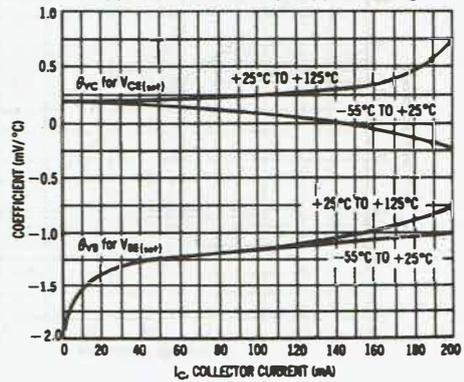


FIGURE 18 — TEMPERATURE COEFFICIENTS




MOTOROLA
**SILICON N-CHANNEL
JUNCTION FIELD-EFFECT TRANSISTORS**

... depletion mode (Type A) transistors designed for general-purpose audio and switching applications.

- N-Channel for Higher Gain
- Drain and Source Interchangeable
- High AC Input Impedance
- High DC Input Resistance
- Low Transfer and Input Capacitance
- Low Cross-Modulation and Intermodulation Distortion
- Unibloc* Plastic Encapsulated Package

MAXIMUM RATINGS

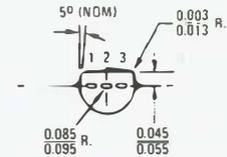
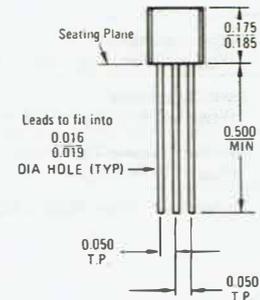
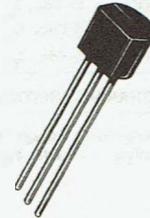
Characteristic	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	-25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	310 2.82	mW mW/ $^\circ\text{C}$
Operating Junction Temperature	T_J	135	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

*Trademark of Motorola Inc.

2N5457
2N5458
2N5459
**JUNCTION
FIELD-EFFECT
TRANSISTORS**
**SYMMETRICAL
SILICON
N-CHANNEL**

JULY 1968 - DS 5207 R2
(Replaces DS 5207 R1)

Type A



To convert inches to millimeters multiply by 25.4
All JEDEC dimensions and notes apply

CASE 29-01
TO-92
PLASTIC

MOTOROLA Semiconductor Products Inc.


A SUBSIDIARY OF MOTOROLA INC.

2N5457, 2N5458, 2N5459

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Gate-Source Breakdown Voltage ($I_G = -10\mu\text{Adc}$, $V_{DS} = 0$)	BV_{GSS}	-25	—	—	Vdc
Gate Reverse Current ($V_{GS} = -15\text{ Vdc}$, $V_{DS} = 0$) ($V_{GS} = -15\text{ Vdc}$, $V_{DS} = 0$, $T_A = 100^\circ\text{C}$)	I_{GSS}	—	—	-1.0 -200	nAdc
Gate-Source Cutoff Voltage ($V_{DS} = 15\text{ Vdc}$, $I_D = 10\text{ nAdc}$)	$V_{GS(\text{off})}$	-0.5 -1.0 -2.0	—	-6.0 -7.0 -8.0	Vdc
Gate-Source Voltage ($V_{DS} = 15\text{ Vdc}$, $I_D = 100\mu\text{Adc}$) ($V_{DS} = 15\text{ Vdc}$, $I_D = 200\mu\text{Adc}$) ($V_{DS} = 15\text{ Vdc}$, $I_D = 400\mu\text{Adc}$)	V_{GS}	—	-2.5 -3.5 -4.5	—	Vdc
ON CHARACTERISTICS					
Zero-Gate-Voltage Drain Current* ($V_{DS} = 15\text{ Vdc}$, $V_{GS} = 0$)	I_{DSS}^*	1.0 2.0 4.0	3.0 6.0 9.0	5.0 9.0 16	mAdc
DYNAMIC CHARACTERISTICS					
Forward Transfer Admittance* ($V_{DS} = 15\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ kHz}$)	$ y_{fs} ^*$	1000 1500 2000	3000 4000 4500	5000 5500 6000	μmhos
Output Admittance* ($V_{DS} = 15\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ kHz}$)	$ y_{os} ^*$	—	10	50	μmhos
Input Capacitance ($V_{DS} = 15\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{iss}	—	4.5	7.0	pF
Reverse Transfer Capacitance ($V_{DS} = 15\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{rss}	—	1.5	3.0	pF

*Pulse Test: Pulse Width $\leq 630\text{ ms}$; Duty Cycle $\leq 10\%$ 
MOTOROLA Semiconductor Products Inc.

BOX 20912 • PHOENIX, ARIZONA 85036 • A SUBSIDIARY OF MOTOROLA INC.

Original Formula	Approximate Formula
$\alpha = \frac{I_C - I_{CBO}}{I_E}$	$\alpha = \frac{I_C}{I_E}$
$B = \frac{I_C - I_{CBO}}{I_B + I_{CBO}}$	$B = \frac{I_C}{I_B}$
$I_C = \alpha I_E + I_{CBO}$	$I_C = \alpha I_E$
$I_C = B I_B + I_{CBO} (B + 1)$ $I_C = B I_B + I_{CEO}$	$I_C = B I_B$
$I_B = \frac{I_E}{B + 1} - I_{CBO}$	$I_B = \frac{I_E}{B}$

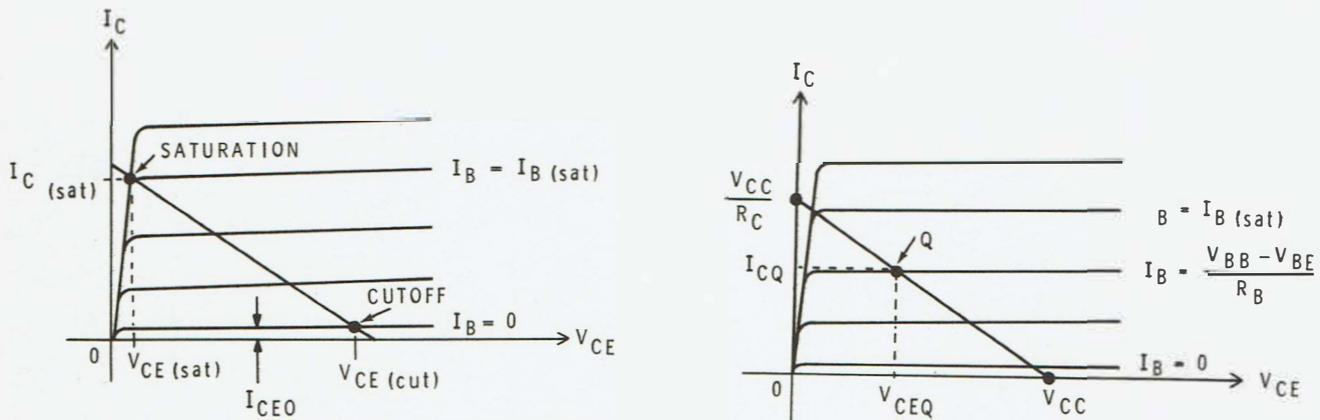
TABLE 1-3

Approximate BJT Formulas (from Page 1-35)

Mode	Original Formula	Approximate Formula	Comment
Cutoff	$I_B = 0$ $I_C = I_E = I_{CEO}$ $V_{CE(cut)} = V_{CC} - I_{CEO} R_C$	$I_C = I_E = 0$ $V_{CE(cut)} = V_{CC}$	Collector and emitter terminals approximate an open circuit.
Saturation	$I_B \geq I_{B(sat)}$ $I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$ $V_{CE} = V_{CE(sat)}$	$I_{C(sat)} = \frac{V_{CC}}{R_C}$ $V_{CE(sat)} = 0$	Collector and emitter terminals approximate a short circuit.
Active	$I_B = \frac{V_{BB} - V_{BE}}{R_B}$ $I_C \approx \beta I_B = I_E$ $V_{CE} = V_{CC} - I_C R_C$	<p>_____</p> <p>_____</p> <p>_____</p>	Operating point is usually near the middle of the load line.

TABLE 2-1

Summary Of Modes And Formulas For The Common-Emitter Base-Biased Circuit. (from Page 2-13)



SATURATION AND CUT OFF POINTS ON THE DC LOAD LINE. A QUIESCENT, Q, OPERATING POINT IN THE ACTIVE REGION.

Figure 2-2

The DC load line (from Page 2-11)

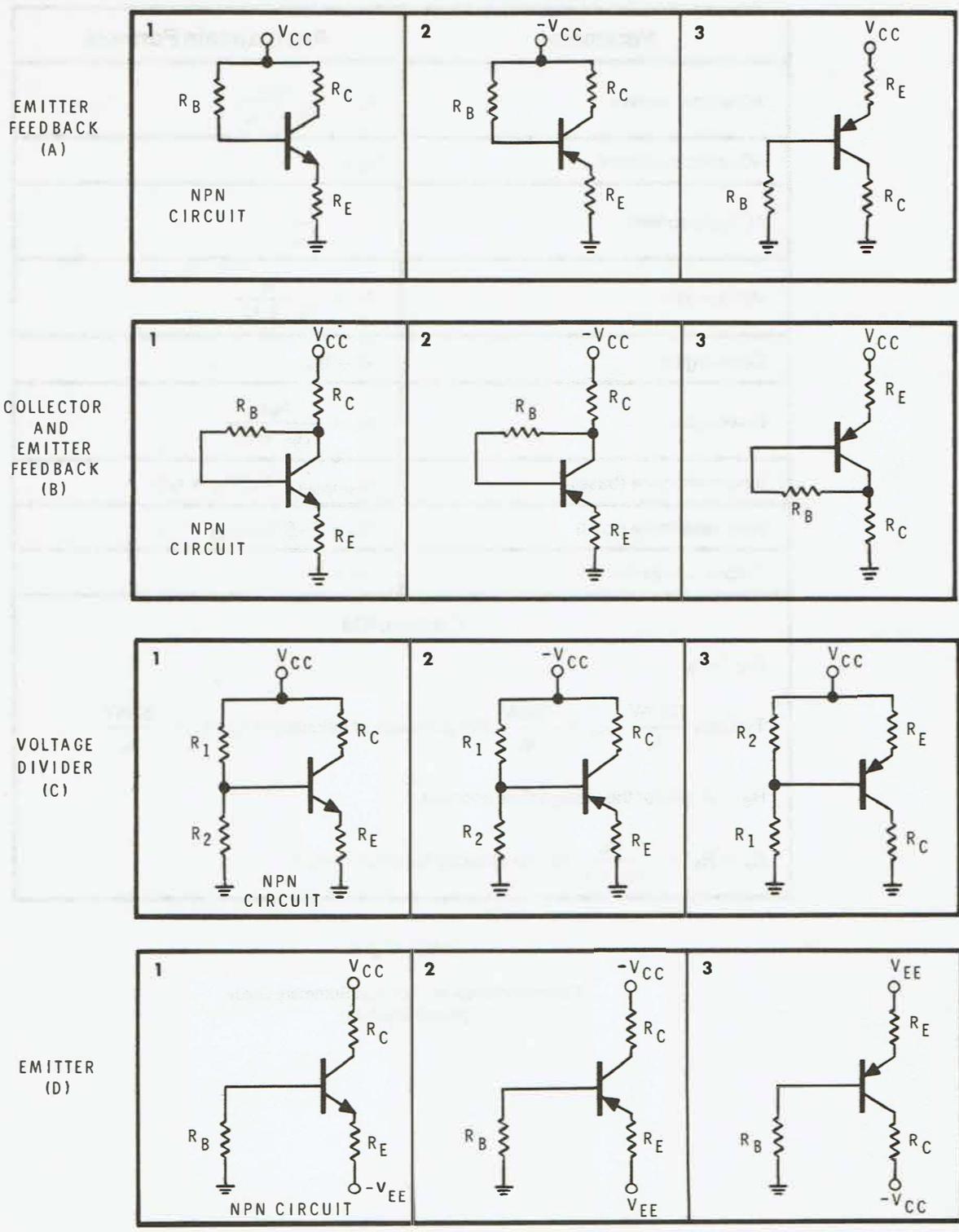


Figure 2-33

NPN and complementary PNP circuits for typical biasing schemes.
 Box 3 shows how the PNP circuit appears on most schematic diagrams.
 (from Page 2-88)

- A. Emitter Feedback.
- B. Collector and Emitter Feedback.
- C. Voltage Divider.
- D. Emitter.

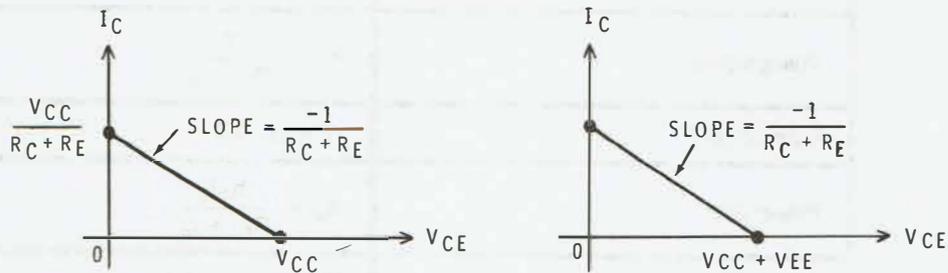
Parameter	Approximate Formula
AC emitter current	$i_C = \frac{v_{IN}}{R_{E_1} + r_{e'}}$
AC collector current	$i_C = i_e$
AC base current	$i_C = \frac{i_C}{h_{fe}}$
Voltage gain	$A_V = \frac{-r_L}{R_{E_1} + r_{e'}}$
Current gain	$A_i = h_{fe}$
Power gain	$A_P = \frac{h_{fe} r_L}{R_{E_1} + r_{e'}}$
Input resistance (base)	$R_{IN(BASE)} = h_{fe}(R_{E_1} + r_{e'})$
Input resistance (total)	$R_{IN} = R_B \parallel R_{IN(BASE)}$
Output resistance	$R_O \approx R_C$
Comments	
$B_{AC} = h_{fe}$ Typically $\frac{26mV}{I_E} \leq r_{e'} \leq \frac{52mV}{I_E}$. For purposes of calculation, use $r_{e'} = \frac{37mV}{I_E}$ $R_B = R_1 \parallel R_2$ for the voltage divider circuit. $R_B = R_{B'} = \frac{R_B}{A_V + 1}$ for the collector feedback circuit.	

TABLE 3-1

Common-Emitter AC Formula Summary Guide
(from Page 3-44)

(A)

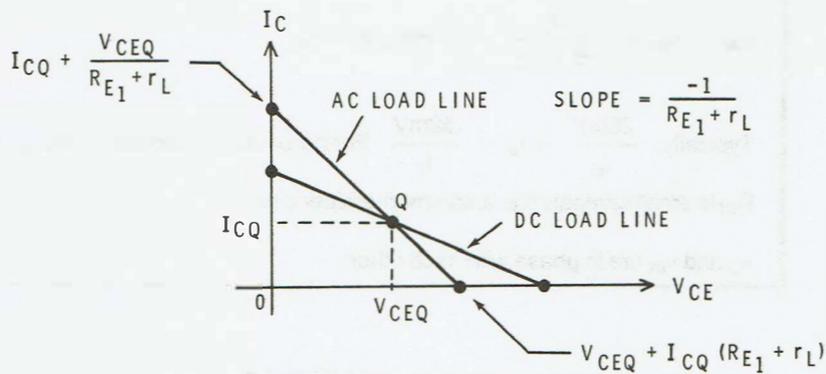
DC LOAD LINES



EMITTER FEEDBACK, COLLECTOR FEEDBACK, AND VOLTAGE DIVIDER CIRCUITS

EMITTER BIAS CIRCUIT

(B)



THE AC LOAD LINE

Figure 3-22

Common emitter DC and AC load lines. (from Page 3-51)

- A. DC load lines.
- B. The AC load line.

Parameter	Approximate Formula
AC emitter current	$i_e = \frac{v_{IN}}{R_{E_1} + r_{e'}}$
AC collector current	$i_C \approx i_e$
AC base current	$i_b = \frac{i_C}{h_{fe}}$
Voltage gain	$A_V = \frac{r_L}{R_{E_1} + r_{e'}}$
Current gain	$A_i = h_{fb} \approx 1$
Power gain	$A_p = \frac{h_{fb} r_L}{R_{E_1} + r_{e'}}$
Input resistance (emitter)	$R_{IN(EMITTER)} = r_{e'}$
Input resistance (total)	$R_{IN} = R_{E_2} \parallel (R_{E_1} + r_{e'})$
Output resistance	$R_O \approx R_C$
<u>Comments</u>	
$\alpha_{AC} = h_{fb} = \frac{B}{(B + 1)} \approx 1, \text{ where } B = h_{fe}$	
<p>Typically, $\frac{26\text{mV}}{I_E} \leq r_{e'} \leq \frac{52\text{mV}}{I_E}$. For purposes of calculation use $r_{e'} = \frac{37\text{mV}}{I_E}$</p>	
<p>R_{IN} is small compared to a common-emitter circuit.</p>	
<p>v_O and v_{IN} are in phase with each other.</p>	

TABLE 4-1

Common-Base AC Formula Summary Guide
(from Page 4-11)

Parameter	Approximate Formula
AC emitter current	$i_e = \frac{v_{IN}}{R_L + r_{e'}}$
AC collector current	$i_C \approx i_e$
AC base current	$i_b = \frac{i_C}{h_{fe}}$
Voltage gain	$A_V = \frac{r_L}{r_L + r_{e'}}$
Current gain	$A_i = h_{fe}$
Power gain	$A_p = \frac{h_{fe} r_L}{r_L + r_{e'}}$
Input resistance (base)	$R_{IN(BASE)} = h_{fe}(r_L + r_{e'})$
Input resistance (total)	$R_{IN} = R_B h_{fe}(r_L + r_{e'})$
Output resistance	$R_O \approx [r_{e'} + \frac{R_B R_S}{h_{fe}}] R_E$
<u>Comments</u>	
R_{IN} is large, R_O small, and $A_V \approx 1$.	
Applications include buffers and impedance matching.	
v_O and v_{IN} are in phase with each other.	

TABLE 4-2

Common Collector/Emitter-Follower AC Formula Summary Guide (from Page 4-39)

Parameter	Definition	Description
h_{11}	$\frac{v_1}{i_1} \Big _{v_2 = 0}$	short-circuit input impedance
h_{21}	$\frac{i_2}{i_1} \Big _{v_2 = 0}$	short-circuit forward current gain
h_{12}	$\frac{v_1}{v_2} \Big _{i_1 = 0}$	open-circuit reverse voltage gain
h_{22}	$\frac{i_2}{v_2} \Big _{i_1 = 0}$	open-circuit output admittance

TABLE 4-3

Hybrid Parameters from Page 4-71

Parameter	Formula
Current gain	$A_i = \frac{h_{21}}{1 + h_{22}r_L}$
Voltage gain	$A_v = \frac{h_{21}r_L}{h_{12}h_{21}r_L - h_{11}(1 + h_{22}r_L)}$
Power gain	$A_p = A_i A_v$
Input resistance	$R_{IN} = h_{11} - \frac{h_{12}h_{21}r_L}{1 + h_{22}r_L}$
Output resistance	$R_O = \frac{1}{h_{22} - \frac{h_{12}h_{21}}{h_{11} + R_S}}$

TABLE 4-4

Two-Port Network Hybrid Parameter Formulas (from Page 4-73)

Parameter	Description	CE	CB	CC
h_{11}	Short-circuit input impedance.	h_{ie}	h_{ib}	h_{ic}
h_{21}	Short-circuit forward current gain.	h_{fe}	h_{fb}	h_{fc}
h_{12}	Open-circuit reverse voltage gain.	h_{re}	h_{rb}	h_{rc}
h_{22}	Open-circuit output admittance.	h_{oe}	h_{ob}	h_{oc}

TABLE 4-5

BJT h parameter Notation (from Page 4-74)

CE → CB	CE → CC
$h_{ib} = \frac{h_{ie}}{h_{fe} + 1}$ $h_{fb} = \frac{-h_{fe}}{h_{fe} + 1}$ $h_{rb} = \frac{h_{ie}h_{oe}}{h_{fe} + 1} - h_{re}$ $h_{ob} = \frac{h_{oe}}{h_{fe} + 1}$	$h_{ic} = h_{ie}$ $h_{fc} = -(h_{fe} + 1)$ $h_{rc} = 1 - h_{re} \approx 1$ $h_{oc} = h_{oe}$
CB → CE	CB → CC
$h_{ie} = \frac{h_{ib}}{h_{fb} + 1}$ $h_{fe} = \frac{-h_{fb}}{h_{fb} + 1}$ $h_{re} = \frac{h_{ib}h_{ob}}{h_{fb} + 1} - h_{rb}$ $h_{oe} = \frac{h_{ob}}{h_{fb} + 1}$	$h_{ic} = \frac{h_{ib}}{h_{fb} + 1}$ $h_{fc} = \frac{-1}{h_{fb} + 1}$ $h_{rc} = \frac{1 - h_{cb}h_{ob}}{h_{fb} + 1} + h_{rb}$ $h_{oc} = \frac{h_{ob}}{h_{fb} + 1}$

TABLE 4-6

Approximate h Parameter Conversion Formulas (from Page 4-75)

Parameter	Approximate Equivalents
α	$\frac{1}{1 - \frac{h_{rb} + 1}{h_{fb}}} = \frac{h_{fe}}{h_{fe} + 1}$
B	$\frac{-h_{rb}}{h_{rb} + 1} = h_{fe}$
r_e'	$h_{ib} = \frac{h_{ie}}{h_{fe}}$
r_b'	$\frac{h_{rb}}{h_{ob}} = h_{ie} - \frac{h_{fe}h_{re}}{h_{oe}}$
r_e'	$\frac{1}{h_{ob}} = \frac{h_{fe}}{h_{oe}}$

TABLE 4-7Useful Conversions
(from Page 4-80)

Parameter	Single Supply	Dual Supply
I	$\frac{V_{CC} - 1.4V}{R_1 + R_2}$	$\frac{2V_{CC} - 1.4V}{R_1 + R_2}$
V _{CE}	$V_{CE_1} = \frac{V_{CC}}{2}, V_{CE_2} = -\frac{V_{CC}}{2}$	$V_{CE_1} = V_{CC}, V_{CE_2} = -V_{CC}$
V _B	$V_{B_1} = V_{CC} - IR_1$ $V_{B_1} = V_{CC} - 0.7V$ $V_{B_2} = IR_2$	$V_{B_1} = V_{CC} - IR_1$ $V_{B_1} = V_{CC} - 0.7V$ $V_{B_2} = IR_2 - V_{CC}$
V _E	$ V_{E_1} = V_{E_2} = \frac{V_{CC}}{2}$	$V_{E_1} = V_{E_2} = 0V$
V _C	$V_{C_1} = V_{CC}, V_{C_2} = 0V$	$V_{C_1} = V_{CC}, V_{C_2} = -V_{CC}$
A _v	$A_v = \frac{R_L}{R_L + r_{e'}} \approx 1$	$A_v = \frac{R_L}{R_L + r_{e'}} \approx 1$
A _i , A _p	$A_i = h_{FE}, A_p = A_i A_v$	$A_i = h_{FE}, A_p = A_i A_v$
R _{IN}	$R_{IN} = R_1 \parallel R_2 \parallel h_{FE}(R_L + r_{e'})$	$R_{IN} = R_1 \parallel R_2 \parallel h_{FE}(R_L + r_{e'})$
P _{AC}	$\frac{(V_{CC})^2}{8R_L}$	$\frac{(V_{CC})^2}{2R_L}$
P _{DMAX}	$\frac{(V_{CC})^2}{40R_L} = \frac{P_{AC}}{5}$	$\frac{(V_{CC})^2}{10R_L} = \frac{P_{AC}}{5}$

TABLE 5-2

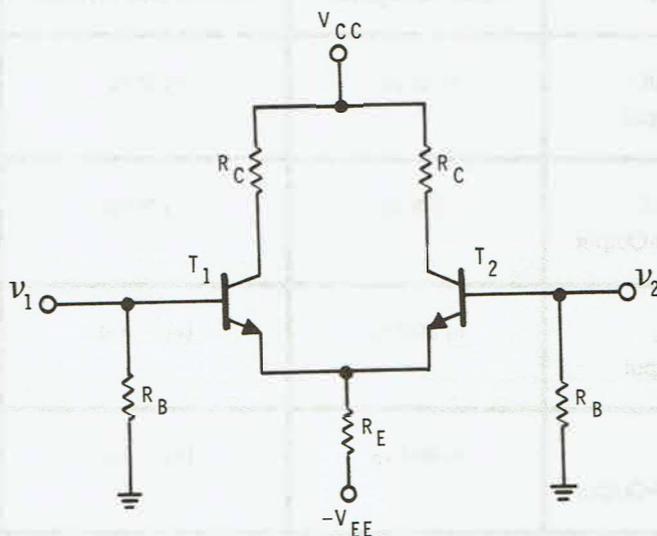
Summary of approximate formulas for the single and dual supply, complementary-symmetry push-pull class AB amplifiers. (from Page 5-71)

Mode	(v_{IN}) Input Voltage(s)	(v_d) Differential Voltage	(v_o) Output Voltage
Single-Input, Single-Output	v_1 OR v_2	v_1 OR v_2	$\frac{R_C}{2r_{e'}} v_{IN}$
Single-Input, Differential-Output	v_1 OR v_2	v_1 OR v_2	$\frac{R_C}{r_{e'}} v_{IN}$
Dual-Input, Single-Output	v_1 and v_2	$(v_1 - v_2)$	$\frac{R_C}{2r_{e'}} (v_1 - v_2)$
Dual-Input, Differential-Output	v_1 and v_2	$(v_1 - v_2)$	$\frac{R_C}{r_{e'}} (v_1 - v_2)$
Differential-Input, Single-Output	v_{IN}	v_{IN}	$\frac{R_C}{2r_{e'}} v_{IN}$
Differential-Input, Differential-Output	v_{IN}	v_{IN}	$\frac{R_C}{r_{e'}} v_{IN}$

Table 6-1

Differential Amplifier operating modes.
(from Page 6-35)

DIFFERENTIAL AMPLIFIER DESIGN GUIDE



1. Select I_S .

2. Calculate R_C .

$$R_C = \frac{V_{CC}}{I_S}$$

3. Calculate R_E .

$$R_E = \frac{V_{EE} - V_{BE}}{I_S}$$

4. Select R_B .

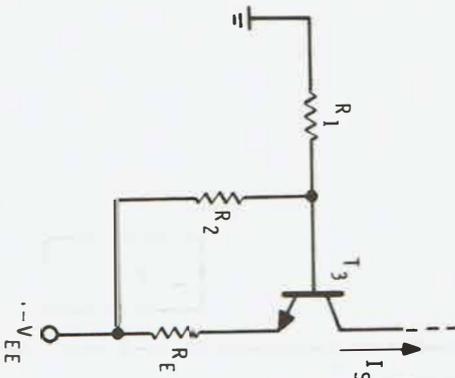
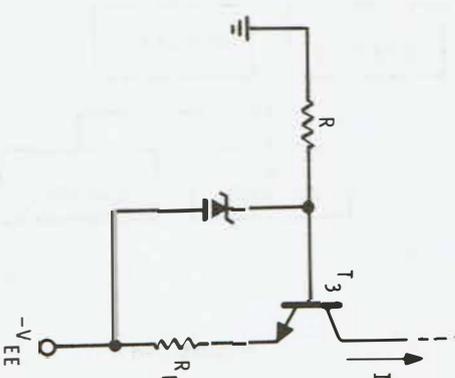
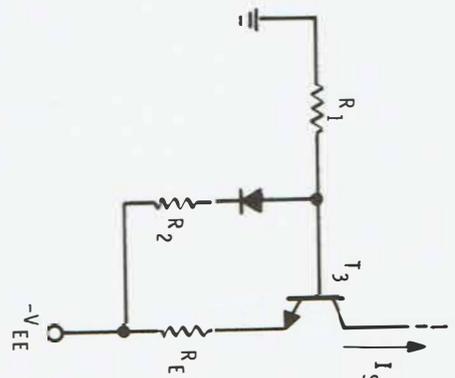
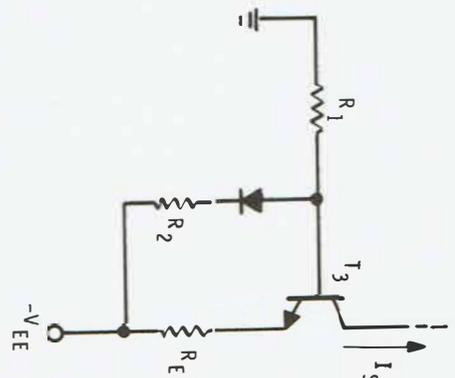
$R_B = 1k\Omega$ to $10k\Omega$ is typical.

To obtain a large CMRR, use a BJT constant current source in place of R_E . In this case, step 3 is replaced by steps 1 through 3 in the constant current source design guide.

(from Page 6-39)

CONSTANT CURRENT SOURCE DESIGN GUIDE

(from Page 6-40)

<p>1</p>  <ol style="list-style-type: none"> 1. Calculate V_{R_2}. $V_{R_2} = \frac{V_{EE}}{2}$ 2. Select R_1 & R_2. ($10k\Omega$ to $47k\Omega$ is typical.) $R_1 = R_2$ 3. Calculate R_E. $R_E = \frac{V_{R_2} - V_{BE}}{I_S}$ 	<p>2</p>  <ol style="list-style-type: none"> 1. Select V_Z. $V_Z \approx 1/3 \text{ to } 1/2 V_{EE}$ 2. Calculate R_E. $R_E = \frac{V_Z - V_{BE}}{I_S}$ 3. Calculate R. $R = \frac{V_{EE} - V_Z}{I_Z}$
<p>3</p>  <ol style="list-style-type: none"> 1. Calculate V_{R_2}. $V_{R_2} = \frac{V_{EE} - V_{BE}}{2}$ 2. Calculate R_E. $R_E = \frac{V_{R_2}}{I_S}$ 3. Select R_1 & R_2. ($10k\Omega$ to $47k\Omega$ is typical.) $R_1 = R_2$ 	<p>3</p> 

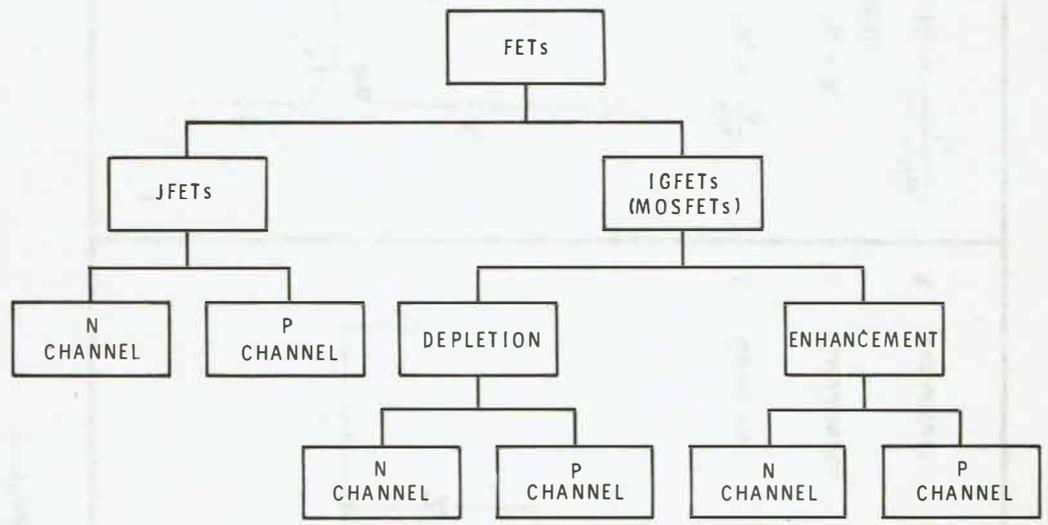


Figure 7-47

FET family tree.
(from Page 7-81)

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